ulm university universität
uulm

Fully Integrated, Multichannel IC for Brain Machine Interfaces

DISSERTATION

to obtain the academic degree

DOKTOR-INGENIEUR

(Dr.-Ing.)

at the faculty of Engineering, Computer Science and Psychology of the University of Ulm

by

Michael Haas

from Ochsenhausen

(Place of birth)

Supervisor:	Prof. Dr.-Ing. Maurits Ortmanns
Second Examiner:	Prof. Qiang Li
Officiating Dean:	Prof. Dr.-Ing. Maurits Ortmanns

Ulm, 20.09.2019

Declaration of Authorship

I, Michael Haas, declare that this thesis titled, 'Fully Integrated, Multichannel IC for Brain Machine Interfaces' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed:

Date:

Officiating Dean:	Prof. Dr.-Ing. Maurits Ortmanns
Committee Members:	Prof. Dr.-Ing. Maurits Ortmanns
	Prof. Qiang Li
	Prof. Dr.-Ing. Robert Fischer
	Prof. Dr.-Ing. Christian Damm

"One, remember to look up at the stars and not down at your feet. Two, never give up work. Work gives you meaning and purpose and life is empty without it. Three, if you are lucky enough to find love, remember it is there and don't throw it away."

Stephen Hawking (1942 - 2018)

To my wife Julia

Abstract

The rapid progress of technology in the semiconductor industry over the last decades allowed the development of a whole new generation of fully integrated neuromodulators. By an increase in the level of integration, new systems on chip (SoCs) that allow the simultaneous recording and stimulation of nervous signals were developed. These chips enable implantable, medical devices, capable of providing so far unreachable spatiotemporal resolution, while eliminating inflammation prone through-skin wires. The ongoing demand for higher spatial resolution, together with the tight power and size requirements imposed by implantation needs, result in growing challenges for the integrated circuit design.

Besides the fundamental requirements for power, area and noise, the unknown, biological system itself imposes the biggest challenge. Since the observable signals and the required stimulation patterns heavily depend on the physiology of each individual, all systems require high flexibility and maximum adaptability to the patient. The presented work deals with that challenge and presents new circuit architectures, that allow the reconfiguration of the recording system as well as the stimulation system to the current neurological state, while being implanted.

In the recording subsystem, a new tuning mechanism for the low noise amplifier is presented. It provides a flexible trade-off between noise performance and amplifier bandwidth, to adapt the recorder to the currently observed, neural signal. Further, electrode impedance estimation was introduced with a new low-gain recording mode. Thereby, the recorder is reused to acquire the impulse response of the electrode, which allows to detect broken wires or electrode degradation due to electrochemical processes.

In order to provide maximum flexibility for the stimulation, a novel, high voltage (HV) stimulator was developed, which is capable of providing current and voltage controlled, arbitrary stimulation waveforms. This was achieved by a new, semi-digital feedback loop, which controls the output current of the current stimulator in order to achieve the desired electrode voltage. Thereby, power efficient class-B operation is achieved, while requiring only little area overhead, as the full HV output stage is reused.

Both subsystems were combined, together with two high resolution analog to digital converters (ADCs), in a 32 channel SoC, which provides significant advantages for future implants by minimizing the required amount of off-chip components. Furthermore, integrated electrode monitoring improves patient safety and the increased flexibility in recording and stimulation improves the freedom in the design of experiments and therapies.

Acknowledgements

First and foremost, I would like to thank my supervisor Prof. Dr.-Ing Maurits Ortmanns for his consistent guidance, financial support of my research, great discussions, encouragement and invaluable advice. It was a great honor and privilege for me to work with him over the years under his supervision and mentorship.

Additonally, I would like to thank Prof. Qiang Li for being my second examiner. Thank you for giving me valuable feedback and for making the long journey from Chengdu to Ulm.

Furthermore, I want to thank Dr. Joachim Becker for giving me many helpful suggestions and assistance with the digital design and for a perfect digital design flow, making digital synthesis really just the press of a button.

Additionally, I would like to thank all my former colleagues. Jiazuo Chi has been an excellent office mate and friend over almost my entire time at the institute. We had great discussions on IC design and much, much more. I would like to thank my colleagues, co-authors and good friends, Patrick Vogelmann and Prof. Dr.-Ing. Jens Anders for all their help in design, implementation and measurement. Last but not least, I would also like to thank everyone taking part in our early morning coffee round, sharing numerous great on- and off-topic discussions.

Finally, I would like to thank my wife, Julia Haas and my whole family for their support and encouragement during all times of my Ph.D. studies. If it wasn't for them, this work would have not been possible.

Contents

List of Figures

List of Tables

Abbreviations

AAF	Anti-Aliasing Filter
ADC	Analog-to-Digital Converter
AP	Action Potential
ASIC	Application Specific Integrated Circuit
BMI	Brain Machine Interface
CB	Charge Balancing
CCS	Constant Current Stimulaton
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CNS	Central Nervous System
CQS	Constant Charge Stimulation
CSB	Chip Select Bit
CT	Continuous Time
CVS	Constant Voltage Stimulation
DAC	Digital-to-Analog Converter
DDU	Data Distribution Unit
DR	Dynamic Range
DT	Discrete Time

ECoG Electrocorticography

EEG Electroencephalography

ENoB Effective Number of Bits

ESD Electrostatic Discharge

FES Functional Electrical Stimulation

fMRI Functional Magnetic Resonance Imaging

fNIRS Functional Near-Infrared Spectroscopy

FSM Finite State Machine

GCU Global Control Unit

HV High Voltage

HV CMOS High Voltage CMOS

IC Integrated Circuit

IΔΣ-ADC incrementel ΔΣ ADC

IR-UWB Impulse Radio Ultra Wide Band

I-SD Incremental ΣΔ

LCU Local Control Unit

LDO Low Dropout Regulator

LFP Local Field Potential

LNA Low Noise Amplifier

LS Level Shifter

LSB Least Significant Bit

LV Low Voltage

MEA Micro Electrode Array

NEF Noise Efficiency Factor

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

PBS Phosphate Buffered Saline

RLP Root Locus Plot

SC Switched Capacitor

SDM ΣΔ Modulator

SEM Scanning Electron Microscope

S/H Sample-and-Hold

SNDR Signal-to-Noise-and-Distortion-Ratio

SNR Signal to Noise Ratio

SoA State-of-the-Art

SoC System on Chip

SPI Serial Peripheral Interface

TF Transfer Function

THD Total Harmonic Distortion

TIA Transimpedance Amplifier

UEA Utah Electrode Array

UWB Ultra Wide Band

Chapter 1

Introduction

Biomedical brain implants are of major interest within the research and therapy of neurological disorders, as implantable electrodes, that interface the brain below the dura, can provide much higher signal levels and spatial resolution compared to non-invasive Electroencephalography (EEG) techniques [19, 20]. Additionally, placing the electrodes closer to the interacting neurons does not only yield improved signal quality, but also allows to stimulate a reaction of the surrounding tissue with high spatial resolution, via Functional Electrical Stimulation (FES). This reaction is triggered by injecting charge into the nervous tissue, in order to depolarize a neuron and trigger an action potential. The ongoing trend in brain implants is towards systems that provide a fast growing number of independent, parallel recording and stimulation sites, together with wireless power and data transmission [21–24].

In research, the increasing number of channels allows a higher spatiotemporal resolution of the communication paths within the central nervous system. The combined stimulation/recording capabilities can provide a detailed image of the nervous reaction, which can be used to derive a mapping of the functional brain units [25] and lead to a deeper understanding of the working mechanisms. Even high resolution recording alone can be used to exactly locate the propagation of stimuli through the brain and track the complete path from the processing of a visual stimulation all the way to a reaction in the motor cortex [26]. Furthermore, high-resolution, bidirectional implants are not only applicable in brain research, but also provide a significant improvement in the therapy of neurological disorders, as they allow closed-loop stimulation devices. During closed-loop stimulation, the recorded nervous signals are used to trigger a stimulation, to adapt the stimulation parameters like waveform or intensity to the reaction of the nervous tissue, or a combination of both [23, 27–29]. Several studies have shown, that this improves the

stimulation efficacy and allows to adapt the stimulation process to the individual neural state of each patient.

By integrating more and more functionality onto a single System on Chip (SoC) the size, battery lifetime and functionality of neural implants could be improved over the last decades. This led to systems with 100 channels or more [21, 30, 31] and even a system with 1024 channels has been reported [32]. However, publications in the field of neurology show, that a pure increase in the amount of recording/stimulation sites is not the only way to go in order to improve therapeutic results. Besides the location of stimulation, many other parameters like stimulus waveform, stimulation duration and stimulation timing can severely influence the neural reaction [33–35]. The varying results from different experiments make it clear, that an integrated neural stimulator should offer maximum flexibility, in order to be adaptable to the neurological state of each individual patient.

A new obstacle, which arises through the growing channel count, is the increasing amount of data which must be transmitted from the implant to an external unit. With a bandwidth of the neural signals of approximately 10 kHz [3, 20], a sample resolution of 16 Bit and a channel count of 32 or more, a transmitter that is capable of transmitting several 10s of Mbit/s is required. This task becomes especially challenging with regard to the power budget and the limitations in antenna size, due to the small size of the implant.

In conclusion, this briefing shows that a versatile stimulator is needed, as it offers researchers maximum freedom in the design of neurological experiments and allows to adapt stimulation patterns to the individual needs of each patient. Additionally a highly integrated SoC is required in order to use the limited power and space in an implant to its full capacity. Therefore a fully integrated 32 channel, bidirectional neural interface has been developed in this thesis. The interface was implemented in a High Voltage CMOS (HV CMOS) technology, which allows the use of a High Voltage (HV) supply for stimulation, together with a Low Voltage (LV) supply for recording, thus increasing the stimulators voltage compliance, while maintaining a low noise recorder with low power and area consumption. During the design process three prototypes with increasing complexity were manufactured and evaluated and all results were combined into the final SoC. Additionally Ultra Wide Band (UWB) data telemetry was investigated, as it is reported to offer the best power efficiency for the required data rates and its high center frequency allow for small antenna dimensions.

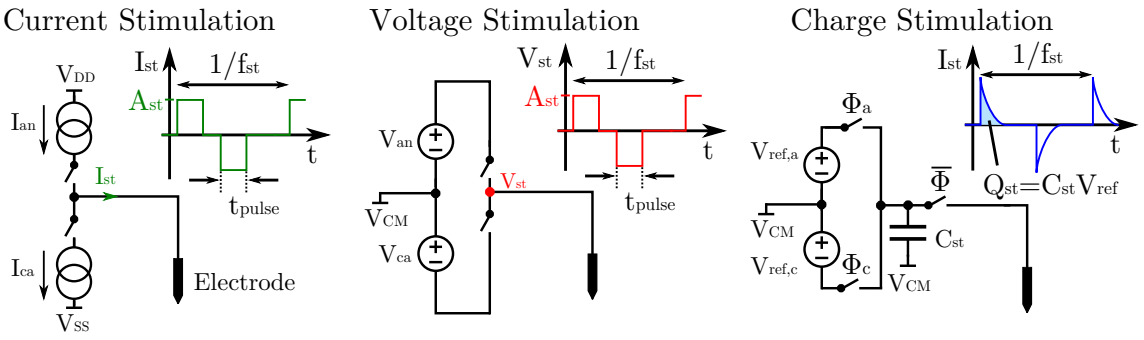


FIGURE 1.1: Different implementations of FES and their key parameters.

1.1 Motivation

Neurological disorders like epilepsy, impairments caused by stroke or Parkinson's disease are a common global health-care problem. Motor recovery after a stroke is a large application field, mainly of neural recording, as loss of functional movement after a stroke is the main cause of acquired adult disability in high-income countries [36]. In this case, Brain Machine Interfaces (BMIs) can be used to bypass damaged brain areas and restore lost body functions or control prosthetic devices [19]. The second big research field for FES is the suppression of seizures in epilepsy or tremor in Parkinson's disease [37–40].

Epilepsy is the most common, serious, neurological disease, affecting approximately 50 million people worldwide [38], Parkinson's disease is the most common neurodegenerative disease affecting 1 - 2 % of persons over the age of 60 years [39]. Although the symptoms of the majority of both patient groups can be efficiently treated with pharmacological medications, around one quarter of the epilepsy patients remain with drug-resistant epilepsy [38, 41] and approximately 50 % of patients with essential tremor, caused by Parkinson's disease, do not improve with pharmacological medications [39]. In this case, clinical experience over the last decades has clearly shown, that FES can be used to dramatically reduce the symptoms and significantly improve the patients quality of live.

In the open-loop, neural FES approach, voltage, current or charge pulses are applied to one or several electrodes with a constant amplitude, duration and repetition frequency, which must be preliminarily determined, based on empirical values. Figure 1.1 illustrates the three different stimulation types together with their characteristic values. These stimulation parameters must be adjusted by a person with adequate training during a programming session [39], average values, e.g. for voltage stimulation in tremor patients, are reported with amplitudes of 2.4 - 4.4 V, a frequency of 143 - 173 Hz and pulse widths around 100 µs [42]. However, studies showed that more complex stimulation waveforms, e.g. an exponential decrease, can provide more energy and charge efficient stimulation

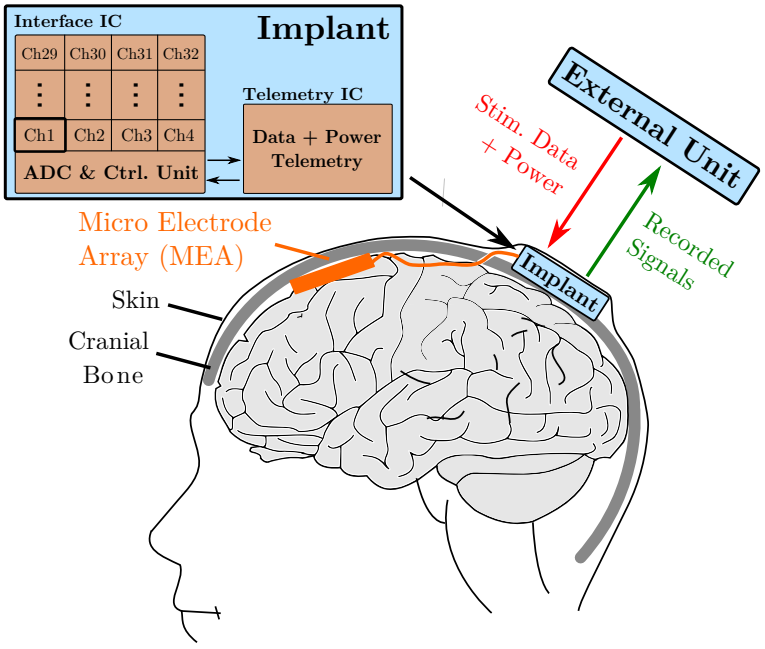


FIGURE 1.2: Conceptual neural modulator to stimulate and record the neural network of the human brain.

[33, 34, 43]. This allows to increase the battery lifetime of an implant and reduce the risk of tissue damage, as the amount of delivered charge can be reduced.

The next step to increase charge and power efficiency is to combine a neural recorder with a stimulation device and deliver on-demand stimulation pulses. This is done in closed-loop FES, where not only the timing but also the stimulation amplitude can be changed, based on the recorded signal, leading to a more efficient treatment, while offering less side effects than continuous stimulation [37, 38]. Figure 1.2 shows the concept of a closed-loop BMI. It consists of an implant, which contains the electronics for wireless data and power telemetry, as well as the neural recording/stimulation front-end. The interface between electronics and the nervous tissue is provided by a Micro Electrode Array (MEA) with several tens up to more than a hundred separate electrodes for stimulation and recording [44], [21, 45]. The example shows the system design intended in this thesis, where every channel in the interface Integrated Circuit (IC) contains a combined recorder and stimulator, to allow parallel recording and stimulation and a shared Analog-to-Digital Converter (ADC) is used to digitize the recorded signals. A digital on-chip control unit manages the stimulation timing and the communication to the telemetry unit, which provides a wireless data and power link to an external unit. Thereby no wired connections through the scalp are required, which minimizes the risk of infections and inflammations.

In the shown example, the raw, recorded data is streamed out to the external unit which has two major advantages. First, it allows to store all recorded data on a mass storage

device, which is especially important for researchers, as offline signal analysis can be performed. Second, the available computation power in an external unit is much higher compared to the implanted device, since the power budget is strictly limited by the heat flux of the implant. In order to limit its heating to less than 1 °C, the implanted device must not exceed a heat flux of 65 mW/cm^2, which sets, together with the limited space, the overall power budget [46, 47]. Therefore, complex and power hungry signal processing algorithms are put outside the body, were more area is available and more heat can be dissipated without tissue damages.

In order to estimate the required data rate in this scenario, the bandwidth of the expected signals that will be recorded can be analyzed. In extracellular neural recordings the signal can be spectrally separated into low frequency Local Field Potentials (LFPs) and high frequency Action Potentials (APs). LFPs are located between 0.5 - 200 Hz with amplitudes in the range of 5 µV to 5 mV, APs are located between 0.2 - 7.5 kHz with 5 - 10 times smaller amplitudes [48, 49]. This results in an overall bandwidth of 7.5 kHz for the neural signal, which requires a sampling rate of at least 15 kS/s to avoid aliasing. In order to ensure that the signal quality is not limited by the quantization error of the ADC a resolution of 16 bit is chosen in commercially available systems [50]. If we increase the sampling rate to 20 kS/s to account for non-ideal filtering of the recorded signal, the required data rate per channel R_{ch} can be calculated to:

$$R_{ch} = 20\,kS/s \cdot 16\,bit/S = 320\,kbit/s \tag{1.1}$$

Many recent publications about implantable data links use the Impulse Radio Ultra Wide Band (IR-UWB) technique, as it offers high data rates, combined with high power efficiency and a license free use. Modern Complementary Metal-Oxide-Semiconductor (CMOS) technologies allow to design power efficient implementation of transmitters that use the frequency band between 6 - 8.5 GHz, which can be combined with on-chip data encoding or even be included in a neural recorder SoC [51]. The reported transmitters provide data rates of up to 230 Mbit/s, which is enough to transmit the raw data of more than 100 channels, with a power consumption of less than 4 mW [52–54].

The main motivation of this thesis is to combine a neural recorder, a neural stimulator, the digital control logic required to control the stimulation process and a high resolution ADC on one chip, in order to allow extremely area and power efficient implants. A second goal is to extend the capabilities of the on-chip neural stimulators in order to allow arbitrary stimulation waveforms in current mode, as well as in voltage mode with one device. This would give researchers as well as clinicians a powerful tool with maximum

flexibility in the design of experiments and the possibility to adapt therapies to the needs of individual patients.

To achieve this goal, different stimulator and recorder architectures were considered during this research work, which are discussed within this thesis. A newly developed architecture is shown that combines recorder and stimulator, while providing voltage and current mode stimulation with minimal area and power overhead. Additionally an improved recorder architecture that offers on-chip, signal adaptive bandwidth tuning and bioimpedance estimation is presented. All presented solutions were verified with 5 prototypes, manufactured in a 180 nm HV CMOS technology.

1.2 Achievements and innovations of the research work

This section highlights the achieved findings of this work for biomedical modulators. Furthermore, the specific innovations for neural recording as well as for the neural stimulator are shortly presented.

The starting point of this thesis was a 32 channel neuromodulator design presented in [55], which featured 32 low noise recording front-ends. However, there was no on-chip stimulator included, but only 32 HV transmission gates were used to direct the stimulation current of an external stimulator to one of the working electrodes. Therefore, the first task in this thesis was to find a stimulator architecture, which allows to be combined on-chip with the existing neural recorder. In the first approach, a HV, biphasic, current mode stimulator was designed, in order to provide a large voltage compliance, which is required for small, high-impedance electrodes. During stimulation phases the recorder is protected from the potentially harmful voltage levels via HV switches. The combined, bidirectional front-end was realized in a 180 nm HV-CMOS technology and provides measured stimulation currents of up to $\pm 10.2\,\mathrm{mA}$ with an output compliance of $\pm 8\,\mathrm{V}$. Arbitrary stimulation waveforms were realized with a 5-bit current steering Digital-to-Analog Converter (DAC), whose Dynamic Range (DR) was increased to more than 50 dB by an additional output range selection. The recorder features a measured, input referred noise of $3.3\,\mu\mathrm{V_{rms}}$ in the LFP and the AP band [16].

In a second revision of the stimulator, its functionality was extended by a constant voltage stimulation mode. This was achieved by a semi-digital feedback loop, which controls the stimulation current in order to adjust the electrode potential to the desired stimulation voltage. This novel architecture allows for the first time to fully reuse the area consuming HV output stage of a current stimulator in order to achieve voltage mode stimulation. Therefore, a very high area and power efficiency is achieved, with an

area overhead of only 11 % for the bidirectional channel and less than 1 µW of additional power consumption [14].

The second task in the thesis focused on the recording of neural data and to make it more versatile for a broader variety of applications. Since not the entire bandwidth from 1 Hz to 7.5 kHz is of interest in every experiment, a tunable high-pass cut-off frequency was introduced to the Low Noise Amplifier (LNA). This allows a flexible trade-off between recorder bandwidth and noise performance, which makes the recorder more adaptable to the desired neural signal. Additionally, a 0 dB low gain mode was introduced, which can be used to estimate the bioimpedance of the used electrode in combination with the current mode stimulator. This increases patient safety, as electrode degradation and ripoff can be detected and the stimulation waveforms can be adjusted accordingly [13].

Both results, from the development of the stimulator and the revision of the recorder, resulted in the design of a 32 channel fully-integrated, bidirectional neural interface. It combines a high resolution incrementel $\Delta\Sigma$ ADC (I$\Delta\Sigma$-ADC), the digital control logic for stimulation and recording and 32 bidirectional neural front-ends. This allows to reduce the number of components that are required for a neural implant, which tremendously reduces the size and power consumption.

Therefore, the results in this thesis can be used to improve the State-of-the-Art (SoA) in implantable neuromodulators, not only by decreasing their size and power consumption: Additionally the extended functionality allows more patient safety, increases the freedom in the design of experiments in research and makes the implant more adaptable to the individual needs of patients. This can help neurologists in future work to further extend the knowledge about function mechanisms in the central nervous system and even provide new therapeutic measures for neurological disorders.

In the last part of this work, the already mentioned wireless data link, which is needed to stream the data to an external unit, was investigated as an outlook for further developments. This led to a first, successful design and testing of a miniaturized UWB transmitter, which is capable of delivering data rates up to 100 Mbit/s. Its small form factor, power consumption and the measured robustness to environmental change make it very promising for implantable, transcutaneous high-speed data transmission [18].

1.3 Outline of the thesis

This thesis is organized in 6 chapters. Chapter 1 gives a general introduction into the topic of neuromodulation and highlights the work that was done in this thesis. The second chapter explains the signaling mechanisms in the central nervous system between

the fundamental, functional units, the neurons. This is used to derive the nature of the observable, neural signals, how these can be measured using integrated circuits and finally how brain activity can be electrically modulated. After deriving these fundamentals, Chapter 3 shows the neural recorder design, which was developed during this work, explains novelties that were realized and how they improve patient safety, as well as signal quality. In Chapter 4, the integrated, high voltage, neural stimulator is shown and how the sensitive neural recorder can be protected from potentially harmful stimulation events. A novel, semi-digital feedback architecture is presented, which allows reconfiguration between current and voltage mode stimulation, achieving outstanding area and power efficiency. Thereafter, the implemented 32 channel neuromodulator is presented in Chapter 5, explaining in detail the utilized on-chip, digital waveform synthesis, on-chip analog-to-digital conversion and the supporting analog circuitry. Finally the thesis is concluded in Chapter 6 and an outlook on possible, future work in the field is given.

Chapter 2

Background and State of the Art

In this chapter, the principal structure of a neuron and its communication mechanisms are explained. Followed by this, the nature of electrical, neural signals will be explained, which can be derived from the fundamental working principle of a neuron. It is important to understand the working mechanisms that lay behind these signals, in order to successfully interface and record them, as well as to electrically stimulate a desired neurological response. The second section of this chapter describes how nervous tissue can be interfaced with electronics and what the resulting possibilities for signal recording and neural stimulation are. Additionally, an overview of neurological disorders that can be treated with electrical stimulation of the Central Nervous System (CNS) is given. To close the chapter, the SoA in circuits used for neural interfaces is reviewed and a selection of architectures is compared against each other.

2.1 Central nervous system

The CNS consists of the spinal chord and the main part of the whole nervous system, the brain. It consists of approximately 10^{12} neurons [56], which communicate amongst each other and thereby allow us to perceive our environment and control our body. Understanding the complex working mechanisms that underly the overall functioning has been a major area of research, on a cellular level as well as on a more macroscopic, anatomical level.

2.1.1 Anatomy and function of the neuron

Figure 2.1 shows the anatomy of a neuron, the fundamental functioning unit of the nervous system, and its connection to a second neuron. Starting on the left side, the

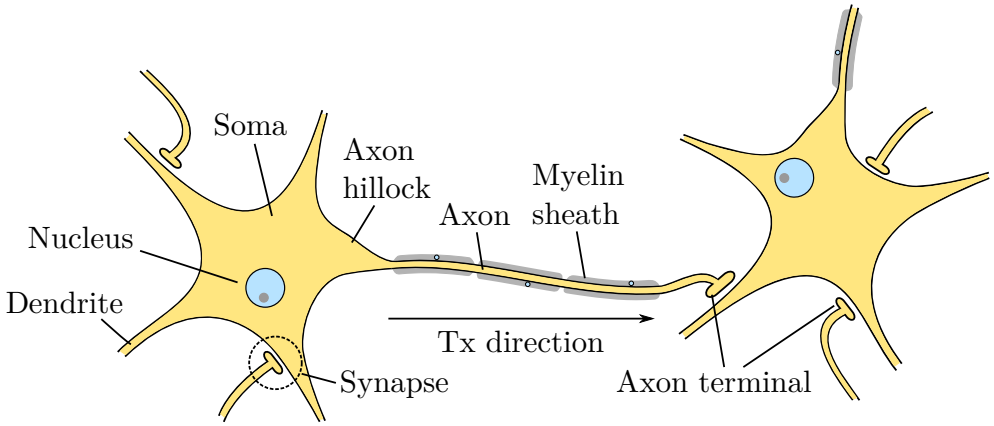


FIGURE 2.1: Anatomy of a multipolar neuron.

neuron consists of the cell body (*soma*), to which two different types of extensions are connected:

- *Dendrites* are the receiving part of the neuron, where the synapses of other neurons end. A neuron can have several dendrites, with complex branching.
- The *Axon* is the transmitting part of the neuron and propagates signals to other neurons or other types of cells (e.g. muscles). Every neuron has only one axon, which is usually enclosed by a myelin sheath [57].

The dendrite is the part of the neuron that receives the input from one or several previous neurons via the synapses. If a signal arrives at the axon terminal, a neurotransmitter is released into the synaptic cleft, where it propagates to the dendrite of the next neuron. Depending on the type of neurotransmitter, this excites signal propagation by depolarization or inhibits signal propagation by hyper polarization of the adjacent neurons membrane voltage. All incoming signals are integrated at the axon hillock, where an all-or-nothing decision is made, meaning if the membrane voltage stays below a certain threshold no signal is propagated at all. However, if it reaches the threshold a new action potential (AP) is generated at the axon hillock and propagates along the axon to the next axon terminal.

Figure 2.2 illustrates the propagation of an AP along the axon. For simplicity only Na^+ and K^+ ions are shown, as these are the ones responsible for AP propagation. In the absence of an excitation, a voltage difference between the intracellular and the extracellular potential of about -70 mV is observable, the so called resting potential (Figure 2.2 (1)). This is maintained by Na^+, K^+ and Cl^- channels as well as Na^+ and K^+ ion-pumps. If the cell is depolarized above the marked threshold value, e.g. by synaptic excitation or by an AP event along the axon, the voltage-gated Na^+ channels open (Figure 2.2 (2)), allowing more Na^+ ions to flow into the neuron along their concentration gradient. This

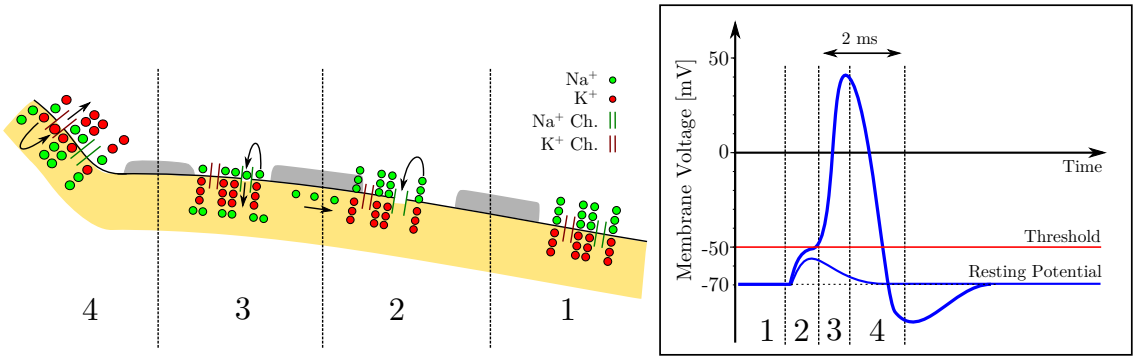


FIGURE 2.2: Propagation of an AP along a myelinated axon and the resulting membrane voltage over time, based on [1].

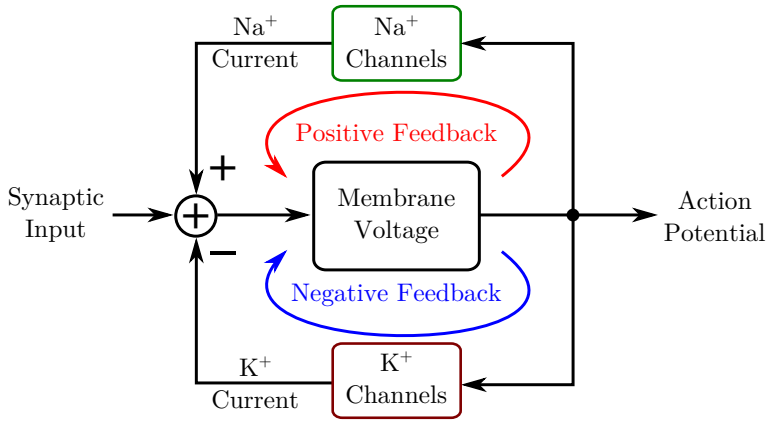


FIGURE 2.3: Feedback mechanisms in the propagation of APs, based on [2].

current leads to further depolarization, which opens even more Na^+ channels, until a maximum membrane voltage of approximately 40 mV is reached (Figure 2.2 (3)), where the Na^+ channels close again. The K^+ channels have a delayed reaction, which leads to a dominant K^+ current at the peak of the AP, causing the membrane voltage to drop back to its resting potential, after an observable undershoot, called hyper polarization [2]. After an AP event the initial concentration levels are gradually restored by sodium-potassium-pumps.

The described process can be modeled by two feedback loops as illustrated in Figure 2.3. If a synaptic input depolarizes the membrane voltage above the threshold value, the positive, sodium feedback loop amplifies the received signal to the full AP level. After that, the negative, potassium feedback loop restores the resting potential and brings the neuron back to its initial state. This signal triggering can be used to stimulate nerve cells by electrical depolarization, as it will be explained in section 2.4.

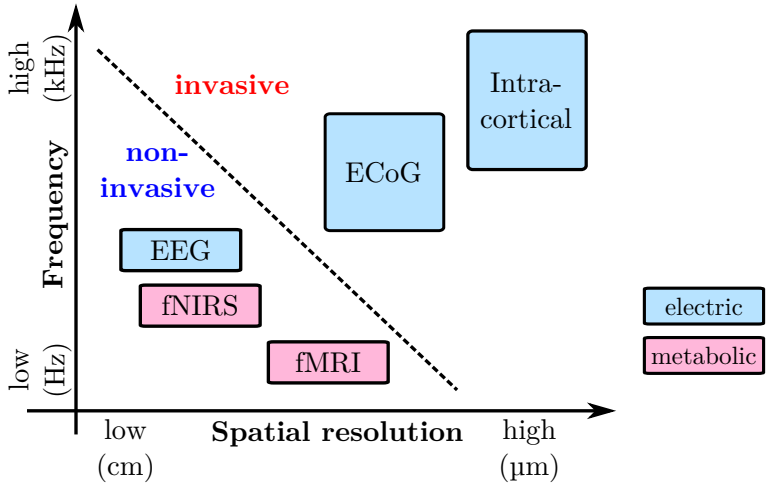


FIGURE 2.4: Comparison of different recording approaches regarding spatial and temporal resolution, derived from [3].

2.1.2 Observable neural signals

In the previous section the general propagation mechanism of neural signals was described. Many approaches exist to record this communication between neurons, which make use of different measurands that indicate neural activity. In the chemical domain, direct measurement of neurotransmitter concentration is applied, mainly in in-vitro experiments, where it can be used for early drug screening and drug discovery [58]. Another method is Functional Magnetic Resonance Imaging (fMRI) and Functional Near-Infrared Spectroscopy (fNIRS), where haemodynamic changes are measured to locate enhanced neural activity and thereby study sensory processing, control of action or draw conclusions about neural mechanisms [59]. Figure 2.4 compares all recording approaches which can be used for BMIs, regarding invasiveness and spatiotemporal resolution [3].

It is clear that a trade-off between spatiotemporal resolution and invasiveness has to be found for BMIs. Most commonly, implantable systems that use Electrocorticography (ECoG) or intracortical electrodes are chosen, since they offer the highest spatiotemporal resolution and can be recorded with highly integrated, area and power efficient devices. Figure 2.5 shows the unfiltered, recorded extracellular potential from the prefrontal cortex of a sleeping rat [4, 5]. The signal can be spectrally divided into two parts, in the lower frequency band located between $f_{LFP} = 0.5 \text{ - } 200\,\text{Hz}$ are the local-field-potentials (LFP) and in the higher frequency band located between $f_{AP} = 200\,\text{Hz} \text{ - } 7.5\,\text{kHz}$ are the action potentials (AP).

APs or spikes are caused by the rapid change in the extracellular potential when an excitation is propagated along an axon, as described in subsection 2.1.1. Therefore, the same characteristic waveform, which was previously explained with the two feedback loops, can be observed as shown in the zoom in Figure 2.5. However, the maximum

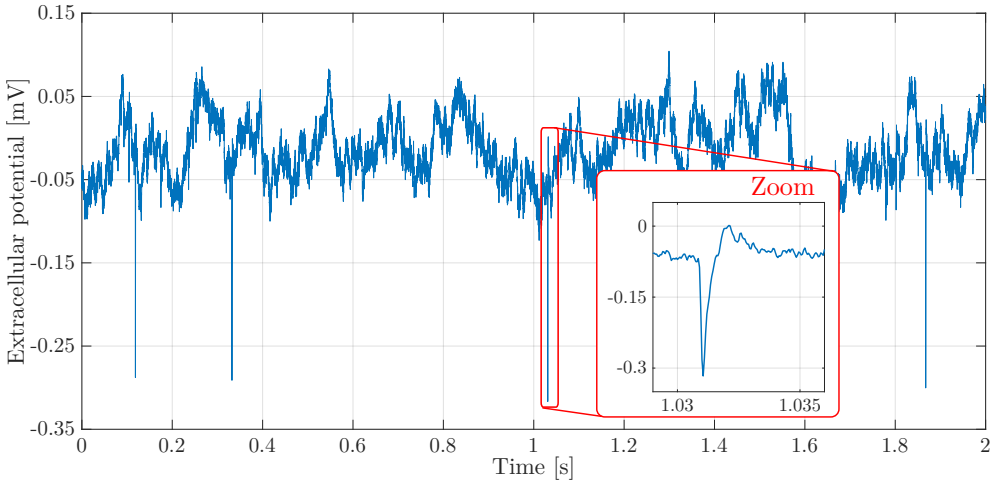
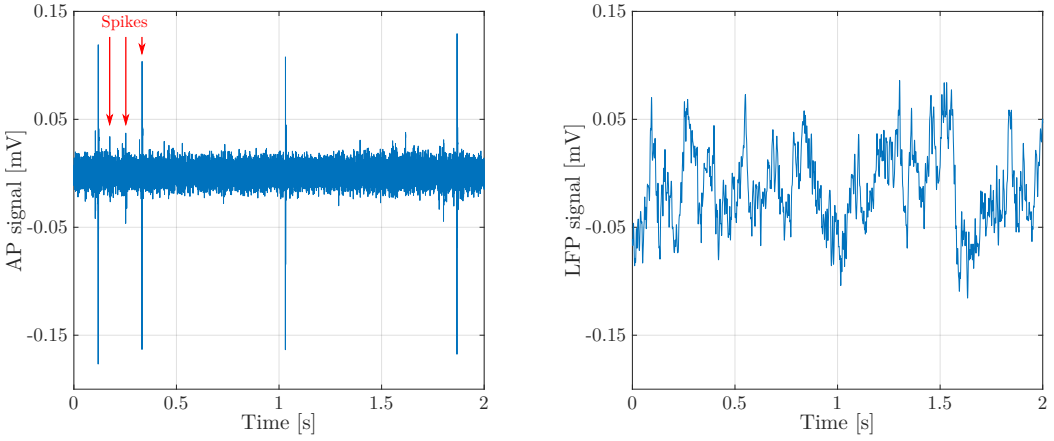


FIGURE 2.5: Recorded, extracellular potential of a sleeping rat, showing LFP and AP signal parts; Signals from [4, 5].



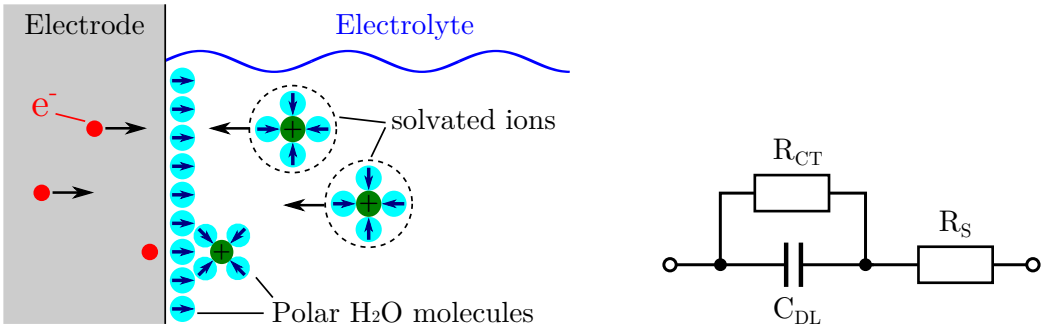
(a) High-pass filtered AP signal ($f_{HP} = 100\,Hz$)

(b) Low-pass filtered LFP signal ($f_{LP} = 100\,Hz$)

FIGURE 2.6: Neural signal filtered with 6th order Butterworth filter; Signal from: [5].

amplitude is much smaller than the amplitude shown in Figure 2.2, as only the change in extracellular potential is measured and not the actual membrane voltage. Additionally, the signal is damped because of the distance between the recording electrode and the axon, which results in observable signal amplitudes in the order of 100 µV. The low frequent LFPs are caused by synchronous activity of many neurons in a certain region of the brain. As these neurons are too far away from the recording electrode their individual spikes can't be resolved, however the "crowd noise" of their increased activity produces a large signal which can be easily observed [49].

The waveforms shown in Figure 2.6 have been extracted using a low-pass and a high-pass 6th order Butterworth filter, each with a cut-off frequency of 100 Hz to separate the LFP and the AP signal. This high-order filtering accentuates the rapid rising edges of the spikes, which results in filter artifacts that look like additional, positive spikes.



(a) Formation of the double layer capacitor.

(b) Randles cell electrode model.

FIGURE 2.7: Non-Faradic reactions at the electrode-electrolyte interface, based on [6].

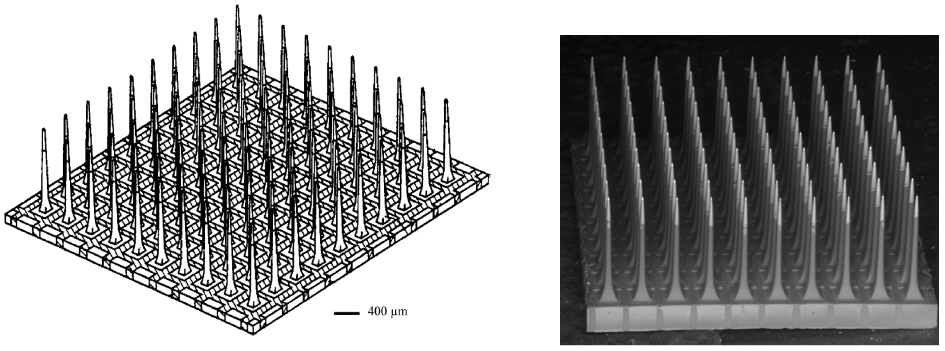
Furthermore, the filtered signal shows more spikes with different amplitudes and waveforms. This is the case, because usually more than one neuron is close enough to the recording electrode, such that their spikes can be resolved. The filtered AP signal even allows to distinguish between different neurons by applying spike sorting algorithms, as every neuron has its individual spike waveform, based on its physiological condition [60].

2.2 Interfacing of nervous tissue

While brief, intracellular recordings are possible using individually guided microelectrodes [49], the majority of interfaces between electronics and nervous tissue is provided by electrodes that record the extracellular potential. These electrodes consist of electrically conductive material, usually some kind of noble metal, which is in direct contact with the brain fluid, but can differ in form, size and the used materials [61]. In the following the signal transporting mechanisms and the resulting electrical model is explained and how the electrode properties influence the parameters of the electrical model.

2.2.1 Electrode-electrolyte interface

If metal electrodes are used, three different mechanisms exist that transfer the electron based signal conduction within the metal into an ion based signal conduction in the electrolyte: capacitive charge transfer, electrochemical reactions and redox reactions. Figure 2.7(a) shows the reversible, capacitive mechanism, which is dominant at small voltages over the phase boundary and not associated with any electrochemical reaction. In principle, a capacitor is formed by the electrons in the metal, a first isolation layer of water molecules that are adsorbed at the metal surface, a second layer of water molecules around the solvated ions and the ions itself as the opposite charge carriers [6]. This process is mainly responsible for generating the recordable neural signal and



(a) Schematic of the UEA. (b) SEM image of the UEA.

FIGURE 2.8: The 10 x 10 Utah electrode array (UEA) [7].

the desired method for stimulation, as for higher voltages, irreversible, electrochemical reactions start. These reactions occur, when charges cross the phase boundary and lead to changes in the chemical composition of the electrode-tissue interface, which can produce cytotoxic substances. Therefore, electrode voltages must be kept within certain, material dependent limits, to ensure patient safety.

If an electrode is operated within its reversible limits, the electrode-electrolyte interface can be modeled with the Randles cell electrode model shown in Figure 2.7(b). It consists of the double layer capacitor C_{DL}, which is caused by the aforementioned non-Faradic reactions, the solution resistance R_S that models the current flow in the solution and the reaction, or charge transfer resistor R_{CT}, which models the undesired, electro-chemical reactions [62]. In order to provide a good electrode for stimulation and recording, a large C_{DL} together with a small R_S is required. This allows on the one hand side to transfer a certain current density, which is required to achieve a stimulation effect, without large electrode voltages and on the other hand side a good Signal to Noise Ratio (SNR) during recording, as the resulting electrode impedance is equivalent to the signals source impedance [63].

2.2.2 Implantable electrodes

Implantable electrodes for neural recording and stimulation come in many different shapes, materials and with varying mechanical properties. One possible characteristic which can be used to group the existing MEAs is between intracortical electrodes, where the electrodes penetrate the brain tissue and ECoG electrodes that record signals from the cortical surface. While intracortical MEAs offer high spatial resolution from high impedance electrodes, ECoG offers larger electrodes with lower electrode impedance and is likely to have greater long-term stability and patient safety [64].

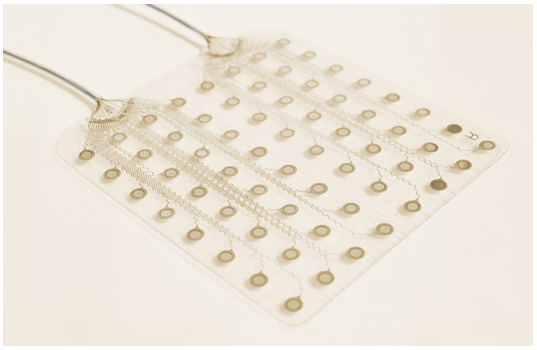


FIGURE 2.9: Commercially available 8x8 ECoG electrode array (CorTEC - AirRay) [8].

The most prominent example of an intracortical MEA is the commercially available Utah Electrode Array (UEA) that is shown in Figure 2.8. It consists of 100 electrodes, with a length of 1.5 mm and a spacing of 400 µm that are fabricated on a silicon substrate. This allows wafer scale fabrication with adapted processes from CMOS manufacturing, which leads to comparably low costs and low variances in the electrode parameters. The well established, silicon based processing allows the manufacturing of the smallest electrodes available, which results in a very high spatial and temporal resolution [7]. Another advantage of penetrating electrodes is that they provide maximum signal amplitudes for AP recording, as the distance between electrode and neuron is minimized. However, this method comes with the disadvantage that the brain tissue is damaged during the insertion of the array into the brain. Although studies showed that useful signals can be acquired even 9 months after implantation, still concerns exist about longterm tissue reactions, e.g. caused by micro movement and encapsulation [65]. Another major drawback lies in the stimulation capabilities of these electrodes, which comes from the unavoidable trade-off between charge capacitance and electrode size. The electrodes double layer capacitance, which determines its charge capacity and thereby the stimulation capability, can be calculated as follows.

$$C_{DL} = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d_H} \tag{2.1}$$

This is a first order approximation of C_{DL} as a parallel plate capacitor, where A is the effective area of the electrode and d_H is the thickness of the water layer between the ions and the electrode [6]. Due to their small, physical size, the shown electrodes have only a comparably small C_{DL}, thus offering only limited stimulation capabilities.

A different approach is the use of planar electrodes on a flexible substrate, e.g. silicone rubber that are either placed directly on the brain tissue or very close to it on the dura. Compared to the previously described intracortical implantation, this method

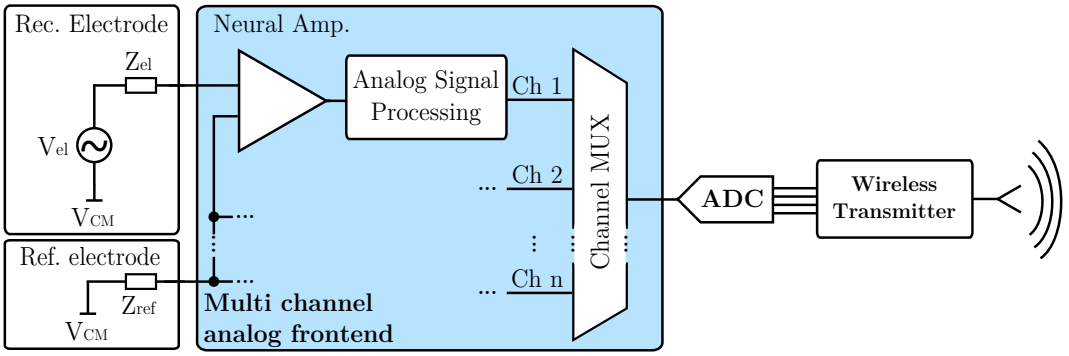


FIGURE 2.10: System level diagram of a multi channel neural recorder.

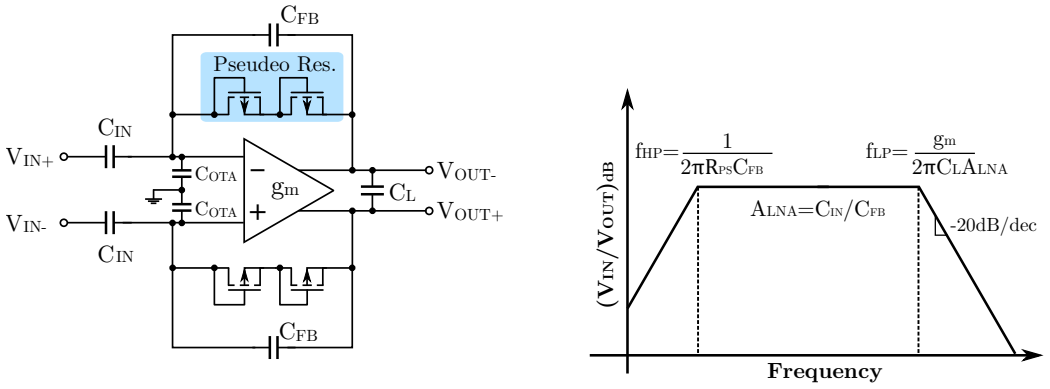
is less invasive, as it does not mechanically damage the tissue during implantation. Additionally, the increased electrode size provides lower electrode impedance and higher charge capacities, which allows for higher stimulation intensities. However, the drawback of this technique is that spatial resolution is lost because of the increased minimum electrode size, which is manufacturable with this technique. Additionally, the neural signal is spread due to the further distance of the electrodes to the neurons, resulting in a further loss of spatial resolution. A second disadvantage is that the maximum number of electrodes per area is lower [3], due to the increased electrode size.

2.3 Integrated recorders for implantable BMIs

As shown in the previous section, many different approaches are used to provide interfaces between neural tissue and electronics. As this thesis is focused on ICs for implantable BMIs, an overview of the SoA in ICs for recording of ECoG and intracortical signals is given in this section, followed by stimulation ICs and bidirectional interfaces in section 2.4.

Extracellular neural signals impose several challenges to an integrated recorder due to the high impedance of the electrode, the small signal amplitudes and DC voltages in the range of tens of mV that occur at the electrode-electrolyte interface. Figure 2.10 shows a typical multi-channel recorder front-end, where each channel has its own neural amplifier, which is the most critical stage in the design due to the following key parameters [49].

- *Input impedance*: Due to the high electrode impedance the first stage needs to provide a large input impedance to avoid excessive loading of the signal source.
- *DC suppression*: DC offsets from the electrode-electrolyte interface must be suppressed to avoid amplifier saturation.



(a) Schematic of the conventional neural amplifier.

(b) Transfer function of the neural amplifier.

FIGURE 2.11: Capacitive coupled neural amplifier with pseudo-resistor feedback [9].

- *Noise*: Since the amplifiers input referred noise is directly added to the signal, it must provide an integrated noise in the µV range to resolve AP signals.
- *Dynamic range*: The dynamic range muist be large enough to resolve spikes and LFPs (10 µV to 2 mV) at the same time.
- *Gain*: Sufficient gain must be provided to alleviate noise requirements on the following stages.
- *Recording bandwidth*: In order to record LFPs and APs a bandwidth of $f_{min} \leq 1$ Hz to $f_{max} \geq 5$ kHz is required.

If the neural amplifier provides a low impedance output and eliminates the DC offset, the input impedance and DC suppression issue is resolved in this stage. Additionally, Friis formula shows that the noise of the following stages will be suppressed by the gain of the neural amplifier. These points make it obvious that the first stage is the most challenging element, but reduces requirements on all following stages.

2.3.1 Conventional architecture

In the conventional architecture, MOS based pseudo resistors are used to overcome the area limited resistance of integrated feedback resistors which was first published in a photo receptor architecture [66]. In Figure 2.11(a) the schematic of the adaption to a fully differential, AC coupled, neural amplifier is shown [67]. It uses AC coupling over the input capacitors C_{IN} in order to block DC offsets from the electrode and two pMOS diodes which act as pseudo resistors in the feedback, to set the input common mode of the Operational Transconductance Amplifier (OTA) and to generate a high-pass corner frequency in the sub-Hertz range.

Figure 2.11(b) shows the bandpass transfer function of the amplifier. The passband gain $A_{LNA} = \frac{C_{IN}}{C_{FB}}$ is determined by the ratio of the input and the feedback capacitor which allows a well defined gain in a CMOS application, since capacitor mismatch can be designed to be in the sub-percent range. In the feedback path, C_{FB} and the pMOS pseudo resistor define the high-pass cutoff frequency $f_{HP} = \frac{1}{2\pi R_{PS} C_{FB}}$, where R_{PS} is the small signal resistance of the pseudo resistor. The innovation in this design was the use of the pseudo resistor which allows an area efficient CMOS implementation, by realizing huge on-chip resistors. If the absolute voltage over the pseudo resistor stays small enough to keep the MOS transistor and the intrinsic bipolar transistor off, R_{PS} can reach values of several TΩs [67]. This allows to choose C_{FB} in the range of hundreds of fF to achieve a high-pass corner frequency below 1 Hz which can not be realized with conventional integrated RC elements, since the required silicon area would exceed the available area budget.

In the described architecture, the input capacitor C_{IN} is usually the dominating area consumer. To achieve the desired gain, it must be sized A_{LNA}-times bigger than C_{FB} which itself is limited in minimum size by technology constraints and the desired high-pass frequency. Additionally, C_{IN} must not be chosen arbitrary small, as a capacitive voltage divider between the parasitic input capacitor C_{OTA} of the OTA and C_{IN} lead to a damping of the neural signal, thus reducing the SNR. According to [67] the input referred noise of the neural amplifier $\overline{v_{n,LNA}^2}$ can be derived from the OTA input referred noise $\overline{v_{n,OTA}^2}$ as follows:

$$\overline{v_{n,LNA}^2} = \left(\frac{C_{IN} + C_{FB} + C_{OTA}}{C_{IN}} \right)^2 \cdot \overline{v_{n,OTA}^2} \tag{2.2}$$

This shows the noise penalty factor which increases with the parasitic input capacitor. However, due to the low frequency band of the LFP signals, the OTA needs to provide a low 1/f-noise corner frequency which can only be achieved by increasing the gate area of the input devices. Therefore, good 1/f-noise performance comes with an increase of the parasitic input capacitor C_{OTA} in this architecture, requiring again for larger input and feedback capacitors. This results in a fundamental trade-off between integrated noise in the LFP band and circuit area which limits the performance of this architecture.

Another disadvantage of this architecture is that the lower cut-off frequency is only poorly designed during design time, as the absolute value changes with process- and temperature variations. A linearized approximation of the pseudo resistor value around its operating point at $V_{DS} = 0$, can be calculated using the EKV model [68]:

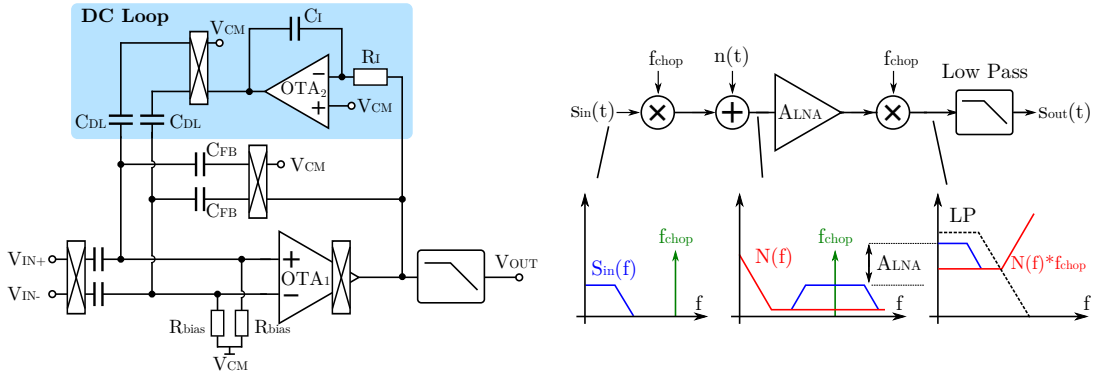
$$R_{PS}\Big|_{V_{DS}=0} = \frac{U_T}{I_{D0}} \tag{2.3}$$

Where U_T is the thermal voltage and I_{D0} the transistor dependent, residual channel current. I_{D0} can be calculated from the subthreshold slope n, the gate oxide capacitance per unit area C_{ox}, the transistors width W and length L and the pMOS threshold V_{T0} as followed.

$$I_{D0} = 2n\mu C_{ox}\frac{W}{L}U_T^2 e^{\frac{-V_{T0}}{nU_T}} \tag{2.4}$$

Although Equation 2.4 shows that the resistance can be designed by the transistors geometry, it also reveals the exponential dependency of R_{PS} on the process dependent threshold voltage. Since the neural recorder is usually operated in the body, the temperature dependency can be neglected, as excessive heating and cooling of the implant is not expected.

2.3.2 Chopper stabilized architecture



(a) Chopper stabilized neural amplifier, derived from [69].

(b) Working principle of chopper stabilization.

FIGURE 2.12: Chopped neural amplifier.

As described in the previous chapter, 1/f-noise imposes a fundamental trade-off between area and noise performance of the conventional neural amplifier architecture. To overcome this limitation, chopper stabilization was introduced in the design of neural amplifiers. Figure 2.12(b) illustrates how chopper stabilization can be used to reduce the in-band power of 1/f-noise.

In an ideal case, the input signal is up-modulated by multiplying it with a sinusoidal signal with the chopping frequency f_{chop}. This results in a shift in the frequency domain,

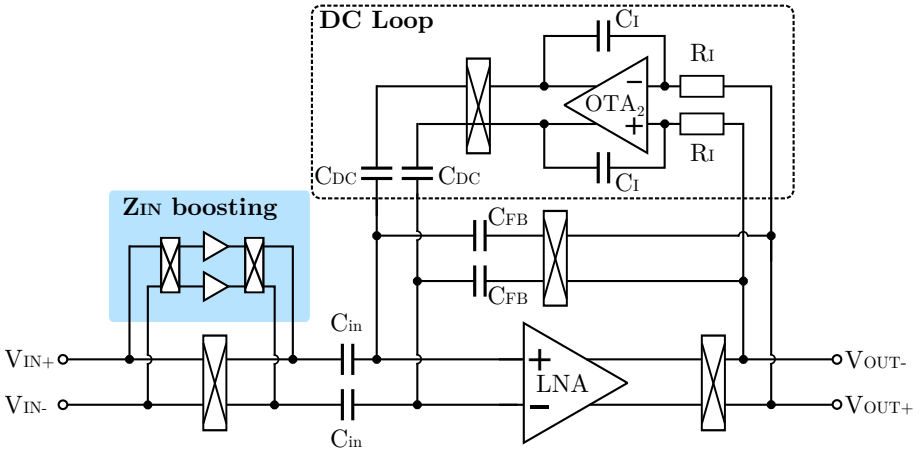


FIGURE 2.13: Simplified schematic of chopper stabilized neural amplifier with input impedance boosting, based on [10].

which separates the signal from the low-frequent, input referred 1/f-noise n(t) which is added by the amplifier. After amplification, the resulting signal is multiplied again, with the same sinusoidal, which shifts the signal back down to its original frequency range, while shifting the 1/f-noise to the chopping frequency (c.f. Figure 2.12(b)). Therefore, the undesired noise can be filtered out by a low pass filter, which results in an overall increase of the SNR, which is equivalent to a decreased input referred noise.

When looking into the SoA, many chopper stabilized architectures can be found [10, 69–71] that successfully demonstrate the 1/f-noise reduction, which allows integrated noise levels of $< 1\,\mu V_{rms}$ in the LFP band. Although this approach yields the lowest noise level, it comes with two major disadvantages, compared to the conventional architecture. The first disadvantage is that the chopped amplifier requires an increased bandwidth, as it must provide sufficient gain at the modulation frequency. This results in a higher power consumption for the same load capacity compared to an un-chopped amplifier.

The second issue that comes with input chopping, is the reduction of the amplifiers input impedance. Fig. 2.13 shows the simplified schematic of a chopped neural amplifier with input impedance boosting [10]. The up-modulation is performed before the input capacitors C_{in}, which is necessary for a fully integrated design. Chopping after the input capacitors would decrease the input impedance of the OTA and therefore require large off-chip capacitors as input devices to provide sufficient input signal. Without the input impedance boosting, this results in the following input impedances Z_{Conv} for the conventional architecture and Z_{Chop} for the chopped amplifier.

$$Z_{Chop} = \frac{1}{2\pi f_{Chop} C_{in}} \qquad Z_{Conv} = \frac{1}{2\pi f_{Max} C_{in}} \tag{2.5}$$

Where f_{Chop} is the chopping frequency and f_{Max} is the maximum signal frequency of the neural signal. Usually f_{Chop} is chosen around 10 times larger than the maximum input frequency, which yields an approximate chopping frequency of 100 kHz if LFP and AP signals are recorded. This high chopping frequency pushes the up-modulated noise and the chopping artifacts far enough away from the signal band to alleviate the adjacent filtering. However, the resulting input impedance is more than 10 x smaller, compared to the conventional architecture, resulting in a significant loading of the working electrode.

To improve the input impedance, impedance boosting can be applied as shown in Fig. 2.13 [10]. However, the achievable input impedance is still lower compared to the conventional architecture, as the impedance boosting buffers must be chopped as well to eliminate the 1/f-noise contribution of the buffering amplifiers. Additionally, the remaining noise of the impedance boosting stage adds directly to the input referred noise and the complexity of the architecture increases tremendously, requiring additional power and chip area.

2.4 Integrated neural stimulators

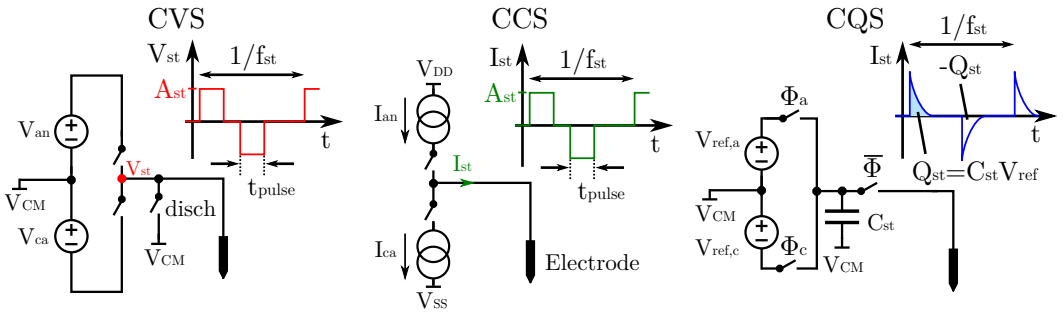


FIGURE 2.14: Block diagram of a constant voltage (CVS), constant current (CCS) and constant charge (CQS) stimulation.

Integrated neural stimulators are used to inject a controlled amount of charge into the previously described electrode-tissue-interface or to actively drive the electrode to a desired potential. Thereby, the extracellular potential can be modulated, which is used to depolarize the membrane voltage and thereby trigger spikes at the desired neurons. Depending on their working principle, SoA neural stimulators can mainly be divided into three categories: constant voltage, constant current and constant charge stimulators.

Constant Voltage Stimulation (CVS) is the classical stimulation form which requires the least circuitry. As depicted in Fig. 2.14, it can be simply realized by two stimulation switches, for cathodic and anodic stimulation phase that connect the electrode to a voltage source, e.g. realized by an implanted battery. The advantages of this method are that it offers a very high power efficiency, since the only power losses are caused

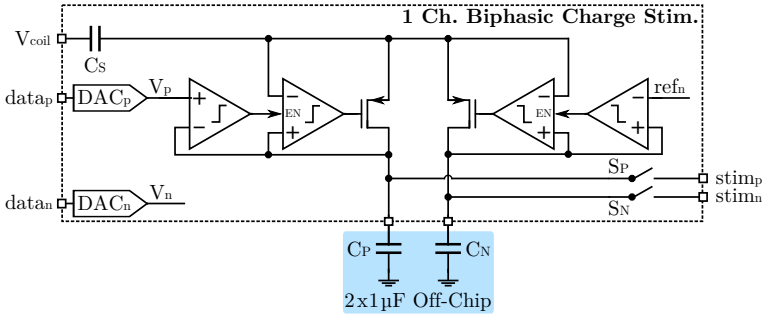


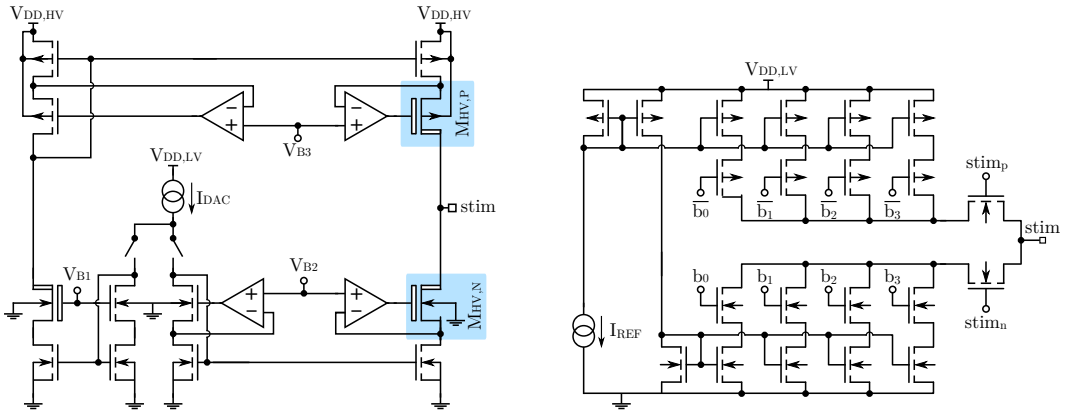
FIGURE 2.15: Single channel of the inductively powered CQS presented in [11].

by the on-resistance of the stimulation switches. Furthermore, vast experience with CVS exists among neurologists, since the first available stimulators for clinical trial implemented it, making it still the method of choice for many studies. Despite these advantages, the approach comes with two main drawbacks that directly effect the patient safety, which must always be the main concern. First, the peak stimulation current is uncontrolled and only dependent on the unknown electrode impedance. Second, the amount of charge which is delivered per stimulation pulse is unknown as well, as it also depends on the electrode impedance. Although the illustrated discharge switch can be used to eliminate excessive charge, this is still an issue, since the required discharge duration is unknown and discharging of excessive charge could trigger an undesired, second stimulation response.

Rarely implemented, constant charge stimulators solve this shortcoming by applying a programmable amount of charge to the working electrode, which is usually achieved by using switched capacitor (SC) stimulation circuits. If a biphasic stimulation pattern is used, two equal charge pulses of opposite polarization cancel each other, leaving no remaining net charge on the electrode as it is illustrated in Fig. 2.14.

An example for a Constant Charge Stimulation (CQS) that was presented in [11], is shown in a simplified version in Fig. 2.15. It consists of a high efficiency, capacitor charger that charges a pair of external positive/negative stimulation capacitors $C_{P/N}$ from the sinusoidal voltage V_{coil}, which is provided by an inductive link. The stimulation intensity can be controlled over two reference DACs, which set the voltage $V_{P/N}$ to which the external capacitors are charged, resulting in a stimulation charge $Q_{P/N} = C_{P/N} \cdot V_{P/N}$. After the charging phase, a stimulation is performed by sequentially discharging the capacitors over the switches $S_{P/N}$ into the electrode [11].

The advantage of this technique is that it offers a charge controlled stimulation mechanism with a very high power efficiency. However, its main disadvantage is that it requires large stimulation capacitors, which cannot be realized on-chip. This makes it hard to realize this approach for more than a few parallel stimulation channels.



(a) HV current stimulator derived from [73].

(b) LV current stimulator derived from [72].

FIGURE 2.16: HV/LV CCS with current steering DACs.

2.4.1 Constant current stimulators

In Constant Current Stimulaton (CCS), a current waveform is used as stimulation signal. Together with precise timing, this method ensures just like CQS that a well-defined amount of charge is applied to the nervous tissue, producing the desired stimulation effect. Because of the good control over the applied charge and the well defined peak currents, this method yields the highest patient safety, making it the method of choice for integrated stimulators. Many different designs have been reported, with maximum stimulation currents of several 100 µA [32] up to more than 10 mA [55] and voltage compliances ranging from 1 V [72] up to tens of Volts [73]. The large variance in the stimulation current arises from the many different use cases, as e.g. large, planar electrodes for ECoG implantation require currents of several mA, whereas tiny intracortical electrodes can only handle currents in the µA range.

All current stimulators have in common that a large voltage compliance is necessary, since the electrode impedance can have large variations due to aging or tissue changes and the stimulation current is only well defined within the compliance limits. The aforementioned variations yield however a trade-off between area and power efficiency on the one hand side and high voltage compliance on the other side. To illustrate this trade-off, two exemplary stimulation output stages are shown in Fig. 2.16. Although the left design minimizes the use of bulky HV devices by putting the current steering DAC I_{DAC} into the LV domain and shielding the mirroring devices, HV output transistors cannot be avoided to withstand the 20 V supply level. Additionally, these devices must be capable of driving the maximum stimulation current, which makes the highlighted, cascoding transistors $M_{HV,P/N}$ the main area consumer. Compared to that, no HV devices are necessary in the right design, since only a standard CMOS supply level

of 1.8 V is used. This results in a much smaller active area, but mostly insufficient compliance for large electrode impedances.

The power P_{stim} dissipated within the stimulator is usually dominated by the loss in its output branch, since it drives the highest current I_{stim} from the highest supply $V_{DD,stim}$ and can in general be calculated for a stimulation event of time T as follows.

$$P_{stim} = \frac{1}{T} \int_0^T \left(V_{DD,stim}(t) - V_{el}(t)\right) I_{stim}(t) dt \tag{2.6}$$

For a rectangular stimulation pulse of duration T_s on a Randles cell electrode model the resulting dissipated power in the stimulation circuit calculates as follows.

$$P_{stim} = \frac{I_{stim}}{T_s} \int_0^{T_s} \left(V_{DD,stim}(t) - \left(R_S I_{stim} + \frac{I_{stim} \cdot t}{C_{DL}}\right)\right) dt \tag{2.7}$$

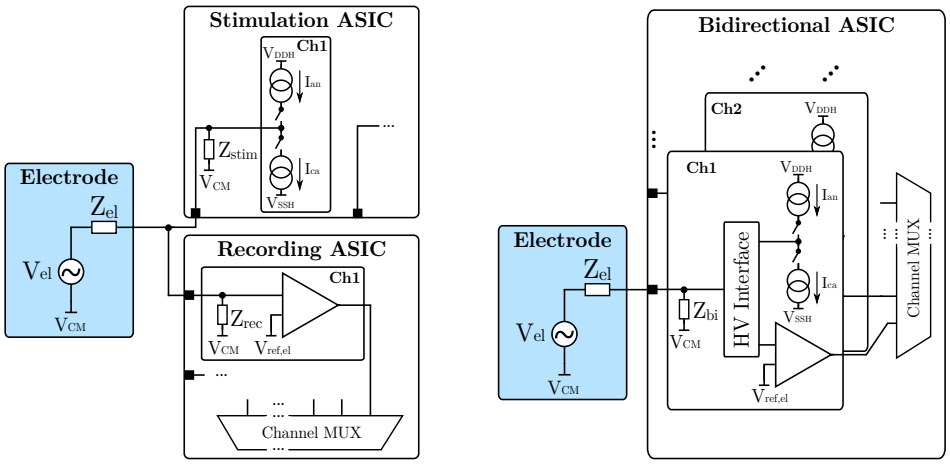
where C_{DL} is the double layer capacitance, R_S is the solution spreading resistance and the charge transfer resistance R_{CT} is neglected, since it is assumed that the electrode is operated in the non-Faradic regime (c.f. Section 2.2.1). This calculation shows that for a minimum power consumption, the stimulator supply has to linearly track the electrode voltage during a stimulation and that large voltage compliance comes with a power penalty, if a constant supply voltage is used. Therefore, a careful analysis of the expected electrode impedances is necessary to estimate the required voltage compliance, or load adaptive supply schemes can be used, as presented in several publications [73–76].

2.5 Multi channel bidirectional neural front-ends

2.5.1 Bidirectional neural front-ends

As described in section 2.1, electrical stimulation can be used to trigger an AP at a neuron, by modulation of the extracellular potential. In order to allow precise monitoring of the evoked neural activity, the neural signal must be recorded at the same site, to eliminate spatial offset. This can either be realized by connecting a standalone stimulator and recorder to the same electrode, or by combining both parts in one Application Specific Integrated Circuit (ASIC) to form a bidirectional channel.

Figure 2.17(a) shows the block diagram of a discrete realization, which consists of a standalone, multichannel stimulator and recorder, with one recording and stimulation channel connected to each working electrode. The advantage of this implementation is that commercial off-the-shelf ASICs can be, which saves development time and costs,



(a) Discrete implementation. (b) Integrated implementation.

FIGURE 2.17: Bidirectional neural interface architectures.

but comes with several disadvantages: The first, major disadvantage is a larger area consumption within the implant required for two separate ASICs, which leads to an increased implant size. The second, major drawback is the increased loading of the working electrode during recording periods. The input impedances Z_{rec} and Z_{stim} are usually dominated by the parasitic capacitance of the bonding pads, which results in an almost doubled capacitive load. This leads to a damping of the neural input signal, which can only be compensated by increasing the active area of the electrode, thus reducing the spatial resolution.

Figure 2.17(b) illustrates the architecture that was developed in this thesis. By combining a recording and stimulation channel on-chip, a higher level of integration can be achieved, which can be used to reduce the overall implant size. Furthermore, only one bonding pad is connected to the working electrode, thus reducing the aforementioned parasitic loading. In addition to that, an on-chip HV interface increases the circuit safety, as it automatically disconnects the recorder from the electrode during stimulation events, where potentially harmful voltage levels can be reached. Furthermore, the blind time after a stimulation event can be reduced, since a combined on-chip control logic can provide a more accurate synchronization of stimulation events and recorder blanking.

2.5.2 State of the Art

SoA multichannel, bidirectional neural front-ends combine several of the previously described recorder and stimulator circuits on a single chip to provide independent channels for a BMI. The noise performance of the recorder architectures is usually compared by

the Noise Efficiency Factor (NEF), which was first defined in [77] and can be calculated by the following formula.

$$\mathrm{NEF} = V_{rms,in}\sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot \mathrm{BW}}} \tag{2.8}$$

It takes into account the bandwidth BW of the amplifier, the total required current I_{tot} and its integrated, input referred noise $V_{rms,in}$ in said bandwidth. This noise is compared, to the integrated thermal noise of a single bipolar transistor in the same bandwidth, biased with the same current I_{tot} [77]. Fig. 2.18 illustrates the power-area-noise trade-off in the LNA design of neural recorders published in the Journal of Solid State Circuits (JSSC) and Transactions on Biomedical Circuits and Systems (TBioCAS) from 2010 to 2018. Shown is the maximum reported NEF vs. the active area, plotted over the achieved in-band noise. The frontier of the SoA is indicated in blue.

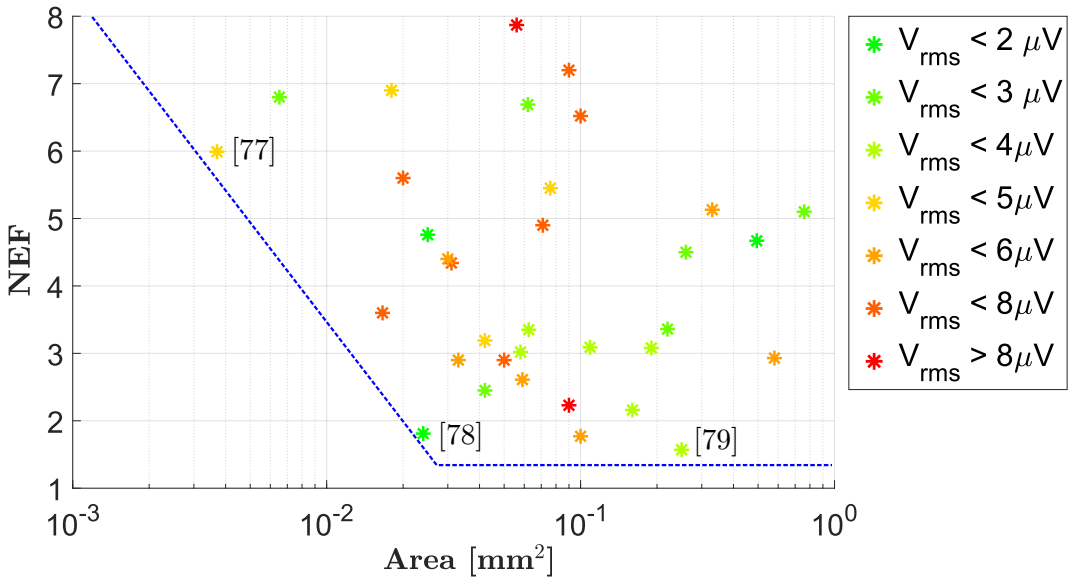


FIGURE 2.18: Illustration of the power-area-noise trade-off of various neural recorders from JSSC & TBioCAS 2010-2018.

Three designs stick out from Figure 2.18, as they mark the frontier of the SoA. Muller et al. achieved the smallest channel size in [78], as they got rid of the large coupling capacitors, required in the classical architecture, by using a semi-digital feedback loop with a DC coupled amplifier. However, this approach comes with very high manufacturing costs, as low area and power consumption can only be achieved through technology scaling. Furthermore, it does not allow the on-chip combination of a recording and stimulation unit, since supply voltages of less than 1 V cannot be exceeded in such small technology nodes, which would result in insufficient stimulator compliance.

In [79] Kim et al. achieve a high NEF, with small area and input referred noise, with a direct oversampling ADC that digitizes the neural signal without pre-amplification. The high area efficiency is achieved with a chopped, DC coupled input stage, which limits the allowed electrode DC offset to ±130 mV, making the design less robust than an AC coupled architecture. High power efficiency is achieved, by limiting the amplifier bandwidth the 500 Hz, which allows the use of a 32 kHz chopping frequency, but cuts-off the AP signal parts. In order to further improve noise and power efficiency, the design does not include any input impedance boosting, as it was e.g. presented in [10], which reduces circuit complexity but decreases the input impedance of the amplifier. Especially for small, high impedance electrodes this results in excessive loading of the working electrode, which causes a deterioration of signal quality or even harmful DC currents.

With a NEF of 1.57, the design presented in [80] by Han et al. achieves an almost ideal noise efficiency with a conventional architecture. A current reuse OTA biased in weak inversion is used to provide the maximum possible transconductance for the given bias current and thereby reduce the thermal noise. However, the overall area of 0.25 mm^2 shows the limits of this approach, since it requires a large active area for the input devices to reduce the 1/f-noise component.

In summary, the NEF vs area plot shows that a general trade-off between noise performance, noise efficiency and area has to be made in the design of neural amplifiers. However, a deeper analysis of only three publications shows, that a systems performance cannot be fully measured by these key parameters. Many different, functional approaches exist, where each one comes with further pros and cons, e.g. regarding recorder robustness, patient safety or possibilities for further system integration.

	JSSC'11 [81]	ISSCC'16 [21]	VLSI'17 [44]	JSSC'14 [82]	ESSCIRC'14 [55]	TBioCAS'16 [83]
No. Ch. (Rec/Stim)	8/8	16/160†	64/4	4/2+8	32/1	4/4
Area/ch.	0.51 mm^2	-	-	0.18 $mm^{2††}$	0.33 mm^2	0.12 mm^2
Technology	0.35 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Stimulator						
On-Chip /Ext.	On-Chip	On-Chip	On-Chip	On-Chip	Ext.	On-Chip
Supply [V]	5.05	±(6...12)	12	5	18	5
Stim. mode	CCS	CCS	CCS	CCS	CCS/CVS	CCS
$I_{Stim,MAX}$	94.5 µA	0.5 mA	5.04 mA	116 µA/ 4.2 mA	15 mA	0.25 mA
$V_{Stim,MAX}$	-	-	-	-	18 V	-
Stim. wvfrm.	Square	Square	Arbitrary	Arbitrary	Arbitrary	Arbitrary
Wvfrm. gen.	On-Chip	On-Chip	On-Chip	On-Chip	Ext. analog	On-Chip
Recorder						
Power [µW/ch]	19.9 LNA+HP	5.4 LNA+LP	8 LNA+ADC	245 LNA+ADC	2 · 48 Ch.+Driver	5.5 bioADC
Input noise [μV_{rms}]	3.12	7.68	1.6	6.3	4.67	1.0
BW	1.1 Hz - 12 kHz	5 Hz - 7 kHz	<1 Hz - 500 Hz	0.6 Hz - 6 kHz	0.2 Hz - 7.5 kHz	0.25 Hz - 250 Hz
NEF	2.68 LNA+HP	6.2	7.8 LNA+ADC	3.76	3.19 LNA*	4.67 ADC
ADC	On-Chip	On-Chip	On-Chip	On-Chip	Ext.	On-Chip
ENoB	9.2 bit	8.5 bit	12 bit**	8 bit	12 bit	9.4 bit

†: 40 current drivers with 1:4 Demux ††: Stim. output stage
*: AP band only **: Estimated from spectrum

TABLE 2.1: Performance compared to the state of the art

Table 2.1 compares recently published, bidirectional front-ends. Most of the shown stimulator designs use a supply level of 5 V, which has the advantage that the device size required for such a supply level is still relatively small, compared to 18 V or even 45 V devices that are available in HV CMOS. However, this results in a voltage compliance of less than 5 V, which is not enough to drive small, high impedance electrodes. Only

the design, presented in [55] by Bihr et al., provides a supply voltage of 18 V but has the drawback that it requires an external stimulator, whose current is demultiplexed to one of 32 recording electrodes. Overall, three designs,[21], [44], [55], provide only a shared stimulation unit between several electrodes. This reduces the flexibility in stimulation patterns and thereby the freedom in the design of experiments.

When looking at the recording capabilities, all implementations provide a similar recording bandwidth from ≤ 1 Hz to 6 - 12 kHz with an integrated noise around 1 - 7.7 μV_{rms}. Only the recorders in [44] and [83] have a cutoff frequency $\leq$500 Hz and are therefore not capable of recording LFP and AP signals at the same time. Although this results in significantly less power consumption, a potentially valuable part of the neural signal is lost.

Except for [81], all implementations use a 0.18 µm technology node, since it is widely available and offers comparably low manufacturing costs. Furthermore, many 0.18 µm technologies offer HV devices, which can be used to improve the voltage compliance of the stimulator as it was done in [21], [44] and [55]. This is absolutely necessary, since standard CMOS supply levels are usually insufficient to drive the varying electrode impedances.

The analysis of the SoA shows, that the stimulation flexibility is still quite limited in the existing implementations. Half of the designs feature less stimulators than recorders, by either multiplexing one current source to several electrodes, or by allowing stimulation only at several sites. This is a huge limitation for experiments as well as therapeutic applications, as it results in a loss of spatiotemporal resolution. A second shortcoming in the listed design is the stimulation supply and maximum current, required to allow the use of varying electrode types. For small, intracortical electrodes, a HV supply is required, which is only realized in three designs, of which one uses an off-chip stimulator. At the same time, a stimulator must be capable of delivering currents in the mA range, to drive large planar electrodes. Both criteria are only targeted by the implementation presented in [44], which has again the drawback of providing only 4 separate stimulators.

2.5.3 Challenges and requirements

When looking into the SoA it becomes obvious, that there are no exact specifications for neural interfaces. For the recording part, it is clear that low noise levels are always demanded because of the small neural signals. However, Fig. 2.18 clearly illustrates the trade-off between noise, power and area consumption of the recorder. Design techniques for further noise reduction, like chopping, work very well, but influence other parameters,

like the reduced input impedance of the amplifier. Therefore, it is very clear that not only one isolated parameter should be optimized but all trade-offs have to be considered.

In order to allow the use of small, intracortical electrodes, a robust recorder with high input impedance is required. This allows at the same time the usage of large, planar electrodes with low electrode impedance, which gives neurologists maximum freedom in the design of the overall system. In order to account for the unknown signal bandwidth, depending on the chosen electrode type, the recording bandwidth should be adjustable to the signal of interest, as this allows the end user a flexible trade-off between noise performance and signal bandwidth. Although, noise levels could in theory be designed arbitrary low, it is important for a practical recorder implementation to find a suitable trade-off between power/area consumption and noise performance. Thereby excessive area and power consumption can be avoided, which allows the use in a large channel count system.

The analysis of integrated stimulation units shows clearly that CCS offers major advantages regarding patient safety and area consumption. Compared to CVS, charge balanced pulses can be guaranteed within the voltage compliance for CCS and the maximum stimulation current is clearly defined, which are both key parameters for patient safety. Compared to CQS, CCS stimulators can be fully integrated, with an active area that allows for a high amount of parallel stimulation channels. In summary, these advantages make CCS the method of choice for integrated, implantable multi-channel stimulators. In order to allow knowledge transfer from previous CVS experiments to CCS, recent studies started to compare both stimulation methods, evaluating their safety, stimulation efficiency and required stimulation parameters against each other [35, 84, 85]. However, these clinical studies require in the best case a stimulation device that is capable of CCS and CVS, as otherwise an undesired level of uncertainty remains in the results, as the study in [85] shows. Two recent publications that compare CCS to CVS showed that it is in general safe to switch from voltage to current mode, but certain patients react event better to CVS than CCS [35, 84]. In order to allow further investigation on this topic, one clear challenge is to develop a stimulator, which can be reconfigured between CVS and CCS. This would allow the direct comparison of both methods and could provide the best stimulation pattern for each individual patient.

The analysis of both stimulator types however shows the same unsteadiness in the requirements for voltage compliance, maximum/minimum stimulation current/voltage and stimulation waveform as in the recorder parameters. This is again a result of the aforementioned variability of the electrode impedance and the varying physiological state of different patients, resulting in a high demand for arbitrary, patient specific, stimulation patterns. In order to allow the use of high impedance electrodes, the stimulator

requires a high voltage compliance, usually exceeding standard CMOS supply levels. Additionally, the voltage overhead of the stimulator should be as small as possible, to minimize the power dissipation. Last but not least, a high dynamic range is required for the stimulation amplitude, to allow the use of electrodes with a large range of charge capacities.

An additional challenge arises from the combination of stimulator and recorder. Since the voltage amplitudes that occur during stimulation can be 120 to 140 dB larger than the input referred noise of the recorder, the sensitive recorder must be protected during stimulation events, which is usually achieved by blanking. This blanking can be realized by protection switches that disconnect the recorder from the electrode during a stimulation and pull its input to a fixed potential [55]. However, during this blanking period the neural signal cannot be observed, leading to a undesired blind time. From the stimulator point of view, highly accurate charge balancing is required to minimize the residual voltage on the electrode, also referred to as stimulation artifact, in order to avoid recorder saturation after reconnection. In passive charge balancing, this is achieved by discharging the electrode over a transistor switch, which has the advantage of low power and area consumption, but the drawback that the discharging is not monitored [73]. To overcome these shortcomings, different active charge balancing methods have been presented. They either actively cancel the residual charge by insertion of the counter charge, e.g. via a regulated number of current pulses [86], or adjust the amplitude of one of the biphasic stimulation pulses until sufficient charge balancing is achieved [87]. Since the first described approach provides a fast cancellation of residual charge after every stimulation and the second approach is well suited for long-term charge balancing, different architectures that employ both methods can be found in the literature [73, 88, 89].

In summary a successful SoC for a BMI must offer high flexibility and adaptability for the following three reasons. First and foremost, BMIs interface with a living organism, the human brain that naturally varies not only from individual to individual, but also over time. Therefore, exact a priori knowledge about the electrode/tissue interface, the shape of the recorded signal or the response to stimulation patterns will never be available, but can only be estimated within certain limits. Second, research and especially therapy in the field of neuromodulation are still under heavy research. This results in only vaguely defined requirements for neural interfaces, which can change due to new scientific findings. Third, a BMI must be applicable in different scenarios, in order to allow the variation of other parameters and investigate their influence.

Chapter 3

Neural recorder design

In this chapter, the implementation of the neural recorder unit and its HV compliant interface to the stimulator is shown. The design is based on the recorder that was developed in a previous Ph.D. thesis [12] and adds further functionality. As a first improvement the recorders 1/f-noise was enhanced by a redesign of the OTA used in the LNA. Further, a tunable high-pass corner frequency was introduced to the recorder by pseudo resistor tuning in the feedback path. As a last addition, an online electrode impedance estimation was realized by including a low gain mode into the first amplifier stage.

3.1 Previous design

Fig. 3.1 shows the block diagram of the previously designed neural recorder, which was published in [55] and [12].

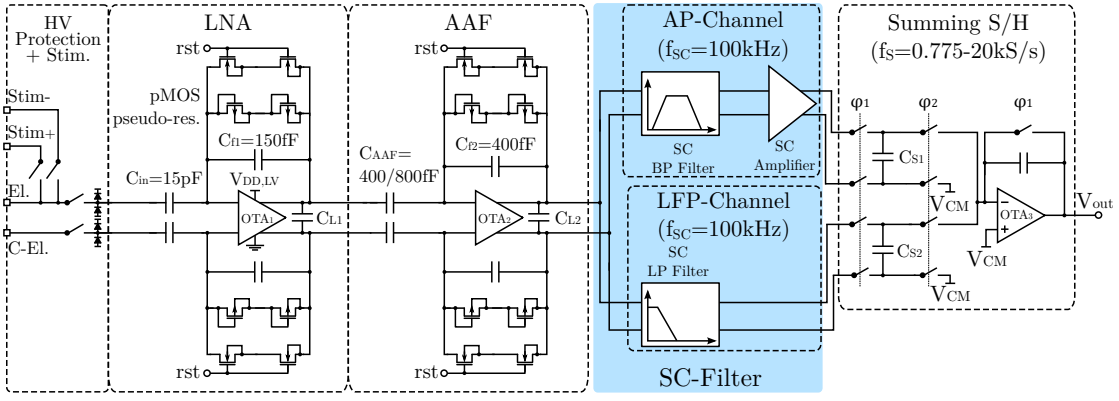


FIGURE 3.1: Neural recorder with spectral separation from [12].

In front of the recorder a HV interface is installed, which will be presented in detail in chapter 4. It provides two stimulation switches, which can connect the electrode to an external, bidirectional current stimulator and two blanking switches, used to protect the LNA from harmful voltage levels during stimulation events. The complete recorder channel consists of an AC coupled LNA with pseudo resistor feedback which is followed by an Anti-Aliasing Filter (AAF) that uses the same structure. Two Switched Capacitor (SC) based biquad filters are used for spectral separation of LFPs and APs and a summing Sample-and-Hold (S/H) amplifier recombines the two signal parts.

The original LNA is a fully differential implementation of the neural amplifier from [67]. It offers an AC coupled, differential input in order to remove any DC-offsets from the electrode/tissue interface. pMOS pseudoresistors are used in the feedback to realize a high-pass cutoff frequency in the sub-Hertz range, which allows the recording of low frequent LFP signals. The closed-loop amplifier has a low-pass cut-off frequency of 7.5 kHz, set by the load capacitor C_{L1}, which is high enough to allow AP recording as well. The inband gain of $A_{LNA} = \frac{C_{in}}{C_{f1}} = 40\,\text{dB}$ is achieved with an input capacitor of C_{in} =15 pF and a feedback capacitor of $C_{f1} = 150\,\text{fF}$. After the LNA an AC coupled AAF with a selectable gain of 0/6 dB and a low-pass cutoff frequency of 50 kHz is used to filter out the DC offset of the LNA and further suppresses signals with a frequency higher than 50 kHz. This second order filtering is required to avoid a loss of signal quality due to aliasing and noise back folding caused by the subsequent SC filters.

In order to separate the low frequency LFPs from the high frequency APs two SC biquad filters with a sampling frequency of $f_{SC} = 100\,\text{kHz}$ are used. A SC implementation was chosen as it allows to realize the required small corner frequencies without excessive area consumption and good linearity. The low-pass filter in the LFP band provides a selectable cut-off frequency of $f_{LFP} = 100/200/400\,\text{Hz}$ and an adjustable gain of $A_{LFP} = 0/6/12\,\text{dB}$. In the AP signal path a bandpass filter with a selectable high-pass cutoff frequency of $f_{AP} = 100/200/400\,\text{Hz}$ and a gain of $A_{AP} = 0/6\,\text{dB}$ filters out the high frequency signal path. Since APs have a much smaller amplitude than LFPs, an adjacent SC amplifier provides an additional, selectable gain of $A_{AP} = 6/12/15/18\,\text{dB}$ after the bandpass filter. This spectral separation allows to individually set the gain for the LFP and AP band, which can be used to equalize the spectrum of the neural signals. This is important, as usually the signal amplitude is much lower in the AP band than in the LFP band and only through equalization the full ADC resolution is used for both signal parts.

After the described spectral separation, a summing S/H is used to recombine the two signal paths and to provide a differential-to-single-ended conversion at the same time (c.f. Fig. 3.1). Additionally, the S/H can be used to deactivate one of the signal paths,

by deactivating the clock ϕ_1 at the corresponding input switch. This can be used to reduce the sampling frequency to lower values if only LFP signals are recorded, which can be used to safe power in the originally used off-chip ADC and the telemetry unit [55].

In [12] it has already been shown, that the noise of the complete channel is dominated by the LNA noise. Therefore, the first amplifier stage was again analyzed an redesigned to further reduce the inband noise. Table 3.1 summarizes the key parameter of the previous recorder.

Design		Original [12]
Gain	LFP	39 dB - 57 dB
	AP	45 dB - 69 dB
Bandwidth	LFP	200 mHz - (100/200/400 Hz)
	AP	(100/200/400 Hz) - 7.5 kHz
Input ref. noise	LFP	$3.3\,\mu V_{rms}$
	AP	$3.3\,\mu V_{rms}$
Area	LNA	$0.033\,mm^2$
	Rec + FE	$0.182\,mm^2$
Power	LNA	11.8 µW
	Rec + FE	52 µW
NEF LNA	AP	3.19

TABLE 3.1: Performance of the original recorder design.

3.2 Noise improvement

Figure 3.2 shows the measured output referred noise spectrum of the old recorder design in the LFP and AP band. In the LFP band it is clearly visible, that the noise is dominated by 1/f-noise, whereas the AP band shows only white noise, shaped by the transfer function of the recording channel.

The noise analysis in [12] showed, that the LNA is the dominating noise contributer with a noise share of 81 % in the LFP band and 87 % in the AP band. Therefore, its noise was again simulated to identify the main noise contributers and further optimize the performance. Figure 3.3 shows the schematic of the LNA and its OTA, implemented

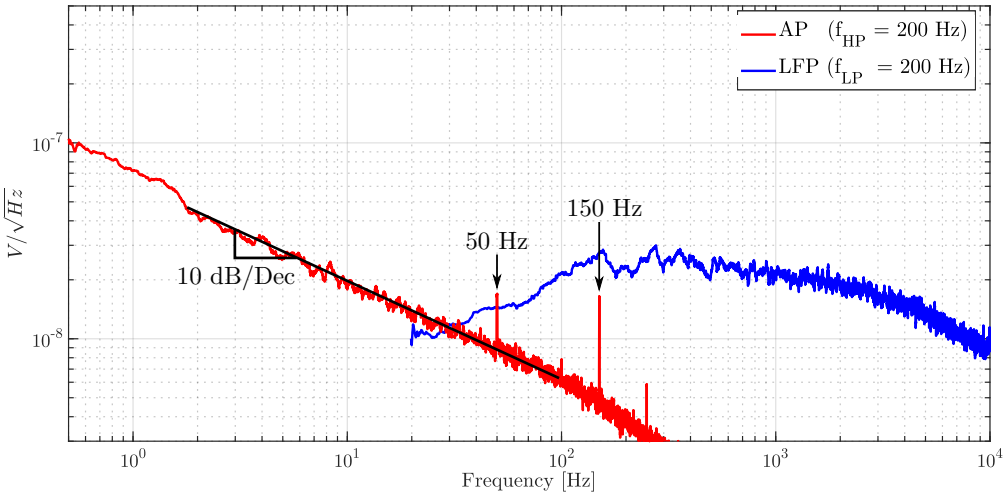


FIGURE 3.2: Measured output referred noise, divided by midband channel gain of the original recorder for LFP and AP band, with maximum gain settings in both bands.

as a telescopic amplifier with continuous time Common Mode Feedback (CMFB). Additionally, the noise current sources of transistors $M_{3/4}$ have been added in parallel to the according transistor. In order to reduce the 1/f noise of the input devices a pMOS input pair has been used, since their 1/f noise is significantly smaller compared to nMOS devices [90].

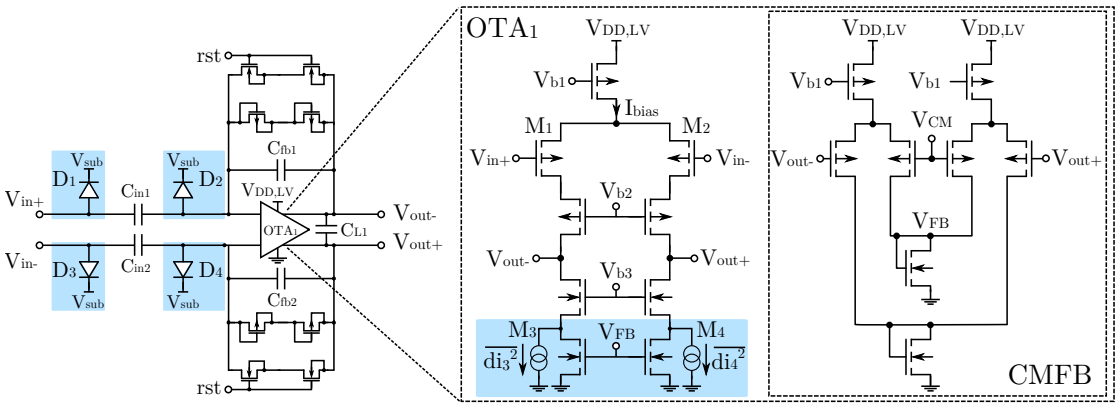


FIGURE 3.3: Schematic of the original neural recorder. Highlighted are the main noise contributers in the LFP band.

Schematic level simulations showed, that the main noise source in the LFP band was the 1/f-noise of the load transistors $M_{3/4}$. According to [90] the noise density of $M_{3/4}$s 1/f noise can be expressed as follows.

$$\overline{di^2_{1/f}} = \frac{KF_F \cdot g_m^2}{W \cdot L \cdot C_{ox}^2} \frac{df}{f} \tag{3.1}$$

where KF_F is a coefficient which depends on the transistor and technology, C_{ox} is the technology dependent unit oxide capacitance, g_m is the transistors transconductance, W the transistor width and L the transistor length. In order to reduce the 1/f noise of $M_{3/4}$ their area was increased by a factor of 4, while keeping the aspect ratio constant. Since the whole area of the LNA is dominated by the 15 pF input capacitors, this could be done with a negligible area penalty.

After the described redesign, simulations showed that the 1/f noise of the input pair $M_{1/2}$ is now dominating the noise in the LFP band and their thermal noise is dominant in the AP band. Following the same explanation as before, the 1/f noise could be further reduced by increasing the area of the input pair. However, this would increase the parasitic input capacitance C_{OTA} of the OTA, which results according to [67] in the following noise penalty.

$$\overline{v_{LNA}^2} = \left(\frac{C_{IN} + C_{fb} + C_{OTA}}{C_{IN}}\right)^2 \cdot \overline{v_{OTA}^2} \tag{3.2}$$

where $\overline{v_{LNA}^2}$ is the integrated noise power of the LNA and $\overline{v_{OTA}^2}$ is the integrated noise power of the OTA. Since a further increase of C_{in} would result in a huge area penalty, the area of the input devices was not further increased.

After the redesign a significant mismatch between the LFP noise of the schematic level simulation and the measured noise could be observed. The measured prototype revealed an input referred noise of 3.4 μV_{rms}, whereas the simulations resulted in a noise of only 2.9 μV_{rms}. The increased noise was caused by the diodes $D_{1\text{-}4}$ which were originally installed in the layout to avoid the violation of antenna rules, which could lead to plasma charging damage. After analog extraction of said diodes, their 1/f-noise contribution could be simulated in the LFP band, resulting in an improved matching between simulation and measurement. In a second prototype, these diodes were removed and the layout was modified to meet the required antenna rules without them, leading to the improved performance listed in Table 3.2.

Although the comparison shows an area penalty of $\sim$ 10%, this is not caused by the previously described, increased transistor size, but for two different reasons. First, the recorders functionality was extended by a low gain mode and a tunable cut-off frequency, which is described in the following Sections. Second, there was a change in the 180 nm CMOS technology, through which the previously used capacitors had to be replaced by a different capacitor type, resulting in a 25 % reduced capacitance per area for the new capacitors.

Design		Original [12]	Revised
Gain	LFP	39 dB - 57 dB	39 dB - 57 dB
	AP	45 dB - 69 dB	45 dB - 69 dB
Bandwidth	LFP	200 mHz - (100/200/400 Hz)	200 mHz - (100/200/400 Hz)
	AP	(100/200/400 Hz) - 7.5 kHz	(100/200/400 Hz) - 7.5 kHz
Input ref. noise	LFP	3.3 μV_{rms}	2.9 μV_{rms}
	AP	3.3 μV_{rms}	3.3 μV_{rms}
Area	LNA	0.033 mm^2	0.036 mm^2
	Rec + FE	0.182 mm^2	0.190 mm^2
Power	LNA	11.8 µW	11.8 µW
	Rec + FE	52 µW	52 µW
NEF LNA	AP	3.19	3.19

TABLE 3.2: Performance of original and revised recorder design.

In order to reduce the noise in the AP band, the thermal noise of the input devices needs to be reduced, which can only be achieved by increasing the transistors g_m. However, since $M_{1/2}$ already operate in week inversion, a higher g_m can only be achieved by increasing the biasing current I_{bias}, which would result in an undesired increase of power consumption.

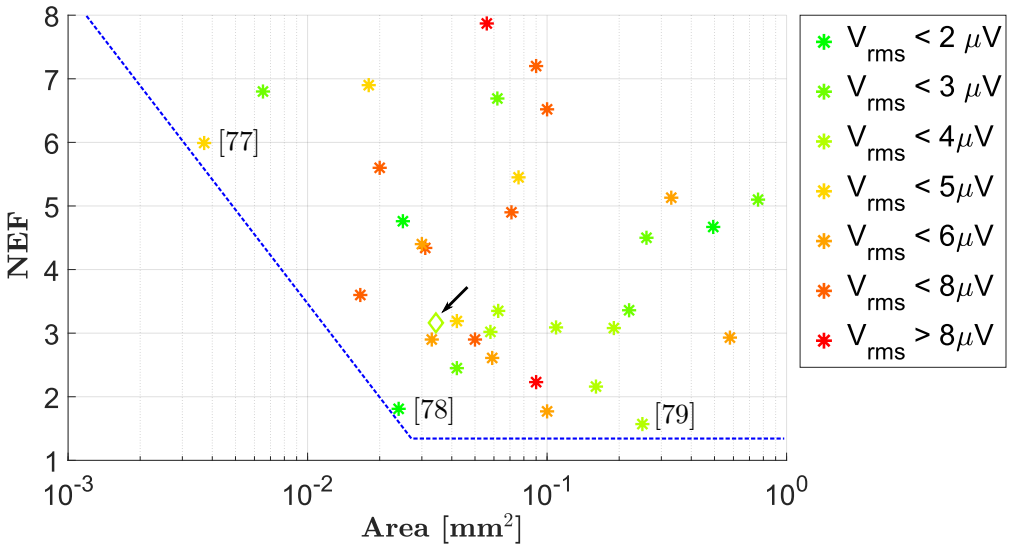


FIGURE 3.4: Comparison of the revised recorders NEF to the SoA.

Figure 3.4 shows that the revised recorder achieves a good trade-off between NEF, area consumption and input referred noise, compared to the SoA. In section 2.5.2 the designs at the frontier of the SoA have already been discussed and their shortcomings compared to the presented implementation has been highlighted. Again, the main reasons for the

chosen implementation were its high input impedance due to AC coupling, its robustness against DC offsets and the compatibility to an on-chip HV stimulator due to the available HV devices in the chosen technology.

Other designs in the proximity of the presented implementation show, that it is possible to further improve the NEF and noise performance, which can be easily achieve by implementing the OTA within the LNA as a current reuse amplifier. Thereby the g_m of the input stage is increased, which reduces the input referred, thermal noise component as previously discussed and thereby directly improves the NEF. However, this improves only AP band performance, since the LFP band is 1/f-noise limited. Since the nMOS input transistors that are required for a current reuse input stage provide worse 1/f-noise performance, this results in an observable area penalty in order to meet the same LFP noise specifications.

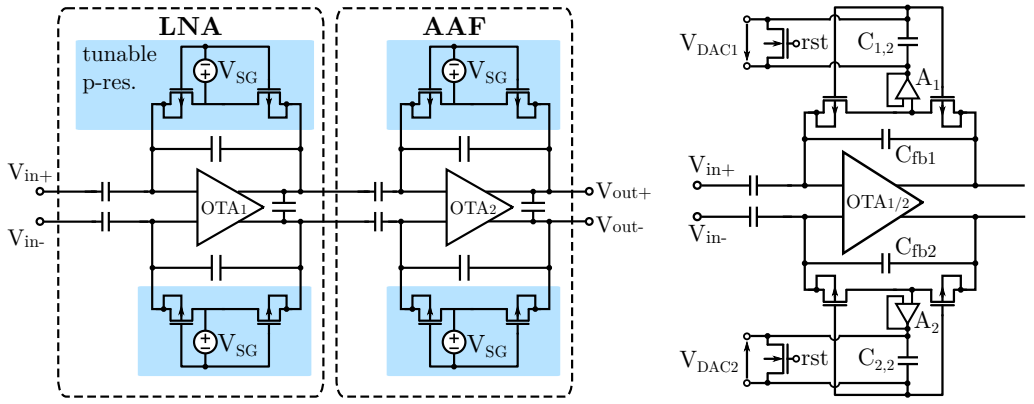
3.3 Tunable neural recorder

The use of a pMOS pseudo resistor in the feedback path offers the previously explained advantage of DC suppression, while providing a high-pass corner frequency that is low enough to record in the sub-Hertz range. However, this technique comes with the drawback that the absolute value of the pseudo resistor is subject to strong variations due to process variations. This shortcoming led to the idea of using an adjustable pseudo resistor, which allows to achieve a tunable high-pass cutoff frequency [13, 91, 92]. The resistance of the pseudo resistor R_{SD0} can be calculated by a linearization around the DC operating point, where the voltage across the resistor $V_{SD} = 0\,V$. Based on the EKV model, this leads to the following expression [93]

$$R_{SD0} = \frac{U_T}{I_0} \exp\left(-\frac{V_{SG}}{n \cdot U_T}\right) \tag{3.3}$$

where U_T is the thermal voltage, V_{SG} is the Source-Gate voltage, n is the slope factor and I_0 is the residual channel current. From Equation 3.3 it can be seen, that the resistance of the pseudo resistor can be exponentially tuned by applying a selectable Source-Gate voltage.

In [91] an approach was presented in which the voltage drop over a diode connected MOS transistor is used to set the Gate-Source voltage V_{GS} of the pseudo resistor. This allows to reduce the resistance, by forcing an adjustable bias current through the diode, which resulted in a high linearity and a large dynamic range tunable recorder. However, the implementation has the drawback of only a moderate tuning range caused by the



(a) Block diagram of the tunable recorder and AAF.

(b) Implementation of the floating battery $V_{SG1/2}$, [13].

FIGURE 3.5: Neural recorder front-end with tunable high-pass frequency.

limited maximum applicable biasing current that causes a static power consumption. In a different design, presented in [92], a two-stage tuning is implemented, which splits the tuning range into a coarse and a fine tuning. The coarse tuning is achieved by a back-to-back MOSFET switch, which is digitally switched off to achieve the high impedance mode, or switched on to achieve the low impedance mode. In series to this switch a pseudo cross-coupled resistor whose resistance is controlled by a 2-Bit current DAC was used for fine tuning. Although the tuning range of this implementation is significantly increased by splitting it into fine and coarse tuning, the resistance change between the on and off state of the back-to-back switch is relatively high. This leads to a large jump of the cut-off frequency, which leaves a large frequency range uncovered.

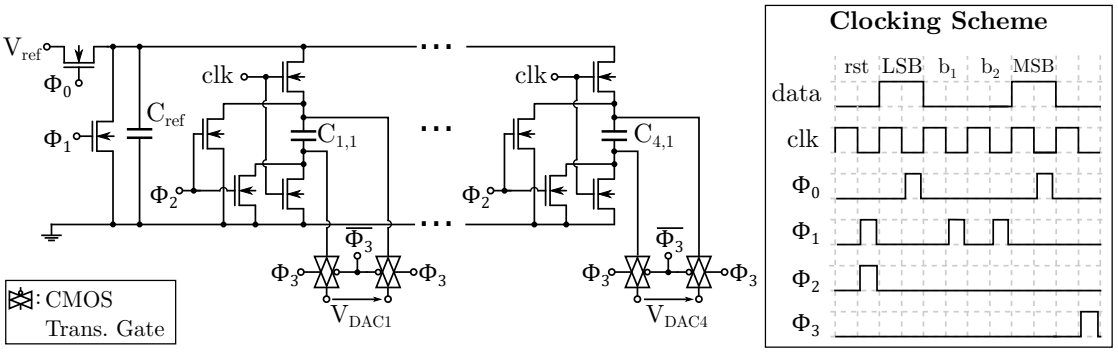


FIGURE 3.6: SC serial DAC used for pseudo resistor tuning, modified from [13], with permission from ©2016 IEEE.

In the approach developed with this these, that was presented in [13], four floating bias voltages $V_{SG1\text{-}4}$ are used to tune the pseudo resistors, as shown in Figure 3.5(a). As it can be seen from Equation 3.3, an exponential tuning characteristic can be achieved by linearly adjusting $V_{SG1\text{-}4}$, which has the advantage of providing sufficient resolution for low frequencies, while covering a wide tuning range.

Therefore the digitally adjustable voltage V_{SG} is generated with a liner, 4 bit serial SC DAC, which is shown in Figure 3.6. It is operated with a clock frequency of $f_{DAC} = 1\,\text{MHz}$, resulting in an update rate of 200 kHz and a dynamic power consumption of $P_{DAC} = 4.3\,\mu\text{W}$. The DAC provides a reference free, differential output voltage between 0 V and 500 mV with a 4 bit resolution at four separate outputs V_{DAC1} to V_{DAC4} and requires an active area of 330 µm x 70 µm. An additional advantage of the chosen architecture is, that the DAC can be switched off if no tuning is required, reducing its current consumption to negligible leakage currents.

By sizing the reference capacitor $C_{ref} = 4 \cdot C_{1\text{-}4,1}$ 4 times as big as the 4 working capacitors $C_{1\text{-}4,1}$, one shared reference capacitor can be used to generate all four outputs. This does not only improve the area efficiency, but also eliminates a possible mismatch in the tuning voltages. Since all working capacitors are shorted whenever the clock signal is high, it is ensured that $V_{DAC,1} = V_{DAC,2} = V_{DAC,3} = V_{DAC,4}$, which avoids a loss of linearity due to mismatch in the tuning voltage.

After each conversion cycle, the 4 outputs of the DAC are used to periodically charge the floating capacitors $C_{1\text{-}4,2}$ of the LNA and the AAF, which is shown in Figure 3.5(b) for the LNA only. A periodic refresh with a frequency high enough to be out of the signal band is necessary in order to compensate for leakage currents and maintain a constant biasing voltage. Since the AAF is designed with a cut-off frequency of 50 kHz, the suppression of the artifacts that are generated in the LNA by the updates of $C_{1,2}$ and $C_{2,2}$ is so high, that they disappear in the noise floor. The tuning artifacts that are generated in the AAF, are input referred suppressed by the gain of the LNA, which is also high enough to push them below the noise floor.

When using the DAC output to bias the pseudo resistors one problem that occurs is that the high impedance node between the two pMOS transistors of the pseudo resistor, is not able to drive the output capacitors of the DAC. This results in a slow transient behavior, which can be improved by adding two unity gain buffers A_1 and A_2 to improve the floating battery, as shown in Figure 3.5(b). Each buffer consumes a current of 50 nA from the 3 V supply, resulting in an overall power consumption of 0.6 µW, which is negligible compared to the combined 13 µW consumed by the differential amplifiers of the LNA and the AAF.

Figure 3.7 shows the measured Transfer Function (TF) of the LFP channel for minimum gain settings. It can be seen, that the midband gain stays constant at 40 dB, while the high-pass corner frequency can be tuned between 200 mHz up to 4 kHz. The initial jump of the corner frequency is caused by an offset of the SC serial DAC, which produces a tuning voltage slightly bigger than 0 V for an all zero input word caused by charge injection. When the digital control word is increased, the predicted exponential tuning

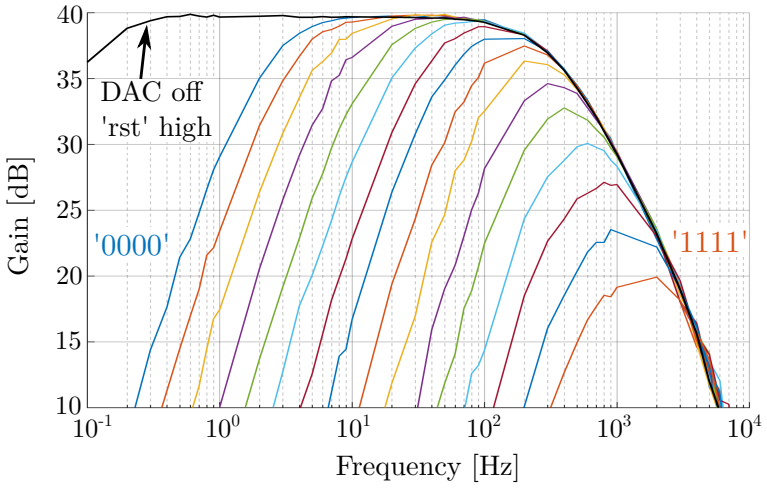
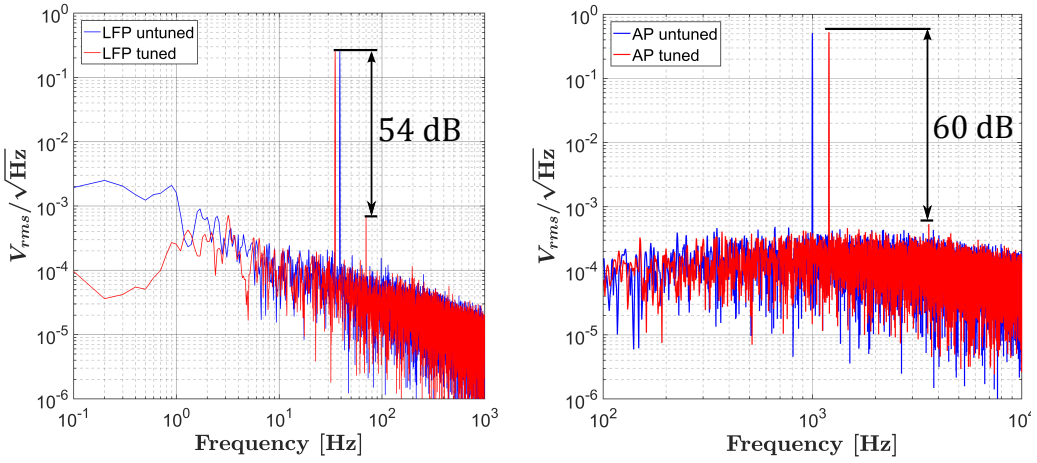


FIGURE 3.7: Measured LFP transfer function of the tuned recorder.



(a) LFP channel (b) AP channel

FIGURE 3.8: Measured output spectra of the tuned (red) and untuned (blue) recorder [14].

characteristic can be observed, which results in equidistantly spread cut-off frequencies in the logarithmic plot. The initial offset could be reduced by increasing the capacitor sizes of the SC DAC, thus reducing the effect of charge injection.

Figure 3.8 shows the measured output spectra for the LFP and AP band in untuned mode and when the lower cutoff is tuned to 4 Hz. In order to demonstrate the effect of tuning on the linearity, two sinusoidal input signals were applied to the recorder in each band. For the LFP channel an input frequency of $f_{in,LFP} = 35/39$ Hz was used and for the AP channel $f_{in,AP} = 1/1.2$ kHz was used. Under both conditions the in-band noise floor stays constant and a linearity of more than 54 dB is achieved. However, it can be observed that the integrated LFP noise is reduced, as the low-frequency 1/f-noise is

filtered when the lower cut-off frequency is increased. This allows a trade-off between measurement bandwidth and in-band noise during runtime [14].

3.4 Electrode impedance estimation

A major problem in the design of neural interfaces is the unknown and varying electrode impedance as previously described. Since it affects the quality of the recorded signal, as well as the optimum stimulation parameters and the safe stimulation boundaries [61, 94], the possibility of characterizing the electrode impedance is of great advantage [95]. Since the electrode/tissue interface can heavily vary over time due to changing tissue adhesion, scarring or electrode degeneration, online impedance monitoring provides crucial information, which can improve patient safety by detecting broken electrodes and adjusting stimulation parameters in the case of impedance changes.

The implemented impedance estimation is based on the measurement of the electrode impulse response to estimate the parameters of a simplified Randles cell model. Similar to the system presented in [21] the electrode voltage is measured while a short current pulse with the minimum amplitude of $I_{stim} = 32\,\mu A$ is driven into the electrode by the CCS. However, in contrast to the approach in [21] the shown implementation, which was presented in [13], does not use a dedicated signal path for impedance estimation, but uses the recording channel itself to measure the impulse response of the electrode. This has the advantage, that the impedance estimation can be performed at every electrode and is not limited to a few testing electrodes.

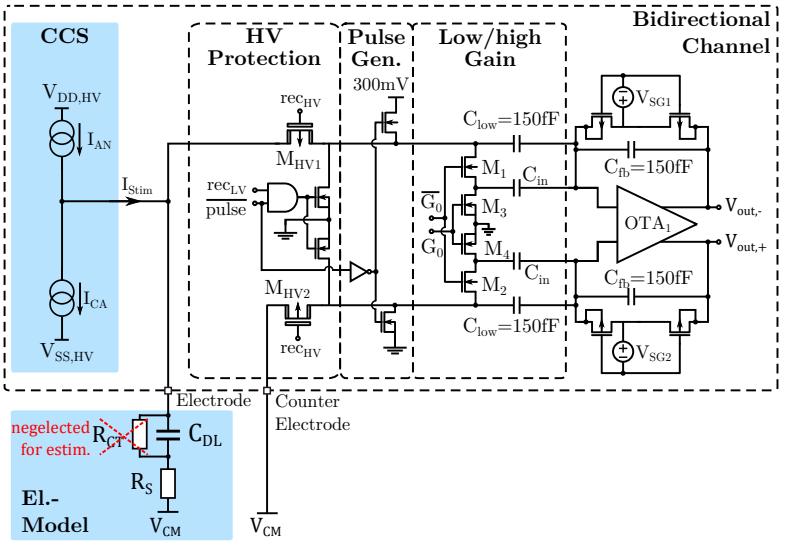


FIGURE 3.9: LNA with low gain mode and impulse source for bio-impedance estimation modified from [13], with permission from ©2016 IEEE.

In order to allow the reuse of the neural amplifier to measure the impulse response an additional low gain mode has been realized, which is shown in Figure 3.9. This is needed since the resulting voltages would drive the LNA into saturation during the impedance estimation. The low gain mode is activated by the control signal G_0, which disconnects the 15 pF input capacitors C_{in} from the input, by opening the nMOS switches $M_{1/2}$. Two additional switches $M_{3/4}$ pull the input capacitors to ground, in order to eliminate the parasitic signal path over the open transistor switches $M_{1/2}$ through the input capacitors, which would otherwise alter the amplifiers transfer function. The remaining input capacitor is then formed by $C_{low} = C_{fb}$, resulting in an in-band gain of 0 dB. Figure 3.10 shows the simulated TF of the LNA, followed by the AAF, in low and high gain mode. As the upper cut-off frequency f_{high} is set by the gain-bandwidth of the differential amplifier and the lower cut-off $f_{low} = \frac{1}{2\pi C_{fb} R_{ps}}$ by the feedback capacitor and the pseudo resistor, both are independent of the gain mode and only the midband gain is reduced to 0 dB.

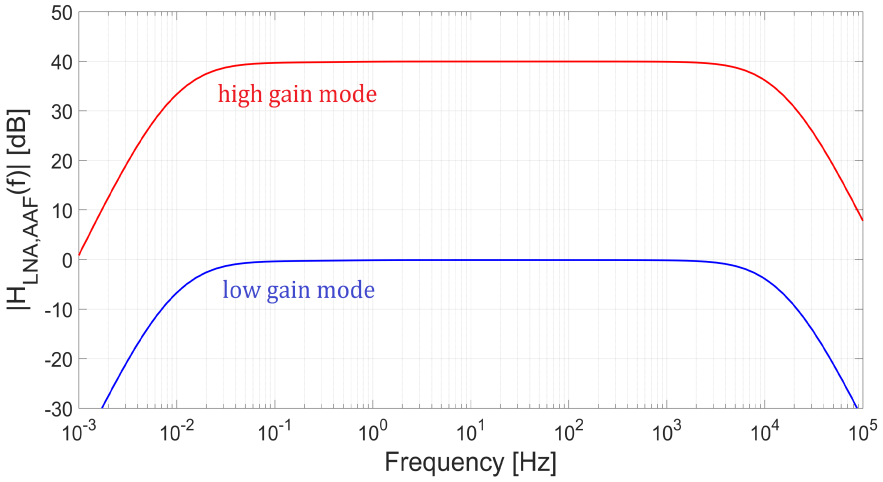


FIGURE 3.10: TF of the LNA and AAF in low gain and high gain mode.

A remaining issue is, that when the neural amplifier is used to estimate the transfer function, the result is not only the impulse response $H_{el}(s)$ of the electrode, but the combined response $H_{comb}(s) = H_{el}(s) \cdot H_{rec}(s)$ of the electrode and the recorder. Since the recorder TF varies due to process variations, device mismatch and aging, an on-chip characterization method is implemented, using the same impulse response based estimation method. Therefore, the recorder is disconnected from the electrode and the stimulator via the HV protection switches $M_{HV1/2}$ and a 100 µs short, 300 mV voltage pulse is applied over the nMOS switches of the pulse generator. After measuring the recorders impulse response, the parameters of the channel can be estimated, based on the second order TF $H_{LNA}(s)$.

$$H_{LNA}(s) = A_0 \cdot \frac{2\pi f_{high} \cdot s}{(s + 2\pi f_{low}) \cdot (s + 2\pi f_{high})} \cdot e^{-s \cdot \tau_{ch}} \tag{3.4}$$

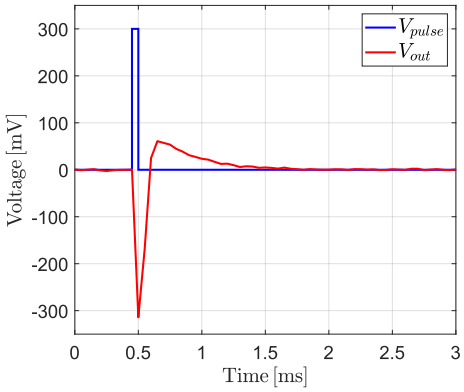
Due to the discrete time operation, the channel introduces an unknown dead time τ_{ch} from the input of the pulse generator to the channel output. It is estimated by sweeping τ_{ch} from 0.5 to $1.5 \cdot T_S$, where T_S is the sampling period of the output S/H and choosing the τ_{ch} that provides the best fit.

After the characterization of the LNA, the electrode is reconnected to its input and an anodic current pulse with the minimum amplitude of 32 µA and a duration of 100 µs is applied. The combined impulse response of electrode and recorder is measured over the AP channel in order to estimate the TF H_{comb}. This estimation is based on a TF with 3 poles, 2 zeros and a dead time τ_{comb}, as the electrode model adds one additional pole and zero, since the charge transfer resistor $\mathrm{R_{CT}}$ is neglected in the estimation. Using the aforementioned algorithm, all necessary parameters can then be estimated. Since the calculated dead times do not influence the result of the parameter estimation, τ_{ch} and τ_{cmp} are both set to zero from here on. However, they cannot be neglected at first, since this would lead to wrong values for the estimated poles and zeros.

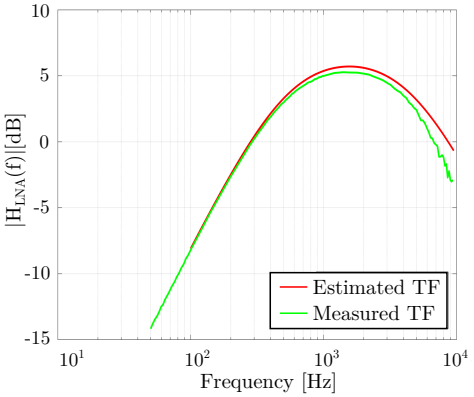
From the channel measurement the parameters C_{DL} and R_S of the Randles cell model can be estimated. As the charge transfer resistance R_{CT} is usually negligible if the electrode is operated within safe limits (c.f. section 2.2), it is replaced by an open. This results in the following, simplified TF for the electrode impedance.

$$H_{el}(s) = \frac{V_{el}(s)}{I_{stim}(s)} = \frac{R_S C_{DL} \cdot s + 1}{C_{DL} \cdot s} = \frac{H_{comb}(s)}{H_{LNA}(s)} \tag{3.5}$$

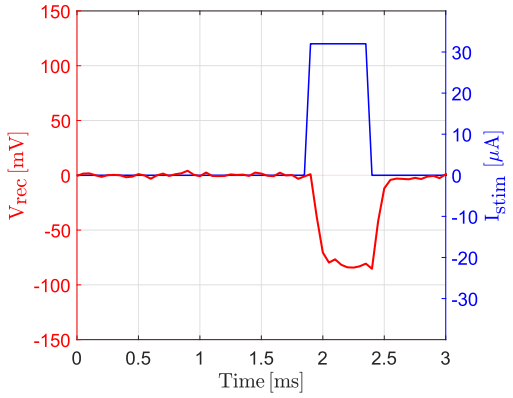
Figure 3.11 shows the estimation process which was measured using a linear, lumped element electrode model with a solution resistance of $\mathrm{R_S} = 1\,\mathrm{k\Omega}$, a double layer capacitance of $\mathrm{C_{DL}} = 290\,\mathrm{nF}$ and a charge transfer resistor $\mathrm{R_{CT}} = 1\,\mathrm{M\Omega}$. First the channel TF is estimated by recording the recorder output while the 100 µs voltage pulse is applied. In (a) the transient waveform of the input pulse and the recorded channel response is plotted, (b) shows the resulting TF estimation and compares it to the measured channel TF. It can be seen, that the estimation matches the measurement very well, with an error of less than 1 dB in the pass band (200 Hz - 7.5 kHz). After the channel estimation the impulse response of the electrode is measured, which is shown in (c) and the corresponding RC-model estimation is shown in (d), together with the impedance of the ideal model. The estimation results in $\mathrm{R_S} = 1.15\,\mathrm{k\Omega}$ and $\mathrm{C_{DL}} = 256\,\mu\mathrm{F}$, which corresponds to an error of 1.2 dB in the impedance magnitude.



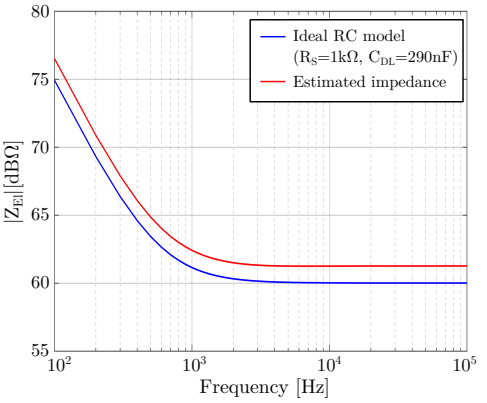
(a) Transient response of the recorder to the 300 mV voltage pulse.



(b) Estimated and measured AP channel transfer function with LNA in low gain mode.

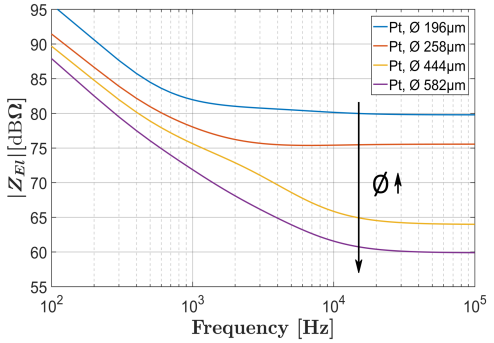


(c) I_{Stim} pulse for electrode estimation and measured recorder output.

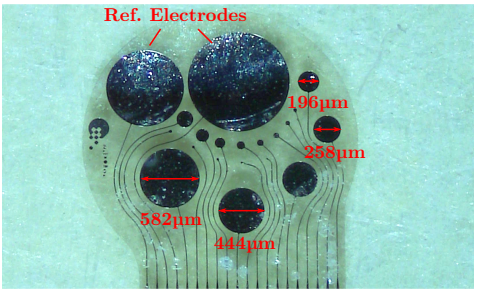


(d) Electrode impedance estimated from measured impulse response and ideal impedance.

FIGURE 3.11: Measured electrode impedance estimation for a lumped elements electrode model ($R_S = 1\,k\Omega$, $C_{DL} = 290\,nF$).



(a) Estimated impedance of Pt electrodes in PBS.



(b) Pt electrodes with varying diameter by courtesy of Dr. Eickenscheidt, IMTEK, Freiburg.

FIGURE 3.12: Electrode impedance estimation of planar Pt electrodes.

In order to validate the results from the linear model, an array of different sized, planar Pt electrodes was measured in Phosphate Buffered Saline (PBS). Figure 3.12 (b) shows the electrodes of which the two largest were used as a common reference, in order to

ensure a reference impedance low enough to be negligible. In (a) the resulting estimations for the electrodes with a diameter of 196 µm to 582 µm are plotted. It can be clearly seen, that the bio-impedance decreases with increasing electrode surface, making the electrodes clearly distinguishable. This allows in-vivo monitoring of electrode degradation, since a large range of bio-impedances can be detected.

3.5 Area and power breakdown

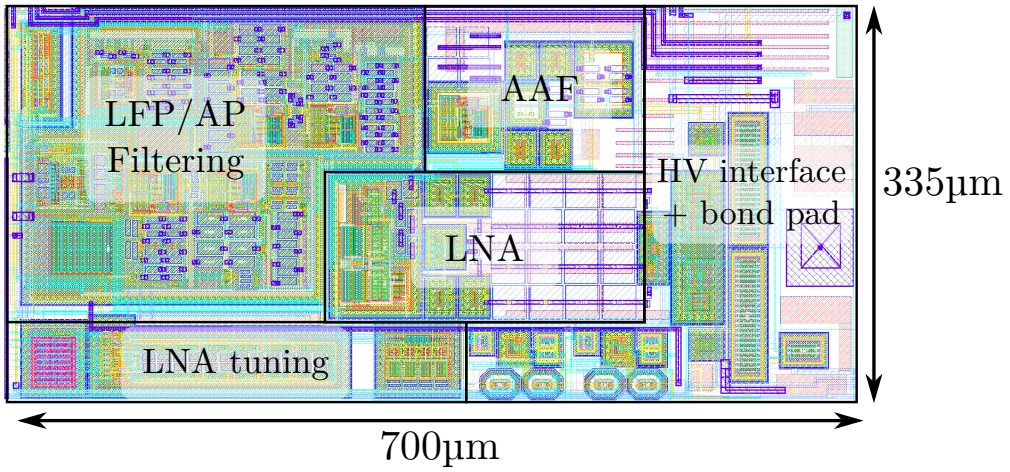


FIGURE 3.13: Layout of the neural recorder.

Figure 3.13 shows the layout of the complete recording channel, including the 57 x 66 µm^2 bond pad. The area and power shares of the different system parts are visualized and listed below.

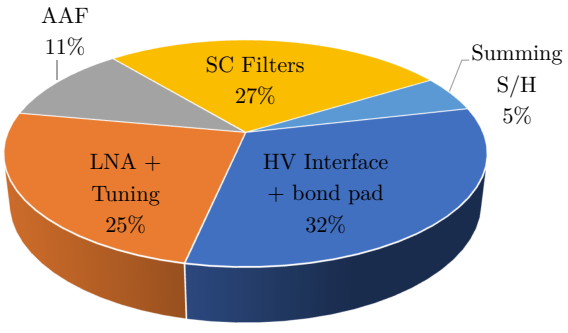


FIGURE 3.14: Area share of the recording channel.

Block	**Area [µm^2]**
HV interface + bond pad	75,000
LNA	34,000
LNA tuning	23,500
LFP channel	22,000
AP channel	42,000
Summing S/H	12,000

TABLE 3.3: Absolute area of the system blocks.

The main area consumer is the HV interface, as it includes the large bonding pad and the bulky HV blanking transistors. Due to the aforementioned noise limitations and the comparably large minimum length of the HV compliant transistors, this area cannot

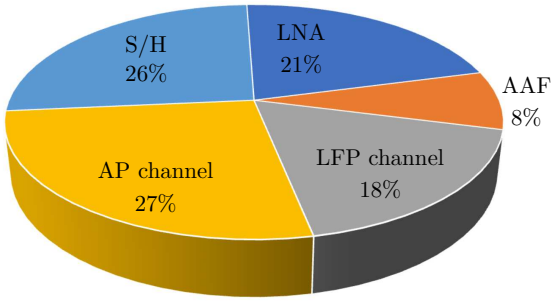


FIGURE 3.15: Power share of the recording channel (Tuning: ON).

Block	Power
LNA	11 µW
AAF	6 µW
Tuning (ON/OFF)	4.9/0.6 µW
LFP channel	13.2 µW
AP channel	19.8 µW
Summing S/H	19.2 µW

TABLE 3.4: Power consumption of the system blocks.

be reduced. The second largest area consumer are the SC filters, used for spectral separation, whose area is dominated by noise limited capacitor sizes.

The table above lists the power consumption of the different system blocks. Together with the previous area analysis it can be seen, that the spectral separation filters have a rather large power and area share. As explained in [12], this is beneficial if a power hungry or bandwidth limited telemetry unit is used. However, when switching to a UWB based data link in future implementations, this part offers the largest potential for optimization with regard to power and area efficiency, as spectral separation might not be required anymore.

Chapter 4

High voltage neural stimulator

This chapter discusses the design decisions and implementation of the neural stimulation unit and the HV interface, which is required to protect the recorder during stimulation events. The design process was started with the development of a HV CCS in a preceding master thesis [96] and fully developed during this Ph.D. thesis. In the first part the current stimulator and its interface to the neural recorder are described in detail and measurement results that prove the combined stimulation/recording capabilities are shown. Thereafter, a novel, semi-digital feedback architecture that allows the reconfiguration between voltage and current mode is discussed in theory, its transistor level implementation is shown and measurement results are presented.

4.1 Constant current stimulator

This section describes the fully integrated, biphasic current mode stimulator, which was developed for the bidirectional, multichannel neural interface. It consists of a HV output stage, that is operated from a $\pm 9\,\mathrm{V}$ supply, in order to provide sufficient voltage compliance, even for high impedance electrodes. On-chip waveform synthesis is realized with a 5 bit current steering DAC, whose dynamic range is extended by a selectable output range which is realized as a variable gain current mirror. The stimulator achieves a maximum stimulation current of $\pm 10.2\,\mathrm{mA}$ with a measured voltage compliance of $\pm 8\,\mathrm{V}$ and a dynamic range of $50\,\mathrm{dB}$.

4.1.1 Voltage domains

When looking into the SoA for neural stimulators, maximum output currents in the range of $0.5\,\mathrm{mA}$ up to $15\,\mathrm{mA}$ [21, 44, 55, 97] can be found for integrated systems and

commercially available systems like the Medtronic Activa™ product series even offer maximum currents up to 25.5 mA [50]. At the same time, bio-impedances are usually reported with R_S in the range of several kΩ and a C_{DL} of around 10 nF-100 nF [86, 95], which is in good accordance with our impedance estimations presented at the end of chapter 3. If we assume, that during a safe stimulation only non-Faradic reactions take place and therefore only a negligible amount of current flows through R_{CT} (c.f. section 2.2), the following electrode voltage V_{El} can be calculated for a 200 µs/0.5 mA rectangular stimulation pulse.

$$V_{El} = \frac{I_{Stim}T_{Stim}}{C_{DL}} + I_{Stim}R_S = \frac{0.5\text{mA} \cdot 200\mu\text{s}}{100\text{nF}} + 0.5\text{mA} \cdot 10\text{k}\Omega = 6\text{V} \qquad (4.1)$$

Where $R_S = 10\,\text{k}\Omega$ and $C_{DL} = 100\,\text{nF}$ are estimates taken from [86]. This simple calculation makes it obvious, that a precise CCS requires a voltage compliance, which is above standard CMOS supply levels to achieve the aforementioned stimulation currents. Since, it is not possible to build a power efficient recorder with such a high voltage supply, as power consumption rises with increasing supply voltage and bulky HV transistors have to be used, the design is split up in a HV stimulator part and a LV recorder part.

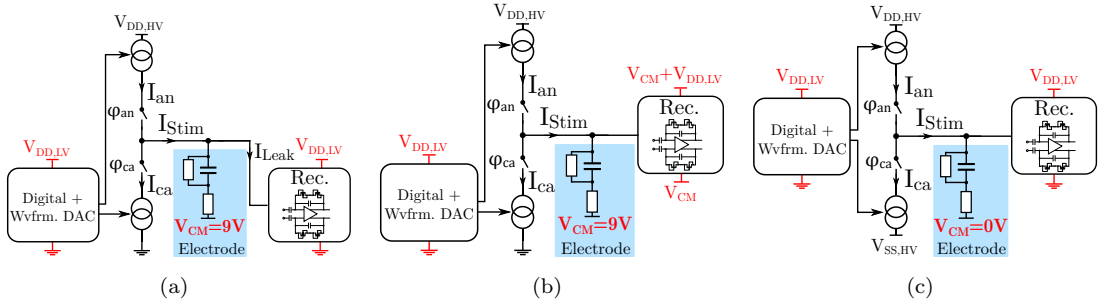


FIGURE 4.1: Evaluated approaches for the LV supply domains.

At the beginning of the stimulator design, three approaches for the split domains shown in Figure 4.1 were considered, which is in detail discussed in [96]. The first options (a) and (b) are directly derived from the design presented in [73]. Both use a unipolar HV supply $V_{DD,HV}$ and achieve biphasic stimulation currents by setting the resting potential of the electrode to $V_{CM} = V_{DD,HV}/2 = 9\,\text{V}$. If only the stimulation unit is considered, this supply approach yields higher area and power efficiency compared to (c), which is why it was chosen in the epiretinal stimulator in [73]. However, the approach suffers from major drawbacks if a bidirectional interface is required. The first implementation (a) requires the input capacitors C_{in} to block a DC voltage of $V_{DC} = V_{CM}$ - $V_{DD,LV}/2 = 7.5\,\text{V}$, which exceeds the specified limits of the high capacitance MIM capacitors in the used technology and would thus require the use of capacitors with a worse capacitance per area. Since C_{in} is the main area consumer in the LNA, as explained in chapter 3, this

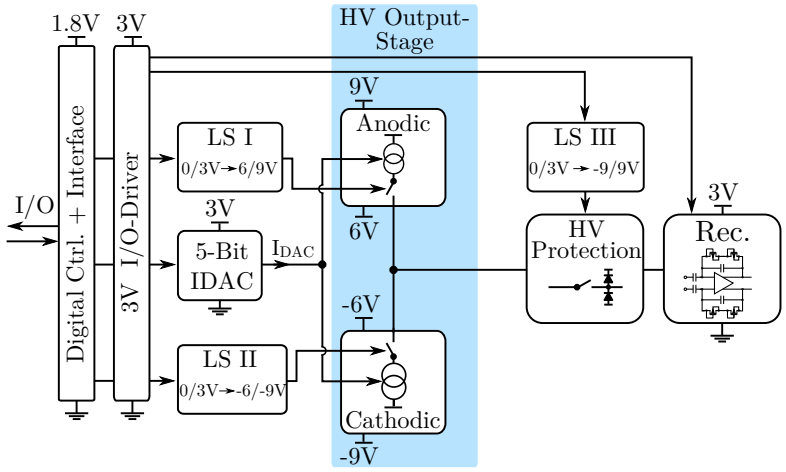


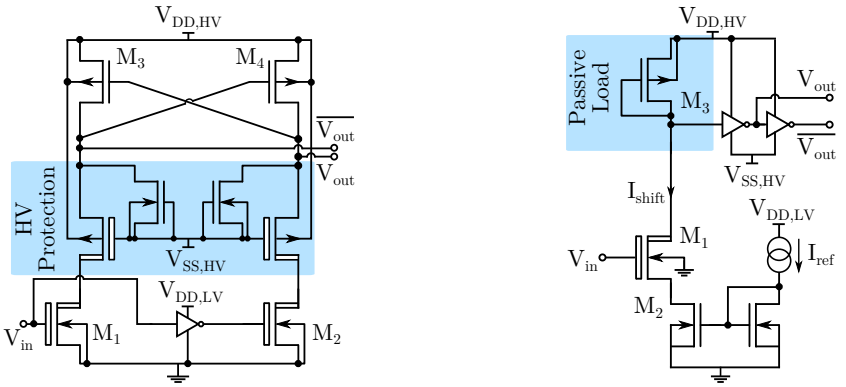
FIGURE 4.2: Block diagram of the bidirectional neural front-end using floating voltage domains.

would result in a large area penalty. Shifting the recorder into a floating voltage domain with V_{CM} as reference potential circumvents this problem, as shown in (b). However, this approach has the problem, that now the digital supply levels and the LV recorder supply have different references, which requires level shifting between the domains. This would still be possible for the static set-up bits of the stimulator with little power penalty by using the technique proposed in [73], but the shifting of the clock signals for the SC filters would already cause an intolerable increase in power consumption.

Because of the aforementioned issues, the implementation shown in (c) was used to realize the current stimulator. Here a bipolar HV supply with the negative voltage $V_{SS,sub}$ below the LV ground and the positive supply $V_{DD,HV}$ is used to allow biphasic stimulation and the resting potential of the electrode is at $V_{CM} = 0\,V$. It is realized by putting the LV circuitry in a shared, floating deep n-well and avoids level shifting, since the same reference is used for the LV recorder and the digital circuitry. Figure 4.2 shows the block diagram of the implemented stimulator, with the different voltage domains. Starting from the left, a 1.8 V digital core voltage is used for off-chip communication and stimulation control, which is shifted to the 3 V analog LV domain using Level Shifter (LS) from the standard cell library. A 5 bit current steering DAC in the LV domain is used to synthesize an arbitrary waveform, which is driven into the electrode by a biphasic HV output stage. Additional LS are needed to provide control signals for the floating output drivers and the HV protection circuitry. All illustrated blocks will be explained in detail in the following.

4.1.2 Digital level shifters

The use of multi supply domains is a common approach in integrated circuits that require a HV supply but has a limited power budget. By implementing floating voltage domains, individual circuitry can be operated from a LV supply with a floating reference, like the anodic and cathodic output stage in Figure 4.2, thus reducing the power consumption compared to the use of the full supply range. Since control signals need to be available in the floating domain as well, LS circuits are required that translate between one and another domain. Especially in biomedical implants, this can be a limiting factor due to the strict area limitations [32].



(a) Dynamic LS with cross coupled transistors, derived from [98].

(b) Static LS with pMOS diode load.

FIGURE 4.3: Evaluated approaches for the LV supply domains.

LS implementations can be divided into two main categories, dynamic LS and static LS [99]. In dynamic LS a cross coupled transistor pair is used to form positive feedback, which generates a bi-stable output stage [98]. Figure 4.3 (a) shows a possible implementation that uses two HV nMOS input transistors and the LV pMOS cross coupled pair. By inserting the highlighted HV protection, the output voltage can never drift lower than one diode voltage below $V_{SS,HV}$, which allows the use of LV devices $M_{3/4}$ and results in faster transition times. The advantage of this structure is, that no static current is consumed from the HV supply, independent of the input signal V_{in}. However, this maximum power efficiency comes with drawback that a higher area is needed, as four HV devices are required to form one LS.

Figure 4.3 (b) shows a static LS, which requires only one HV transistor M_1, that is used to switch the nMOS current source M_2. The voltage drop over the passive load element in the floating domain, in this case a pMOS diode, can then be used as the shifted output signal. In order to get clean, digital output signals two additional inverters were installed in the floating domain. However, the drawback of this circuit is, that a constant current flows from $V_{DD,HV}$ to ground, as long as V_{in} is in the high state. Since this voltage

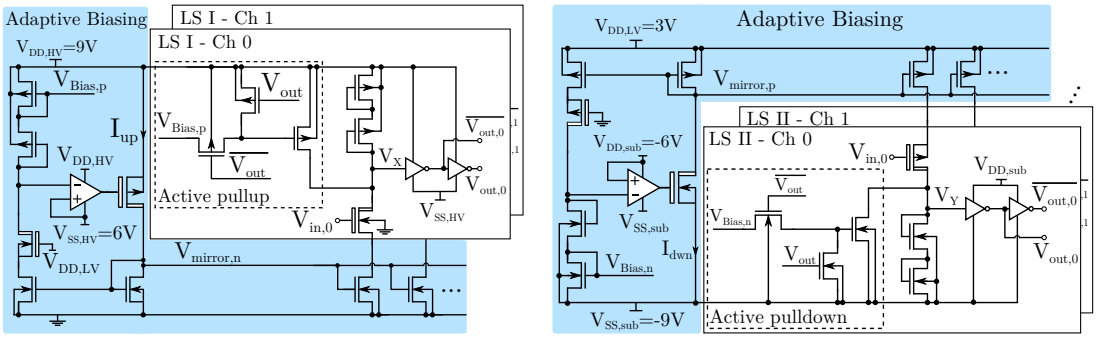


FIGURE 4.4: Static LS with adaptive bias generation, derived from [15].

drop is usually quite large, already small currents cause a significant power dissipation. These two characteristics, maximum area efficiency but static power consumption, make the approach suitable for applications where a large number of signals with small duty cycles need to be shifted. As stimulation events may only occur in a very limited share of time in order to avoid tissue damage, this approach is very well suited for the tasks of LS I&II in Figure 4.2.

A remaining issue of the static LS is, that the current source I_{ref} must match the passive load, such that the input of the first inverter reaches $V_{SS,HV}$. As this voltage drop changes with process, temperature and aging, this signal is only poorly defined, which can cause large static currents in the first inverter. To avoid this issue we implemented two adaptive, on-chip biasing circuits, that we presented in [15]. Figure 4.4 shows the two biasing circuits and the corresponding LS for shifting into the $+6/9\,V$ and the $-6/-9\,V$ domain.

In order to adjust the biasing currents I_{up}/I_{down}, two differential amplifiers in the corresponding, floating domains are used to adjust the gate voltage of a HV MOS transistor, forming a regulated current source. This current is mirrored back into the left branch, which represents a replica of the actual LS channels, consisting of two stacked diodes as the passive load element, a HV cascoding transistor and a LV current source. Since the differential amplifiers have $V_{SS,HV}$ / $V_{DD,sub}$ as a reference, the feedback loop will adjust I_{up}/I_{down} until the voltage drop across the load replica is equal to the floating supply, adapting the biasing current to process, temperature and supply variations. The generated current is then provided to each LS channel using a LV current mirror, which allows to use one shared biasing circuit for all 32 stimulator channels, making the area and power overhead negligible.

The diode stack is designed to have a nominal current of $2\,\mu A$, which can be adjusted over the diode length. When designing the current through the diodes it has to be

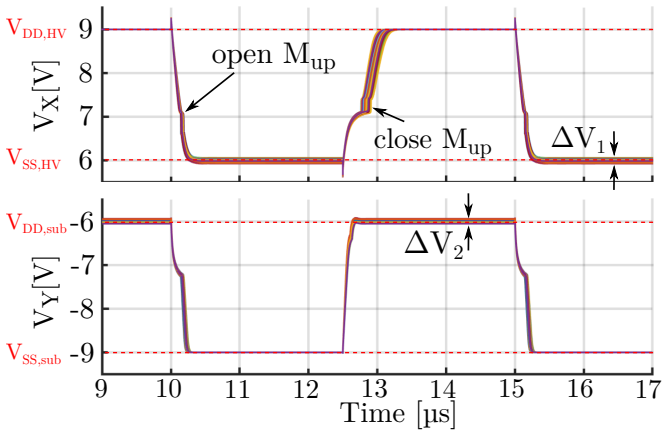


FIGURE 4.5: Monte Carlo simulation with 200 runs of the LS to evaluate device mismatch.

considered, that a higher current results in faster switching times, but increased power consumption as well. For the differential amplifier a single-stage OTA with current mirror load was chosen, which results in an overall power consumption for the reference generation of 40 µW for the shift into the higher voltage domain and 54 µW for the lower voltage domain. Both biasing circuits together require an active area of 137 µm x 97 µm and each LS channel roughly 2000 μm^2.

Figure 4.5 shows the transient input voltage of the first inverters $V_{X/Y}$ over 200 Monte-Carlo runs with a 200 kHz square wave input signal in the LV domain. It can be seen, that $V_{X/Y}$ settle to the floating, digital levels with high accuracy. Due to mismatch between the replica load and the diodes in the LS, a variation of $\Delta V_1 = 130\,\text{mV}$ around $V_{SS,HV}$ can be observed when shifting the signal up and a similar variation of $\Delta V_2 = 110\,\text{mV}$ around $V_{DD,sub}$ when shifting down. Additionally the switching of the active pullup transistor M_{up} is indicated, which is added to the LSs in order to increase the transition speed [98].

Since the HV interface requires additional control signals in the -9/+9 V domain, which will be explained in section 4.2, the full scale LS shown in Figure 4.6 was implemented. It consists of a combination of static and dynamic LS, as it uses the previously described static LS to translate the LV input signal into the -9/-6 V domain, were it is used to drive the input of a dynamic LS, realized as a latch. This design is chosen, as a static LS is not beneficial in this case, since the passive load and the following inverters would have to be HV compliant, resulting in a larger number of HV devices than the presented solution, while still requiring static current.

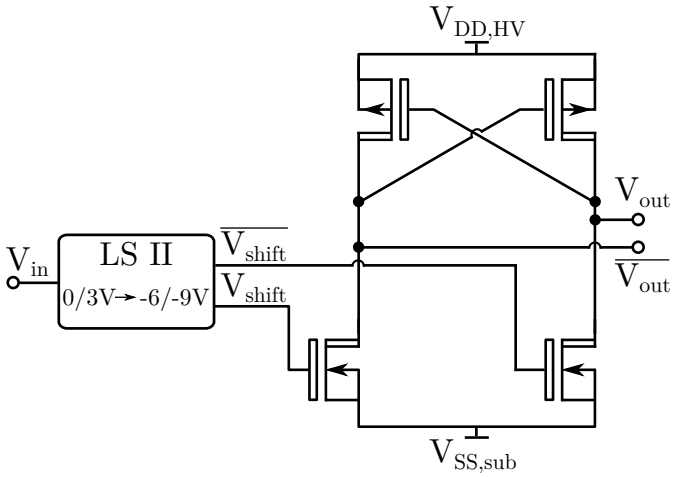


FIGURE 4.6: Digital LS from 0/3 V to -9/+9 V (LS III).

4.1.3 Current steering DAC

In order to provide maximum flexibility to the stimulation waveform, a current steering DAC is used in the LV domain to synthesize arbitrary stimulation waveforms. A moderate resolution of 5 bit was chosen, since it allows to realize the DAC with binary weighted current sources, as shown in Figure 4.7, without limitations due to device mismatch. This results in a compact design, which can be directly controlled by a simple binary input code [100].

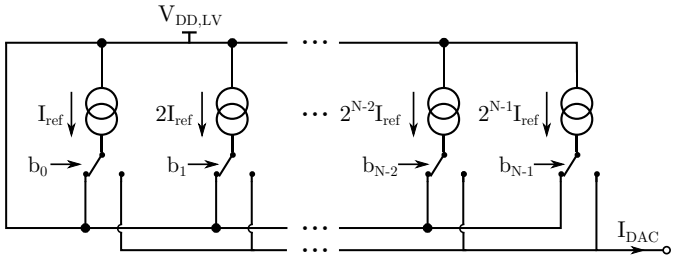


FIGURE 4.7: N bit current steering DAC with binary weighted current sources.

The DAC was implemented with a Least Significant Bit (LSB) current of 3.2 µA, which results in a maximum output current of 100 µA. To further increase the DR, a variable gain stage provides an adjustable gain of 1x, 2x, 5x or 10x, resulting in a DR of 50 dB, which is required to increase the stimulators flexibility.

Figure 4.8 shows the transistor level implementation of the current steering DAC, together with the variable gain current mirror. The highlighted DAC is realized with cascoded current sources to improve its linearity. In order to achieve good matching between the reference and the binary current sources, M_{0m} and M_0 are biased in strong inversion with an aspect ratio of $(W/L)_{M0} = (2.2\mu m/20\mu m)$. All other current sources M_i are realized as multiples of M_0 with 2^i elements to achieve binary scaling. Since matching

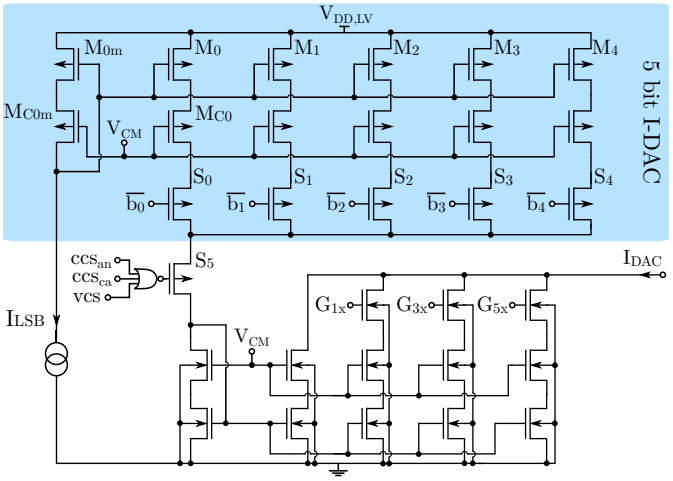
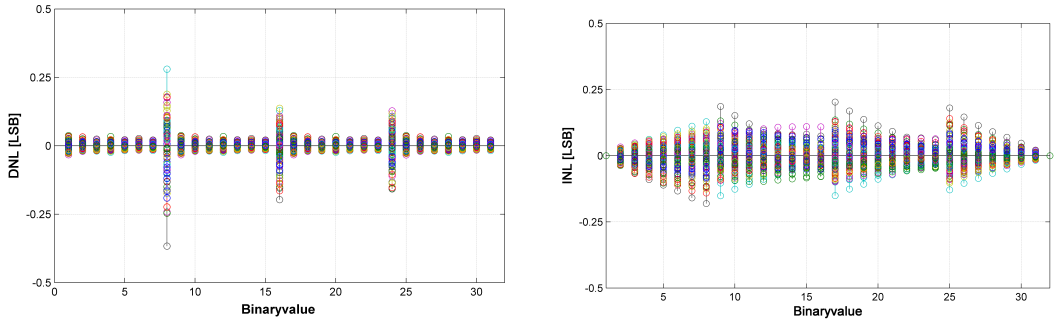


FIGURE 4.8: 5 bit current steering DAC with variable gain current mirror.

is less critical for the cascoding devices C_i, they can be sized to $(W/L)_{MC0} = (3\mu m/500nm)$, which results in the same overdrive voltage, but a reduced active area and the uncritical switches S_i are realized with minimum length devices. The additional output switch S_5 is installed to shut down the DAC current if no stimulation is active, in order to reduce the LV power consumption.



(a) Differential non-linearity (DNL)

(b) Integrated non-linearity (INL)

FIGURE 4.9: Simulated DNL and INL of the 5 bit I-DAC (200 Monte Carlo runs).

Figure 4.9 shows the DNL and INL of the DAC, which both stay below ±0.5 LSB, meaning the DAC achieves the desired resolution and is strictly monotonic. Additionally, the aforementioned disadvantage of the chosen architecture can be seen in the big DNL values at e.g. 8 and 16, which are caused by the binary scaled current sources. However, the simulation showed, that the architecture provides sufficient resolution, making it the best trade-off with respect to area and complexity.

4.1.4 HV output stages

Figure 4.10 shows the biphasic, HV output stage of the current stimulator, where the previously described DAC and variable gain current mirror have been replaced by the adjustable current source I_{DAC}, to improve readability.

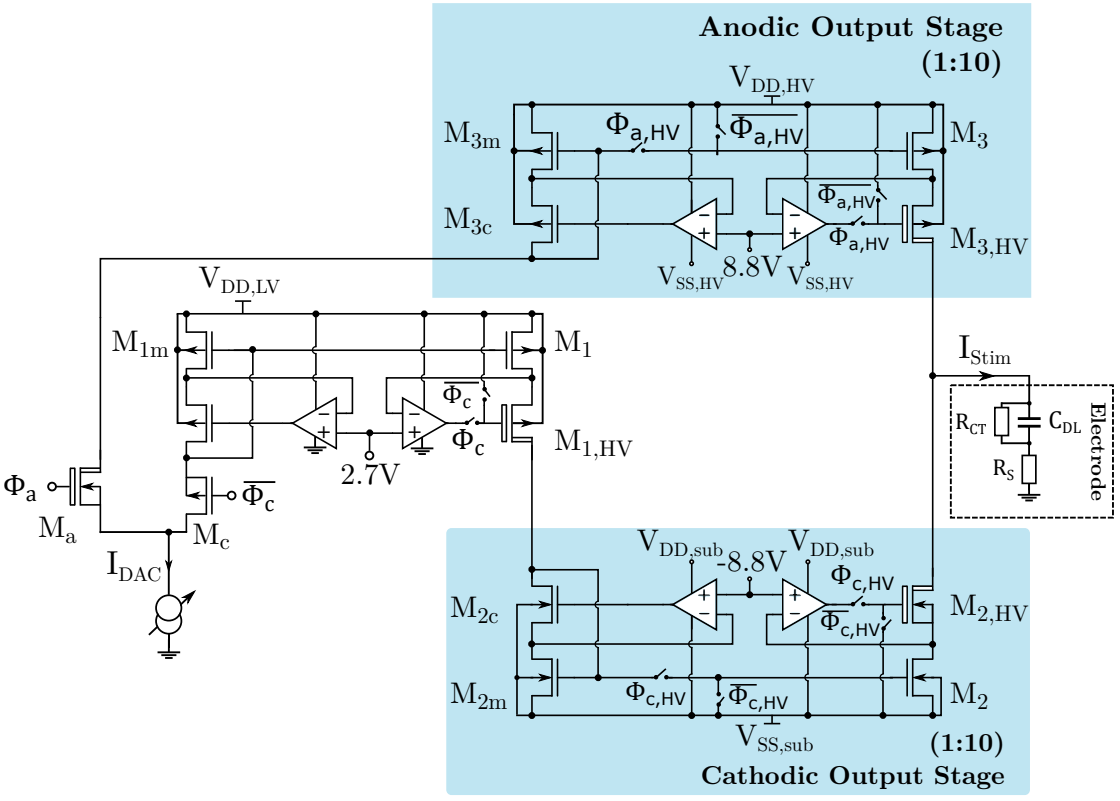


FIGURE 4.10: Biphasic, HV output stage of the current stimulator, derived from [16].

The stimulation polarity is set by the active high, digital control signals Φ_a and Φ_c in the $V_{DD,LV}$ (0/3 V) domain, which are translated into the according HV domain by the LS circuits presented in section 4.1.2. The digital control logic must ensure, that Φ_a and Φ_c are not active at the same time, since this would cause concurrent stimulation currents.

During anodic stimulation Φ_a is in the high state ($3\,V = V_{DD,LV}$), which puts M_a into the saturation region, thereby acting as a HV cascode. This protects the LV variable gain current mirror from harmful voltage levels, as the source of M_{an} can not rise above $V_{DD,LV}$. The reference current I_{DAC} flows through M_a into the floating, anodic output stage, where transistors M_{3m} and M_3 mirror it into the HV output branch with a gain of 10. This enables a maximum stimulation current of 10 mA, while reducing the power loss, which is caused by the current I_{DAC} in the HV reference path.

The output current mirror is realized as a regulated cascode for two reasons. First, this gain boosting allows an asymmetric design with a LV cascoding transistor in the reference

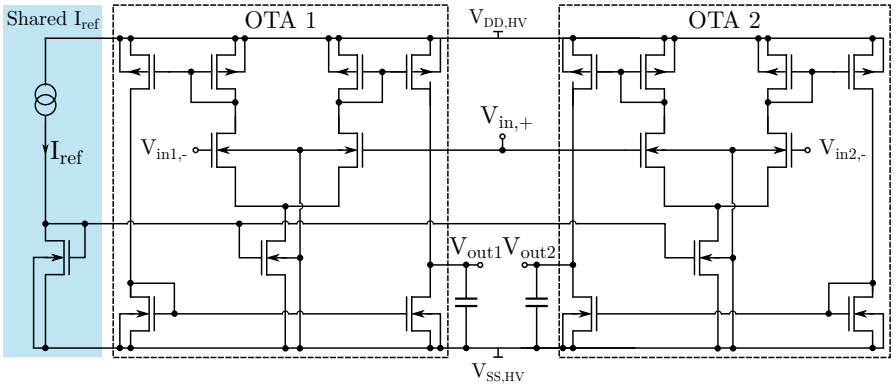


FIGURE 4.11: Dual differential amplifier of the anodic output stage.

path and a HV cascoding transistor in the output path. Since M_{3c} is intrinsically protected by the diode connection of M_{3m} and the by design limited reference current I_{DAC}, an area efficient LV pMOS can be used. In contrast to that, $M_{3,HV}$ must be able to withstand the full supply range, as the stimulator output is a high impedance node, which can reach both supply rails for high impedant loads. Without regulating the sources of the two fundamentally different cascoding transistors, a large current mismatch would result due to the large difference in threshold voltage of a HV and a LV MOS device. The second reason for a regulated cascode is that it can be used to achieve high voltage compliance even for large currents, thus achieving good power efficiency [73]. The high compliance is attained by putting the reference of the two differential amplifiers only 200 mV below $V_{DD,HV}$, which leaves maximum headroom to the cascoding transistor $M_{3,HV}$. For small currents, M_3 and M_{3m} stay in saturation and form a cascoded current mirror with active gain boosting. If the stimulation current is increased, M_3 and M_{3m} will enter triode region, where they act as voltage controlled resistors. Since both transistors have the same V_{GS} and their V_{DS} is regulated to the same value, a good matching between the currents is achieved [101].

Figure 4.11 shows the implementation of the dual differential amplifier used in the anodic output branch. In order to safe power and increase the matching, both amplifiers share one reference current and have a common $V_{in,+}$ input. A symmetrical, single stage amplifier has been used, as it achieves a sufficient DC gain of $A_0 = 62$ dB and gain bandwidth of 2.7 MHz. Since the desired common mode is only 200 mV away from the positive supply, a nMOS input pair has been chosen. The same architecture is used for the two dual differential amplifiers in the cathodic current path. However, the floating amplifiers in the cathodic output stage are realized with a pMOS input pair, since their common mode voltage is 200 mV above the negative rail. Table 4.1 summarizes the key parameters of the used amplifiers. Both versions have been implemented with relatively large input devices, in order to reduce the offset due to mismatch in the input pair, since this determines the current mismatch for large output currents.

NMOS Input stage		**PMOS Input stage**	
$(W/L)_{in}$	$\frac{7\mu m}{2.2\mu m}$	$(W/L)_{in}$	$\frac{8\mu m}{0.8\mu m}$
C_{Out}	100 fF	C_{Out}	200 fF
A_0	60.3dB	A_0	61.6dB
GBW	2.7MHz	GBW	1.6MHz
I_{tot}	$6.2\mu A$	I_{tot}	$5\mu A$

TABLE 4.1: Design parameters of the dual differential amplifiers.

During cathodic stimulation Φ_c is active, allowing I_{DAC} to flow through M_c into a first regulated current mirror, which copies it into the cathodic output stage. Here it is essential to regulate the drains of the mirroring transistors M_{1m} and M_1 in order to achieve good matching, because of the asymmetric design and te big difference in the voltage drop over the mirroring branches. The cathodic output stage is built up analog to the anodic side.

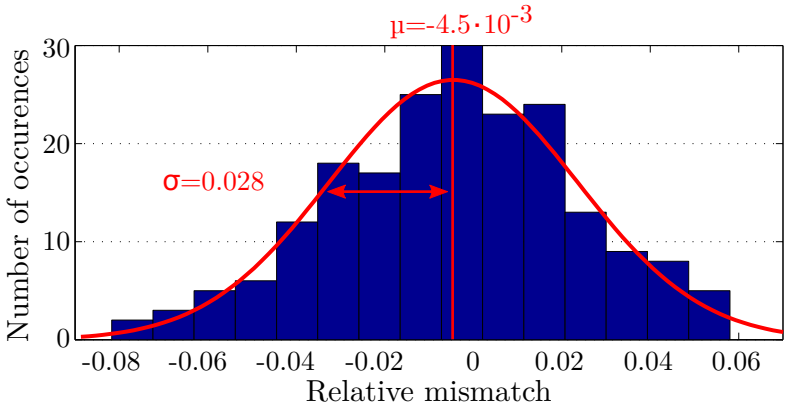
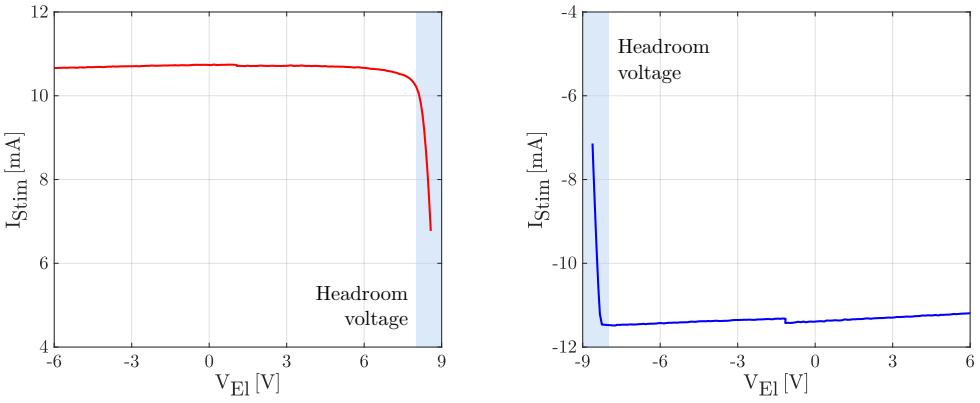


FIGURE 4.12: Relative mismatch of anodic/cathodic stimulation current for $I_{Stim} = \pm 10.2\,mA$.

Figure 4.12 shows the simulated histogram of the current mismatch between anodic and cathodic current for the maximum stimulation current of 10.2 mA. Since the mismatch during maximum stimulation strength leads to the largest, absolute charge accumulation on the electrode, this represents the worst case estimation. A Gaussian distribution has been fitted with a mean of $\mu = -4.5 \cdot 10^{-3}$ and a standard deviation of $\sigma = 0.028$. The high matching reduces the remaining charge on the electrode after a stimulation, which allows to keep the passive discharge period short and record fast after a stimulation [16].

In order to measure the voltage compliance of the recorder, the output voltage of the stimulator V_{El} and the stimulation current through a 100 Ω resistor were measured, using the National Instruments PCIe-6363 multifunction I/O device [102]. The result is



(a) Anodic voltage compliance (b) Cathodic voltage compliance

FIGURE 4.13: Measured anodic/cathodic voltage compliance.

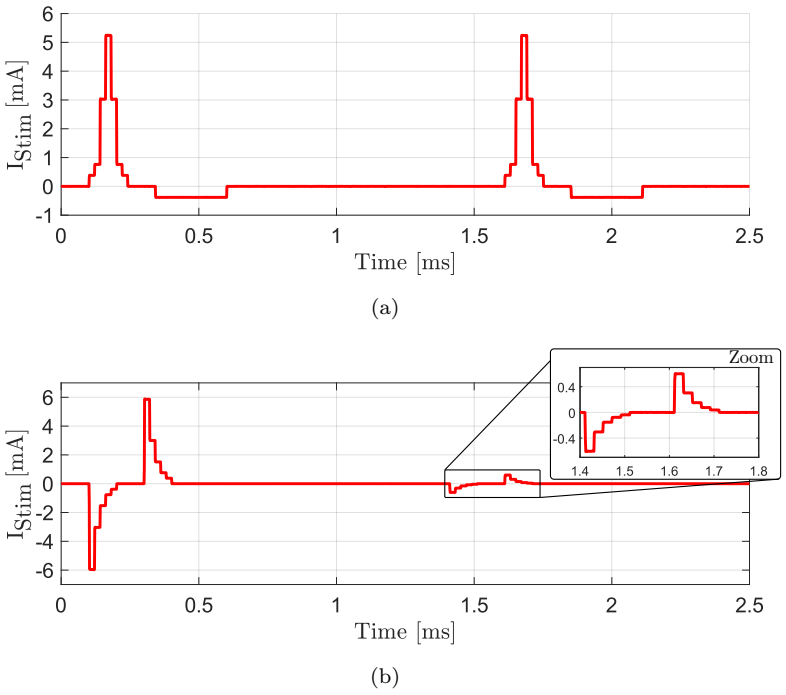


FIGURE 4.14: Measured stimulation waveforms using a 100 Ω dummy load.

plotted in Figure 4.13, which shows a required headroom voltage of 1 V in anodic and cathodic mode for the full scale current, resulting in a voltage compliance of ±8 V.

Figure 4.14 shows two measured stimulation waveforms that were generated with the presented CCS and an external, digital control unit that provided the waveform information. The shown results were acquired by sampling the voltage drop over a 100 Ω dummy load with a 100 kS/s ADC. The first waveform shows an anodic first, biphasic stimulation, with a Gaussian formed anodic pulse, followed by a rectangular, cathodic pulse. The second waveform shows two biphasic, exponentially decaying stimulations

with different amplitudes. Both waveforms illustrate the possibility of generating arbitrary stimulation patterns, when using the on-chip 5 bit I-DAC with variable, transient input codes. Additionally (b) demonstrates the increased dynamic range, realized by the variable gain current mirror. Table 4.2 summarizes the key parameters of the presented current stimulator.

	This work
Stimulation type	Biphasic CCS
Supply voltage	$\pm 9\,\mathrm{V}$
Voltage compliance	$\pm 8\,\mathrm{V}$
Maximum stim. current	$\pm 10.2\,\mathrm{mA}$
Dynamic range	$50\,\mathrm{dB}$
Standby power	$80\,\mu\mathrm{W}$
Waveform generation	On-Chip 5 bit I-DAC

TABLE 4.2: Parameters of the presented CCS.

The listed standby power is only valid if the stimulator is in standby during an active stimulation events (e.g. during the inter pulse delay). This means no stimulation current is currently driven into the electrode, but a stimulation is running. If the bidirectional channel is in recording mode, as it is most of the time, the stimulator is put in sleep mode by shutting down all biasing currents. This results in a negligible, remaining power consumption, which is only caused by leakage currents.

4.2 High voltage recorder interface

During stimulation events, the electrode potential can easily exceed the $0/3\,\mathrm{V}$ supply range of the LV neural recorder, depending on the electrode impedance and stimulation intensity. This can lead to potentially harmful voltage levels at the recorder, leading to accelerated aging due to stressed input devices, or even instantly damage the sensitive recorder input. Previous work has shown that HV transistors can be used to disconnect the recorder before the beginning of a stimulation event, thus protecting it from said over-voltage scenarios [55, 103]. Besides the explained safety reasons, a second reason to use such active blanking is the reduction of stimulation artifacts. Even if a stimulation would cause harmless electrode voltages, the resulting signal amplitudes would drive the recorder into saturation, because of its high gain. Since the neural recorder has a high-pass corner frequency in the sub-Hertz range, it would take several seconds for it to recover, thus leading to an unacceptable blind time after a stimulation event.

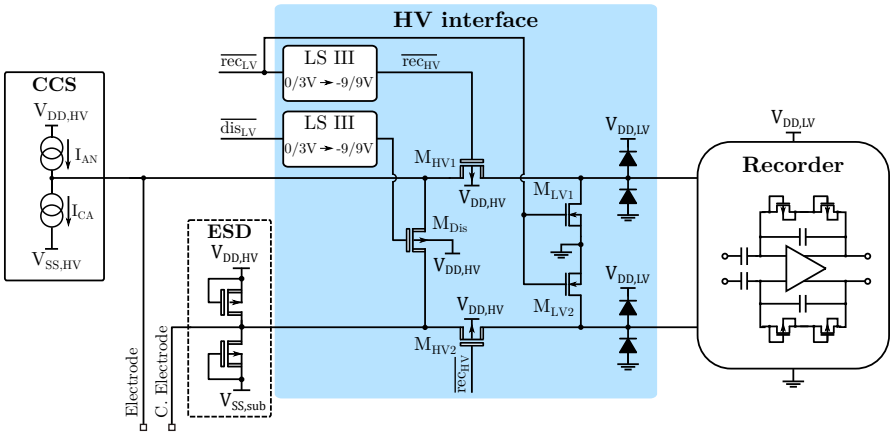


FIGURE 4.15: HV compliant recorder interface.

Figure 4.15 shows the implementation of the HV interface. Two HV pMOS transistors $M_{HV1/2}$ are used to disconnect the recorder from the electrode and the counter electrode during stimulation events. Two additional LV nMOS transistors $M_{LV1/2}$ actively pull the recorder inputs to ground, which further suppresses stimulation artifacts that could otherwise capacitively couple into the high-ohmic recorder input. A third HV pMOS transistor M_{Dis} is installed before the blanking switches between working and counter electrode to provide passive charge balancing.

In [103] and [12] it has been shown, that the HV transistor switches are critical, since their noise contribution will deteriorate the recorders noise performance. As both switches are the first elements in the recording chain and do not offer signal gain, their integrated noise $V_{rms,HV}$ adds to the integrated, input referred noise of the LNA $V_{rms,LNA}$ as follows.

$$V_{rms,tot} = \sqrt{V_{rms,LNA}^2 + V_{rms,HV}^2} \tag{4.2}$$

Since both HV transistors are operated as switches, they are supposed to be biased in the linear region. Therefore, their thermal noise density $\overline{dv_{HV}^2}$ is determined by the on resistance R_{on} [90].

$$\begin{aligned} \overline{dv_{HV}^2} &= 4kTR_{on}df \\ R_{on} &= \frac{1}{\beta_0 \frac{W}{L} \cdot (V_{GS} - V_{th})} \end{aligned} \tag{4.3}$$

Where W is the transistor width, L is the transistor length, β_0 a process dependent scaling parameter and (V_{GS}-V_{th}) the overdrive voltage. Since the noise bandwidth is

determined by the recorder bandwidth, the integrated noise, which is added by the switches, can only be reduced by lowering R_{on}, which results in two design choices. First a full scale LS is used, which provides a $V_{DD,HV}$ to the HV pMOS gates in the case of stimulation, to disconnect them for all possible electrode voltages and -9 V in the recording state in order to achieve the maximum overdrive voltage. Second is that a good trade-off has to be found between the width W of the switches and their area consumption. To determine an adequate size, a detailed noise analysis of the switches was carried out during the first design, described in [12], resulting in a width of 286 µm for the minimum transistor length of 1.8 µm. The chosen size resulted in a simulated input referred noise of 200 nV, which is well below the noise of the LNA and no performance deterioration could be observed in measurements. Since the existing circuit provided sufficient performance, the same sizing was used in this work.

The LV switches $M_{LV1/2}$ are less critical in terms of noise. Since they are opened during stimulation, they only contribute 1/f noise by the reverse biased drain bulk diode. In order to reduce this noise contribution, the width of the transistor must be increased, as this increases the effective diode area. The same considerations hold for the protection diodes towards $V_{DD,LV}$ and ground, which requires them to be larger than the minimal size. A transistor width of 20 µm and a diode area of 58 μm^2 resulted in a simulated noise contribution in the sub percent range.

The circuit is protected against Electrostatic Discharge (ESD) events by two additional HV MOS diodes towards $V_{DD,HV}$ and $V_{SS,sub}$ at the counter electrode. Since the output devices of the CCS provide large, intrinsic diodes towards $V_{DD,HV}$ and $V_{SS,sub}$, no explicit ESD protection is required at the working electrode.

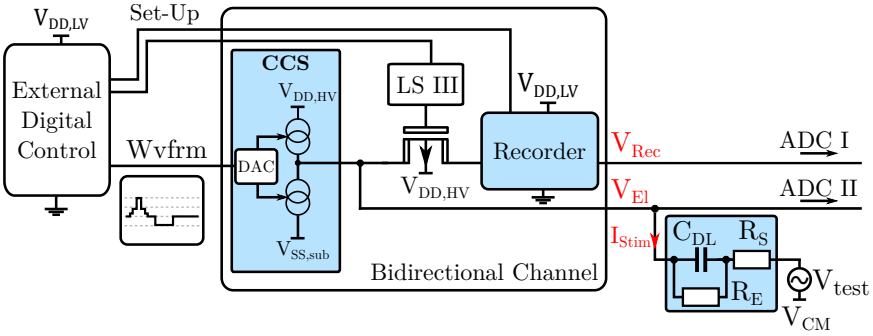
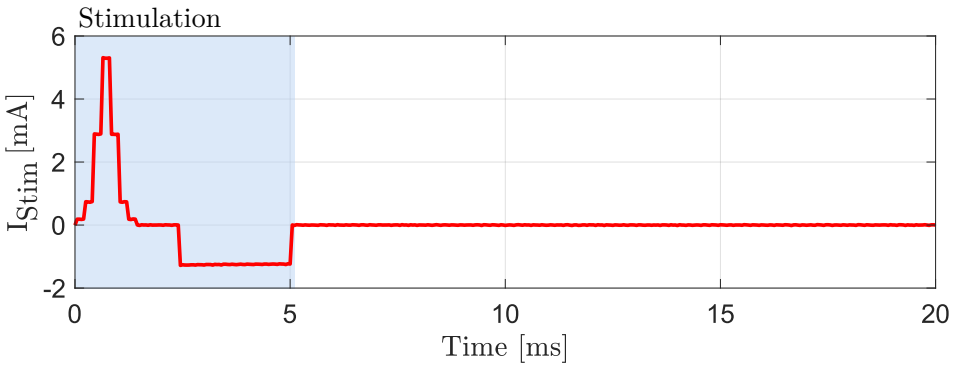
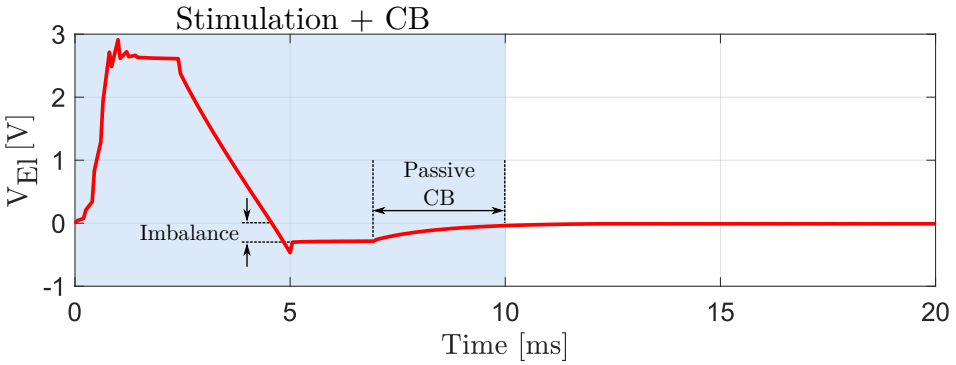


FIGURE 4.16: Measurement set-up to evaluate combined recording/stimulation.

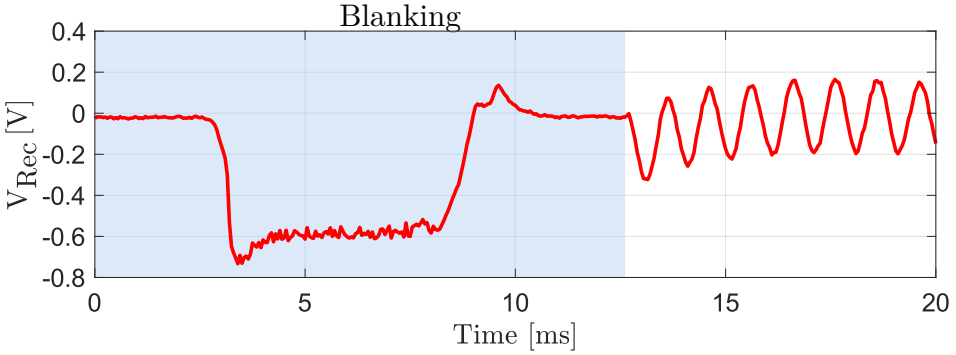
Figure 4.16 shows the test set-up used to evaluate the combined stimulation/recording capabilities, where a stimulation process is applied to a lumped element, Randles Cell model ($C_{DL} = 1\,\mu F$, $R_S = 100\,\Omega$, $R_{CT} = 1\,M\Omega$). To record the stimulation current, the voltage drop over an additional 100 Ω resistor in series to the electrode model was measured, which is not shown in Figure 4.17. Two external, 16 bit ADCs with variable



(a) Stimulation current



(b) Electrode voltage



(c) Recorder output

FIGURE 4.17: Measured stimulation with intentional charge mismatch, passive charge balancing and subsequent recording.

input range were used to sample the recorder output V_{Rec} and V_{El}. The signal source V_{test} generates a 1 kHz, 200 μV_{pp} sinusoidal test signal at the electrode model. An external, digital control unit is used to select only the AP channel of the recorder, with a configured gain of 68 dB and a high-pass cutoff frequency of 100 Hz.

Figure 4.17 shows the acquired waveforms of the recorder output V_{rec}, the electrode potential V_{El} and the stimulation current I_{Stim}. In (a), I_{Stim} shows a Gaussian stimulation waveform in the anodic phase, with a maximum amplitude of 5.2 mA and a square wave

stimulation in the cathodic phase. The stimulation was intentionally designed to deliver asymmetric charge, to illustrate the effect of charge mismatch and passive Charge Balancing (CB). Looking at the electrode potential V_{El} in Figure 4.17 (b), it can be seen, that the anodic charge is not fully canceled, but a residual voltage of 300 mV remains on the electrode after the intentionally mismatched stimulation process. The remaining charge is then canceled by closing the passive CB switch, which results in an exponentially decaying electrode potential. During the stimulation process, blanking is activated, as shown in Figure 4.17 (c). However, due to the high channel gain, some stimulation artifacts are visible, but do not drive the recorder into saturation. 2.5 ms after the charge balancing the recorder is reconnected to the electrode and the amplified test signal is directly visible at the recorder output. The blind time could even be further reduced, as CB was not directly activated after the end of the stimulation, to visualize the residual voltage. This shows, that even for an intentional mismatch, small blind times can be realized with the fully integrated, bidirectional channel.

4.3 Constant voltage stimulator

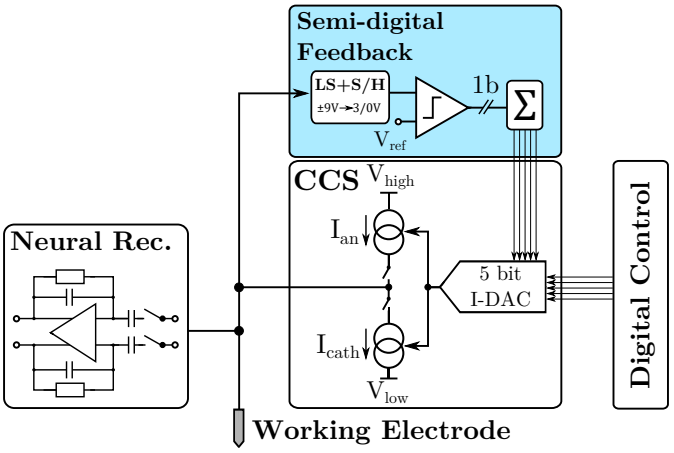


FIGURE 4.18: Neuromodulator with semi-digital feedback to realize CVS, derived from [14].

As it was described in the introduction, Constant Voltage Stimulation (CVS) is still quite popular amongst neurologists, since vast experience with (CVS) is available. Therefore, recent publications try to compare both methods against each other in terms of safety, stimulation efficacy and stimulation parameters [35, 84, 85]. This leads to the need for a reconfigurable current/voltage mode stimulator (CCS/CVS) to provide a powerful tool for the direct comparison of CCS to CVS. A first implementation of such a reconfigurable CCS/CVS stimulator was presented in [97]. However, this implementation used a resistive feedback Transimpedance Amplifier (TIA) to reconfigure the area consuming output stage of the CCS into CVS, which results in large static power consumption for

the voltage mode. Furthermore, stability issues can arise due to the capacitive nature of the electrode, which is connected to the input of the TIA.

Therefore, the idea of a semi-digital feedback loop was adapted, which was first presented in [76]. There it was used to reduce the power consumption of a CCS by controlling an adaptable HV supply voltage. In the newly developed design the TIA used in [76] is avoided, in order to mitigate stability issues. The stimulator uses the idea of semi-digital feedback to reconfigure the CCS into a class-B voltage stimulator as illustrated in Figure 4.18. This approach was first published in [14] and achieves high power efficiency as power consuming HV quiescent currents are avoided, as well as high area efficiency since most of the feedback can be realized in the digital domain. In the following, the system level architecture will be described together with a stability analysis of the feedback loop, followed by measurement results that were obtained with a first prototype.

4.3.1 System architecture

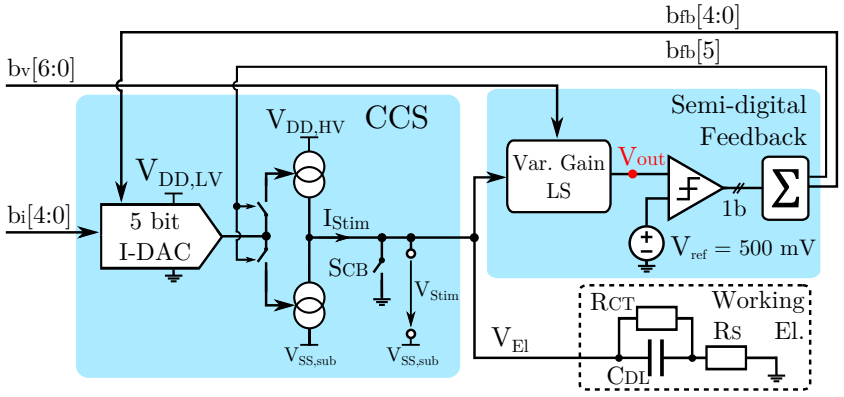


FIGURE 4.19: Block diagram of the voltage/current mode stimulator, derived from [17].

The block diagram in Figure 4.19 shows a more detailed view of the reconfigurable stimulator. In current mode operation the CCS described in section 4.1 is used, illustrated by the 5 bit current steering DAC in the LV domain and the HV output driver. Additionally, the passive CB switch S_{CB} from the HV recorder interface is shown, as it is used for on-chip calibration, which will be explained later. By placing the CCS into the shown semi-digital feedback loop, its output current is controlled to generate a constant output voltage at the working electrode.

Therefore, a variable gain level shifter is used to transfer the electrode potential from the ±9 V HV domain into the LV domain (0/3 V). This LS capacitively divides the electrode voltage into the LV domain, where it is compared against a fixed reference voltage $V_{ref} = 500\,mV$. The 1 bit decision is integrated by a 6 bit digital integrator,

whose output $b_{fb}[4:0]$ controls the current of the I-DAC and the MSB $b_{fb}[5]$ switches between anodic and cathodic current. Figure 4.20 shows the linearized, block-level model of the mixed-signal control loop. Therefore, the single bit quantizer is linearized with a gain of A_Q and the electrode is modeled with a reduced Randles cell electrode model, as the charge transfer resistance R_{CT} is neglected, assuming safe operation.

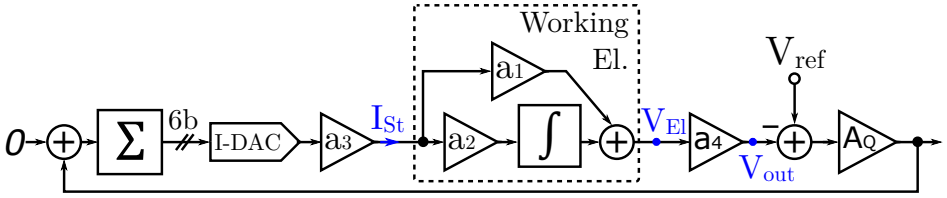


FIGURE 4.20: Linearized model of the CVS control loop, derived from [17].

The implemented control loop works similar to a second order ΣΔ Modulator (SDM) with a constant *'0'* at its input. The first integrator within the loop filter is the digital up/down counter that integrates the single bit comparator decision. Its output is converted into the stimulation current I_{St} over the I-DAC and gets integrated by the second integrator, formed by the double layer capacitance C_{DL}. Together with an additional, proportional part caused by the solution resistance R_S, this results in the electrode potential V_{El}, which is scaled by the gain of the capacitive LS a_4. In order to account for V_{ref} at the negative output of the comparator, an additional summation node is introduced before the quantizer gain. Since a stable ΣΔ loop regulates the input of its first integrator to zero over time, we can calculate backwards that the electrode voltage must be regulated to a value, that results in an output voltage of $V_{out} = V_{ref}$ of the variable gain LS.

This LS must provide two essential features to allow CVS. First it must change the reference potential of the stimulation voltage $V_{Stim} = V_{El} - V_{SS,sub}$ from $V_{SS,sub}$ = -9 V to ground (0 V) and second it must scale V_{Stim} with a digitally adjustable gain A_{LS}. If this is the case and we assume that the control loop works in the aforementioned manner, the electrode potential V_{El} calculates as followed.

$$\begin{aligned} V_{out} &= A_{LS} \cdot V_{Stim} = A_{LS} \cdot (V_{El} - V_{SS,sub}) \\ \Leftrightarrow V_{El} &= V_{SS,sub} + A_{LS}^{-1} \cdot 500\,\text{mV} \end{aligned} \tag{4.4}$$

Equation 4.4 shows, that V_{El} can now be set to the desired value, by adjusting A_{LS}. The required LS is realized as a capacitive, sampling LS, which is shown in Figure 4.21. It uses a clock frequency of $f_S = 1$ MHz, a reference capacitor size of $C_1 = 180$ fF and a binary scaled capacitor array that realizes the variable gain. The additional capacitor

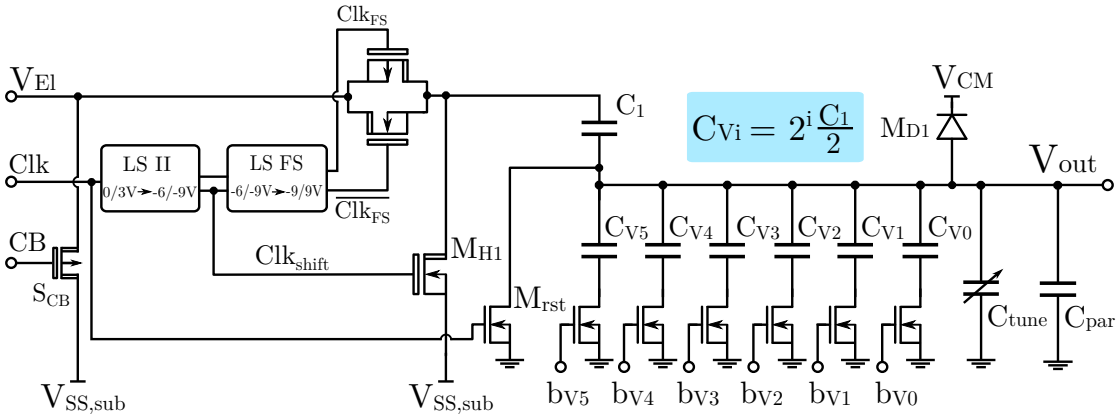


FIGURE 4.21: Variable gain LS with binary scaled C-array, derived from [17].

C_{tune} can be adjusted between 0 and C_1 and is realized with a 3 bit binary array. During initial calibration, the electrode is pulled to ground over S_{CB} and C_{tune} is stepped up until $C_{tune} + C_{par} = C_1$, to account for parasitics.

During CVS, the output node V_{out} is reset by discharging it to 0 V over the nMOS switch M_{rst} and the top plate of C_1 is reset to $V_{SS,sub}$ over M_{H1}, whenever the clock signal is high. In the sampling phase, when the clock signal is low, the electrode potential V_{El} is sampled on the top plate of C_1 and the output node V_{out} is high-ohmic. Therefore, V_{out} and the resulting LS gain A_{LS} can be calculated as a capacitive divider with the following, variable divider ratio.

$$\begin{aligned} V_{Out} &= \frac{(V_{El} - V_{SS,sub}) \cdot C_1}{C_1 + \sum_{i=0}^{5} b_{Vi} C_{Vi} + (C_{tune} + C_{par})} \\ \Rightarrow A_{LS} &= \frac{C_1}{2 \cdot C_1 + \sum_{i=0}^{5} b_{Vi} C_{Vi}} \end{aligned} \tag{4.5}$$

Where b_{Vi} is the 6 bit digital input word of the capacitor array. Since C_{Vi} is binary scaled relative to the reference capacitor C_1, the electrode potential can be calculated using Equation 4.4.

$$\begin{aligned} V_{El} &= V_{Out} \cdot \left(2 + \frac{n}{2}\right) - 9V \\ &= n \cdot 250\,mV - 8\,V \end{aligned} \tag{4.6}$$

This allows to adjust the electrode potential to a desired stimulation voltage, in minimum steps of 250 mV, with an output range of ±8 V. Thereby the explained architecture makes full reuse of the CCS and needs only one LS, a capacitive array and a comparator with adjacent digital integrator in the LV domain. This results in an area overhead

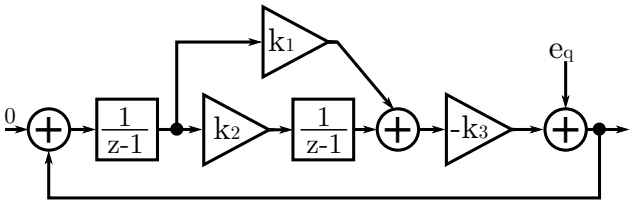


FIGURE 4.22: DT model of the CVS control loop.

of only 18.3 %, which will be shown in detail in section 4.4. Besides the high area efficiency the architecture achieves class-B operation, since no static bias currents in the HV domain are required as the output current is controlled digitally. Because of the large supply voltage of ±9 V small currents lead already to comparably large power consumptions, which emphasizes the high benefit of the proposed circuit.

4.3.2 Stability analysis

In the previous section it was assumed for the calculation of the electrode potentials that the feedback loop is operated in a stable condition. Since an unstable feedback loop would result in a direct hazard for the patient due to uncontrolled stimulation voltages, a detailed stability analysis was performed. Due to the aforementioned similarity of the control loop to a second order ΣΔ modulator, known concepts of SDM stability analysis can be applied.

As one method of stability analysis which is used within the literature of linearized SDM, the Root Locus Plot (RLP) can be applied [104–106]. Therefore, the mixed Discrete Time (DT)/Continuous Time (CT) loop was transferred into the DT model shown in Figure 4.22, using impulse-invariant transformation [104]. There, the single-bit quantizer has been replaced by the additive white quantization noise model (e_q) and a linearized quantizer gain A_Q, used to calculate k_3. This results in the following coefficients $k_{1/2/3}$, which can be used to calculate the complete open-loop gain A_{OL}.

$$k_1 = \frac{R_S}{V_{FS}/I_{FS}} \ , \ k_2 = \frac{1}{f_s \cdot C_{DL}} \frac{1}{V_{FS}/I_{FS}} \ , \ k_3 = A_Q A_{LS} \tag{4.7}$$

$$A_{OL} = \left(k_1 + \frac{k2}{z-1}\right) \cdot \left(\frac{-k_3}{z-1}\right) \tag{4.8}$$

where $V_{FS} = 9\,\mathrm{V}$ is the full scale output voltage and I_{FS} is the full scale output current of 1/2/5/10 mA, depending on the output range selection of the CCS, which was described in section 4.1.

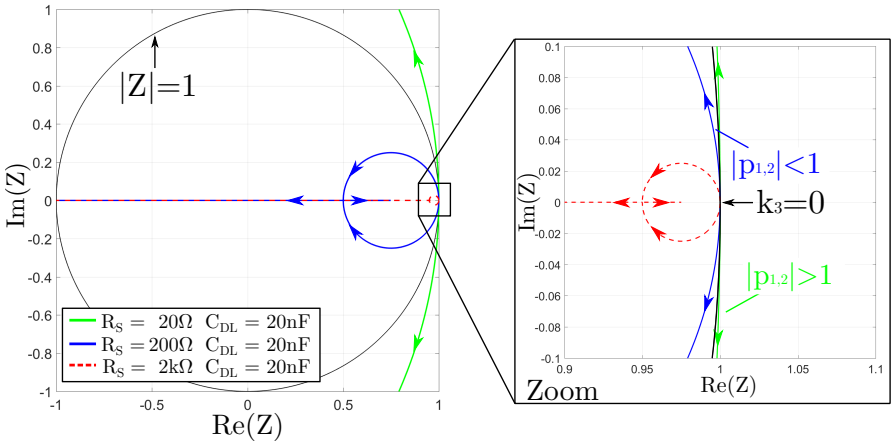
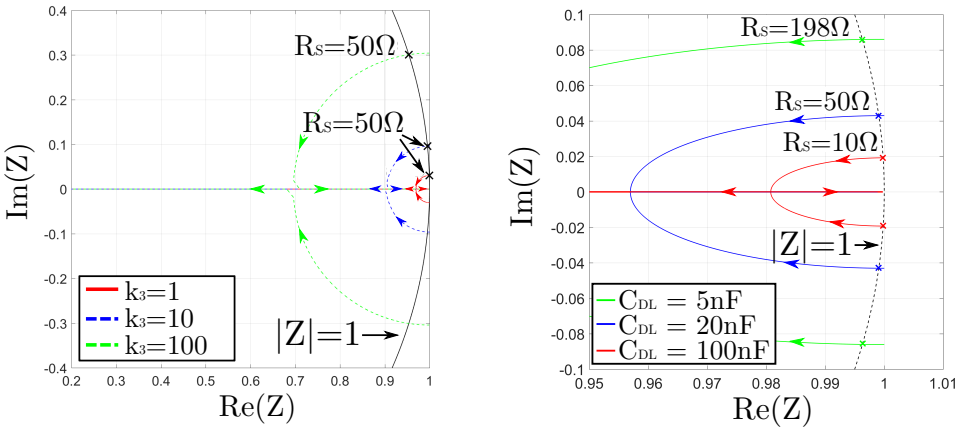


FIGURE 4.23: RLP over $k_3 = A_Q \cdot A_{LS}$ and parametrized electrode values [17].

Figure 4.23 shows the RLP, which is acquired by sweeping the parameter k_3 from 10^{-3} to 10^4 with 3 different combinations of C_{DL} and R_S. This sweep is important, as the quantizer gain A_Q itself is undefined in a single-bit quantizer (large differential input: $A_Q \to 0$, small differential input $A_Q \to \infty$) and the LS gain A_{LS} depends on the selected stimulation voltage. The result is the typical RLP of a second order SDM, where both poles start on the unit circle for quantizer gain of $A_Q = 0$, indicated by '$k_3 = 0$' in the zoomed plot. When k_3 is gradually increased, the poles stay either permanently inside or outside the unit circle, solely depending on the choice of R_S and C_{DL}. This means that the loop stability is independent of the product of quantizer and LS gain, but depends only on the electrode parameters.

When the feedback loop has adjusted the electrode voltage to the desired value, the remaining input voltage at the quantizer will move towards small values, meaning the quantizer gain A_Q and therefore k_3 will move towards infinity. In this case the RLP shows, that one of the poles moves to $-\infty$. However, this will not result in instable behavior, but the pole will always remain on the real axis, representing the effect of a stable limit cycle. In this case, a very small input signal toggles around the comparator decision reference [104]. This happens, when the stimulator reaches the desired electrode potential, as the digital counter will always toggle with one current LSB around the final value.

Figure 4.24(a) shows a second RLP, where R_S was swept, while C_{DL} was kept constant for different values of k_3. It can be seen, that independent of k_3, the two complex poles always enter the unit circle for a solution resistance of $R_S = 50\,\Omega$. Since both analyses show, that stability is solely dependent on the R_S/C_{DL} combination, a third RLP was simulated to see the stability boundaries in dependency of R_S/C_{DL}, as shown in Figure 4.24(b).



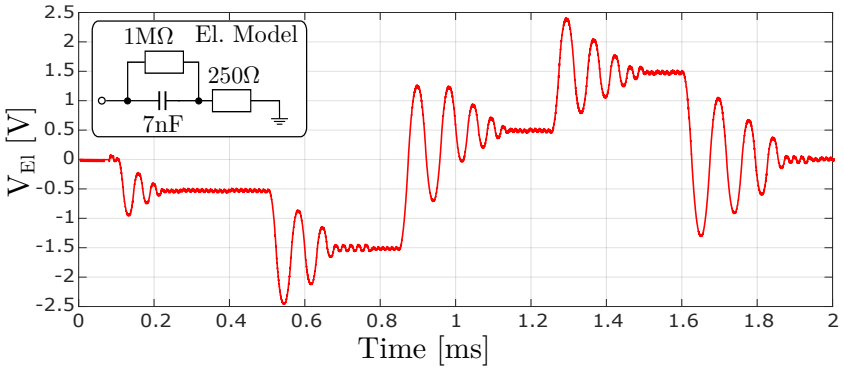
(a) Sweep of R_S with constant C_{DL}.

(b) Sweep of R_S with parametrized C_{DL}.

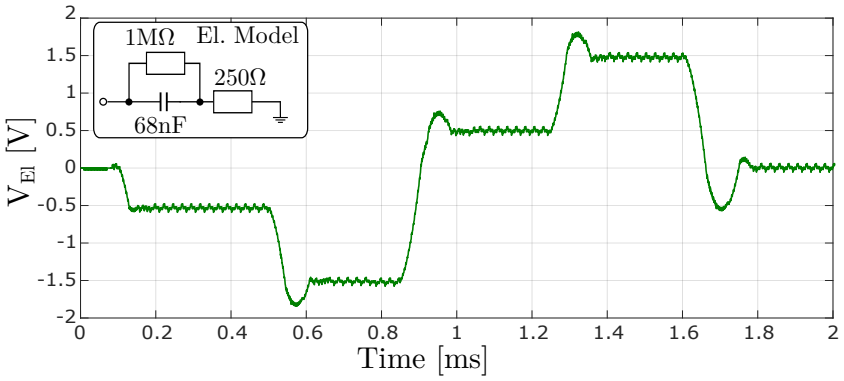
FIGURE 4.24: RLP for varying electrode parameters.

For the smallest simulated capacitance of $C_{DL} = 5\,\text{nF}$, a solution resistance larger than $200\,\Omega$ is required, whereas for larger C_{DL}, this minimum R_S value even drops. Since for small electrodes with small C_{DL}, the resistive part R_S is usually very large, this requirement is basically always met as long as the electrode is safely operated. Moreover, when looking at Equation 4.7, it can be seen that even if an electrode should not fulfill this requirement, the stability can be improved by increasing f_s, as this has the same effect on the system as increasing C_{DL}.

In order to verify the presented stability analysis, the stimulator was simulated on transistor level in the same 180 nm HV CMOS technology which is used for the recorder. The resulting electrode potential for two different R_S/C_{DL} combinations is shown in Figure 4.25. In both cases, an output range of $I_{FS} = 2\,\text{mA}$ was selected and the semi-digital loop was operated with a sampling frequency of $f_S = 1\,\text{MHz}$. According to our analysis, this would result in a minimum stable solution resistance of $R_{S,\text{min}} = 216\,\Omega$ for a double layer capacitance of $C_{DL} = 7\,\text{nF}$. In accordance with our calculations, the output voltage in Figure 4.25(a) shows stable behavior, but with very pronounced ringing, as the electrode parameters are chosen close to the stability limits. With an increased C_{DL}, the system stability can be significantly increased, which eliminates the ringing in Figure 4.25(b) and results in much faster settling speed.



(a) Ringing due to small R_S/C_{DL}.



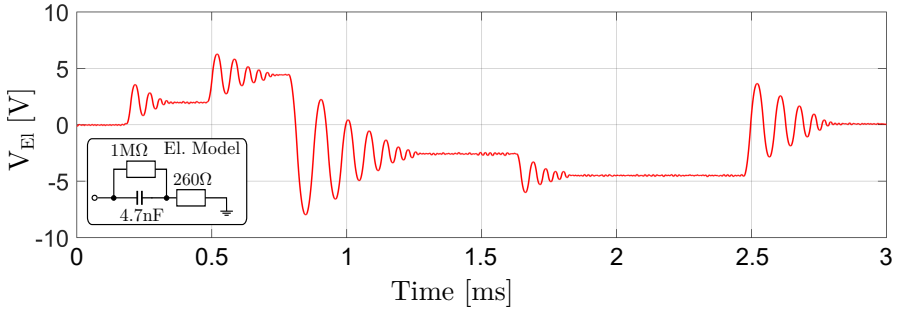
(b) No ringing as C_{DL} is increased.

FIGURE 4.25: Simulated CVS waveforms on two different electrode models.

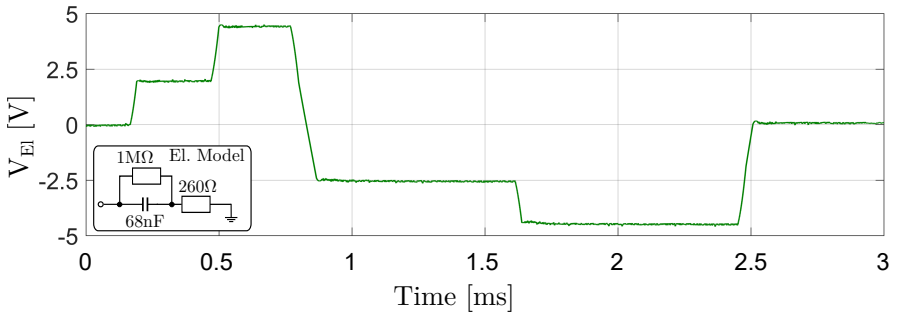
4.3.3 Measurement results

The described stimulator was tested using a single channel prototype, which was manufactured in the same 180 nm HV CMOS technology than the recorder. A first measurement is shown in Figure 4.26, in which the same voltage waveform was applied to two different, lumped element electrode models to demonstrate the electrodes impact on the system stability.

In both cases the sampling speed was set to $f_S = 1\,\text{MHz}$, equivalent to the previously shown simulation set ups. The red curve was recorded with $C_{DL} = 4.7\,\text{nF}$, $R_S = 260\,\Omega$ and $I_{FS} = 2\,\text{mA}$. As these parameters are again very close to the stability boundaries, the measurement shows heavy ringing, similar to the transistor level simulation. In the second measurement, shown in green, the modeled capacitance was increased to $C_{DL} = 68\,\text{nF}$. For illustration purpose, the maximum output current was additionally increased to $I_{FS} = 5\,\text{mA}$ which, according to Equation 4.7, further improves the systems stability. In accordance with the simulation results, the measurement shows no ringing and furthermore the overshoot was reduced to less than 100 mV.



(a) Ringing due to small R_S/C_{DL}.

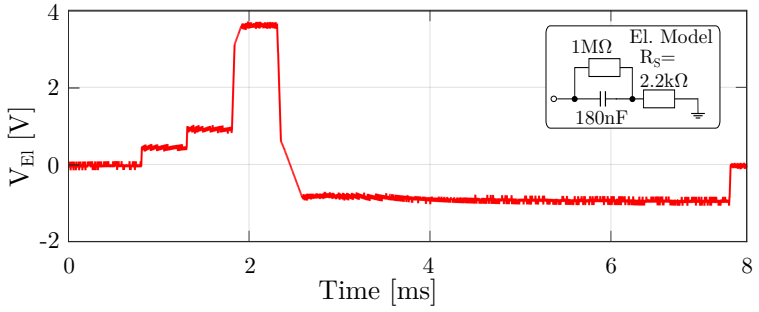


(b) No ringing as C_{DL} is increased.

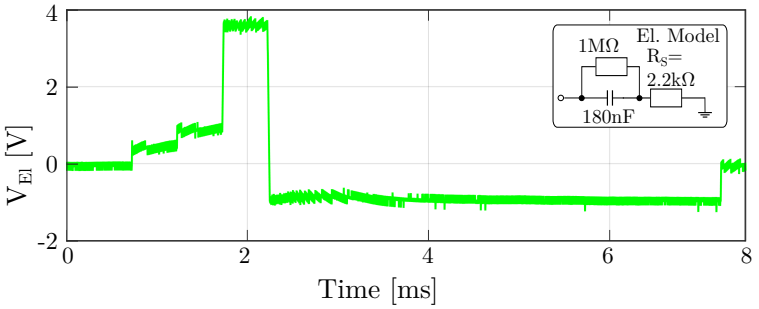
FIGURE 4.26: Measured CVS waveforms on two different, lumped elements electrode models.

In order to illustrate the effect of the adjustable full scale output current I_{FS} on the stimulation waveform, the same stimulation is shown with a full scale current of 1 mA and 2 mA in Figure 4.27. Since I_{FS} is set by the variable gain current mirror, as described in section 4.1, the minimum current step I_{LSB} is increased by a factor of 2 as well. This results in a two times bigger toggling $V_{tgl} = I_{LSB} \cdot R_S$ of the stimulation voltage around the desired value, for the same electrode parameters.

Beside the increased stability, the main advantage of the larger maximum current is the increased slew rate that can be seen when comparing the two curves in Figure 4.27. Since the stimulator can provide twice the current, the desired stimulation voltage is reached without slew rate limitations in Figure 4.27(b), whereas the decreased, maximum current leads to significant slewing in Figure 4.27(a). Thereby, the CVS offers a flexible trade-off between high accuracy, which is needed for small, high impedance electrodes and high output current, which is required for large, planar electrodes. A possible improvement to further increase the accuracy of the high current mode would be the use of a window comparator in a future implementation. Thereby the stimulator could detect if the stimulation voltage is within a certain accuracy window around the desired value and only readjust the current if this window is left, which would minimize the current switching.



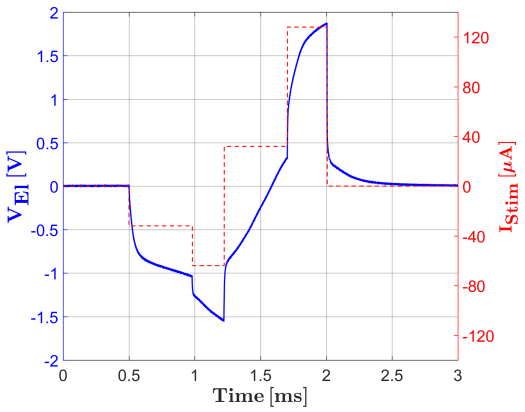
(a) $I_{FS} = 1\,mA$.



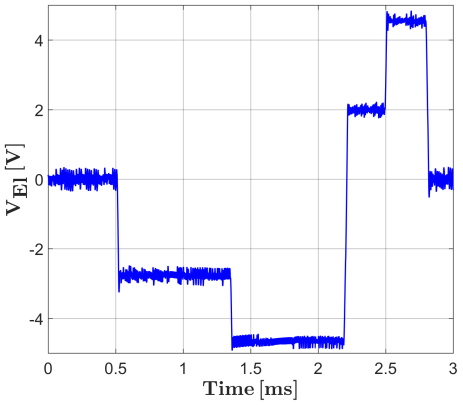
(b) $I_{FS} = 1\,mA$.

FIGURE 4.27: Measured CVS waveforms with varying full scale current I_{FS}.

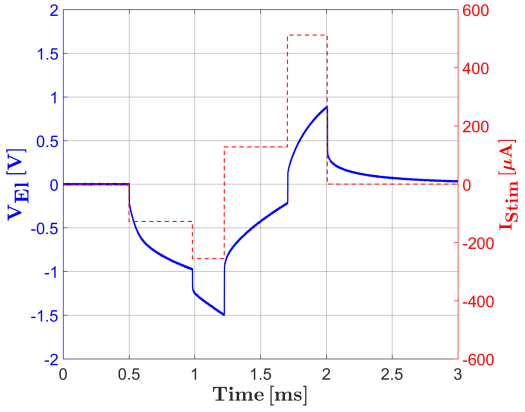
Since the shown lumped element model does not cover the non-linear behavior of the electrode-electrolyte interface, the stimulator was additionally tested on planar, platinum electrodes in PBS. Therefore, the electrode potential was acquired at the electrode connector, with a sampling rate of $f_S = 2\,MHz$. Since an additional shunt resistor would add up to R_S and thereby improve the stability of the control loop, the stimulation current was not measured in this case, therefore only the digital input value scaled by the current LSB is shown in Figure 4.28. The presented measurements show the reconfigurable current and voltage mode capabilities of the stimulator. In order to demonstrate the robustness of the implemented control loop, two electrodes with a diameter of 88 µm and 582 µm were used. Although the active area of the small electrode is more than 40 times smaller, still no ringing or overshoots can be observed in the measurements. After settling, small variations around the desired stimulation value can be observed, due to the toggling of the current LSB.



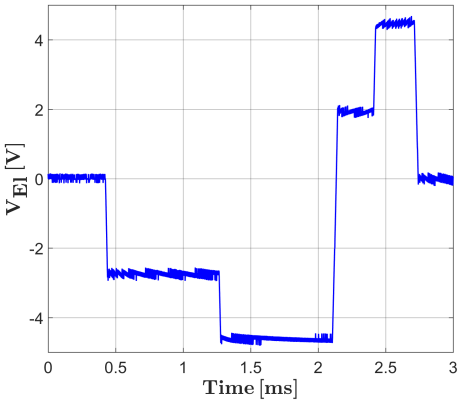
(a) Current mode, Pt electrode: $\varnothing = 88\,\mu m$.



(b) Voltage mode, Pt electrode, $\varnothing = 88\,\mu m$.



(c) [Current mode, Pt electrode, $\varnothing = 582\,\mu m$.



(d) Voltage mode, Pt electrode, $\varnothing = 582\,\mu m$.

FIGURE 4.28: Measured electrode potentials for CVS/CCS on Pt electrodes in PBS.

4.4 Area and power breakdown

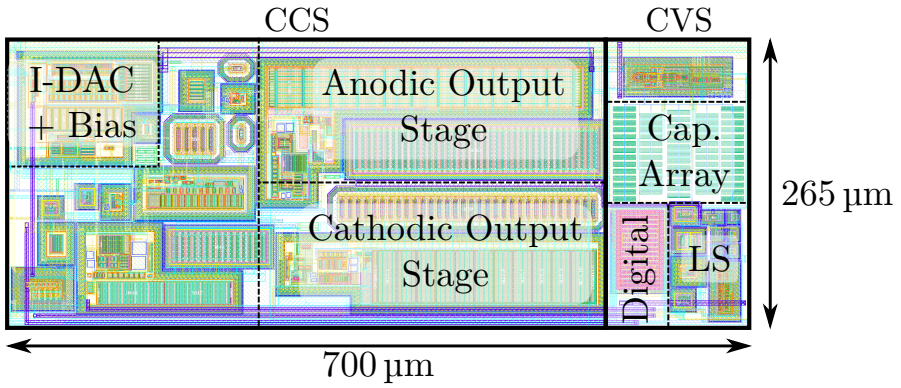


FIGURE 4.29: Layout of the HV current/voltage stimulator.

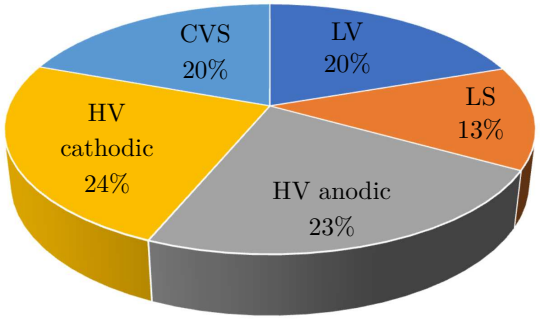


FIGURE 4.30: Area share of the HV stimulator.

Block	Area [µm²]
CCS	**148,960**
Waveform gen.	36,500
Level shifting	24,680
Output stages	87,780
CVS	**36,000**
Var gain LS	21,300
LV + digital	14,700

TABLE 4.3: Absolute area of the system blocks.

Figure 4.29 shows the layout of the combined voltage/current mode stimulator, the area shares of the different system parts are listed and visualized below. It is obvious, that the HV output stages are the main area consumers, as they require HV compliant transistors with large W/L-ratio to drive the stimulation currents of up to 10.2 mA. This shows again the benefit of the proposed, semi-digital feedback loop, as the complete current stimulator is reused, which results in an area overhead of only 20 %.

In section 4.1 it was already mentioned, that the complete biasing of the stimulator can be shut down, which results in a sleep mode where only negligible leakage currents are present. The same holds for the CVS, as the biasing of the comparators preamp can be shut down and the variable gain LS clock is gated. Although the power consumption will in general be dominated by the stimulation current, Table 4.4 lists the quiescent currents of the different system elements and their supply voltage in the standby mode during an active stimulation. This means, that no stimulation current is currently driven, but a stimulation is still active.

Block	**Supply current**	**Supply voltage**
	CCS	
LV dual OTA	5.4 µA	3 V/0 V
Anodic dual OTA	5.4 µA	9 V/6 V
Cathodic dual OTA	4.3 µA	-6 V/-9 V
Bias distribution	1.2 µA	+9 V/-9 V
Anodic LS reference	$I_{shift} = 2\,\mu A$	9 V/0 V
	$I_{OTA} = 330\,nA$	9 V/6 V
Cathodic LS reference	$I_{shift} = 2\,\mu A$	3 V/-9 V
	$I_{OTA} = 330\,nA$	-6 V/-9 V
	CVS (@ $f_S = 1$ MHz)	
Var. gain LS	5 µA	+9 V/-9 V
Comparator	1 µA	3 V/0 V
Digital filter	$< 100\,nA$	3 V/0 V

TABLE 4.4: Quiescent current I_0 of the different stimulator blocks.

The standby currents listed in Table 4.4 sum up to a total power consumption of 67 µW for one stimulation channel in current mode, if no stimulation current is applied but a stimulation is active. As the LS reference is shared between all channels in a multichannel design, it is excluded from the calculations. The biggest current consumers are the dual differential OTAs, as they need to be able to drive the large HV transistors and determine the settling speed of the stimulation currents. In voltage mode additional power is only significantly dissipated by the variable gain LS. In this case, it is the fast switching of the HV transmission gate, which is used to sample the electrode potential, that causes the power consumption. Due to their HV compliance, even minimum sized devices result in a significant gate area, which results together with the HV logic levels of ±9V in the listed current consumption.

If the stimulator is put into sleep mode during recording periods, the bias current of the three dual OTAs and of the CVS comparator is switched off, as well as the HV bias distribution. Additionally, the clock of the variable gain LS and the digital filter is gated. Only the two, shared LS references remain biased, in order to allow fast switching between sleep mode and active stimulation mode, resulting in a sleep mode power consumption of $P_{sleep} = 1.4\,\mu W$ for each channel within a 32 channel stimulator.

Chapter 5

32 Channel Bidirectional Neural Interface

In this chapter, the 32 channel, bidirectional neural interface is presented which was developed during the thesis. This final chip offers 32 independent front-ends, where each channel provides a LV, low noise, neural recorder with spectral LFP/AP selection and a HV stimulator with reconfigurable voltage/current mode stimulation. Additionally two multiplexed, Incremental $\Sigma\Delta$ (I-SD) ADCs were implemented to digitize the amplified, neural signal and a digital stimulation control unit that provides the waveform data during the stimulation process. In the first part of this chapter the front-end and the overall floor plan will be shown. After that, the supporting on-chip analog circuitry is explained, followed by the two ADCs and their digital interface. At the end of the chapter the digital stimulation control unit is presented in detail, together with its programming interface.

5.1 Neural front-end channels

Each channel of the 32 bidirectional, neural front-end channels is a combination of the stimulator and recorder presented in chapter 3 and 4, together with a local digital control unit (LCU), which provides the digital interface for stimulation control and recorder setup. All on-chip digital logic works from a 1.8 V digital supply in order to reduce the power consumption and allow the use of minimum sized standard cells, which are only rated up to 1.8 V. Additionally a separate digital ground pad is implemented to reduce switching noise within the analog parts. The interface between the 1.8 V LCU and the 3 V analog parts is realized with standard cell LS provided by the technology,

as illustrated in Figure 5.2. A detailed description of the LCU together with the digital waveform synthesis will be given in section 5.2.

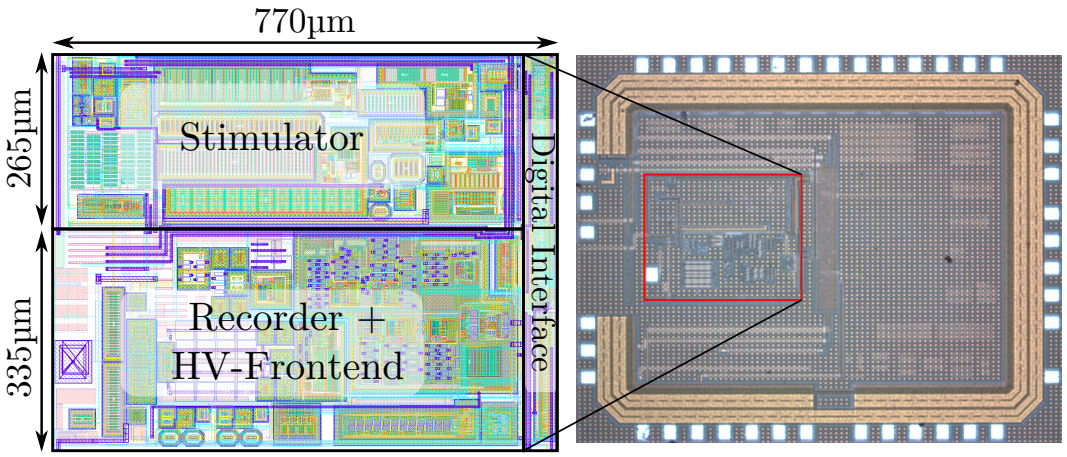


FIGURE 5.1: Layout and prototype of a single front-end channel.

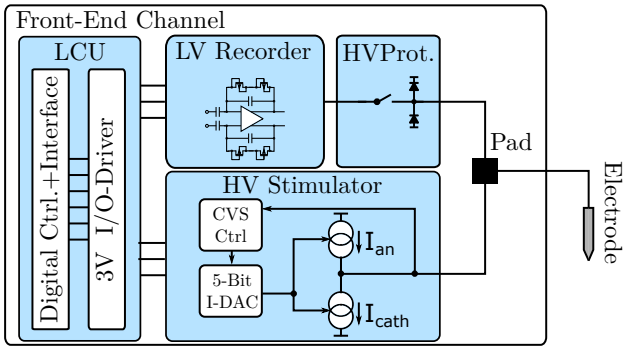


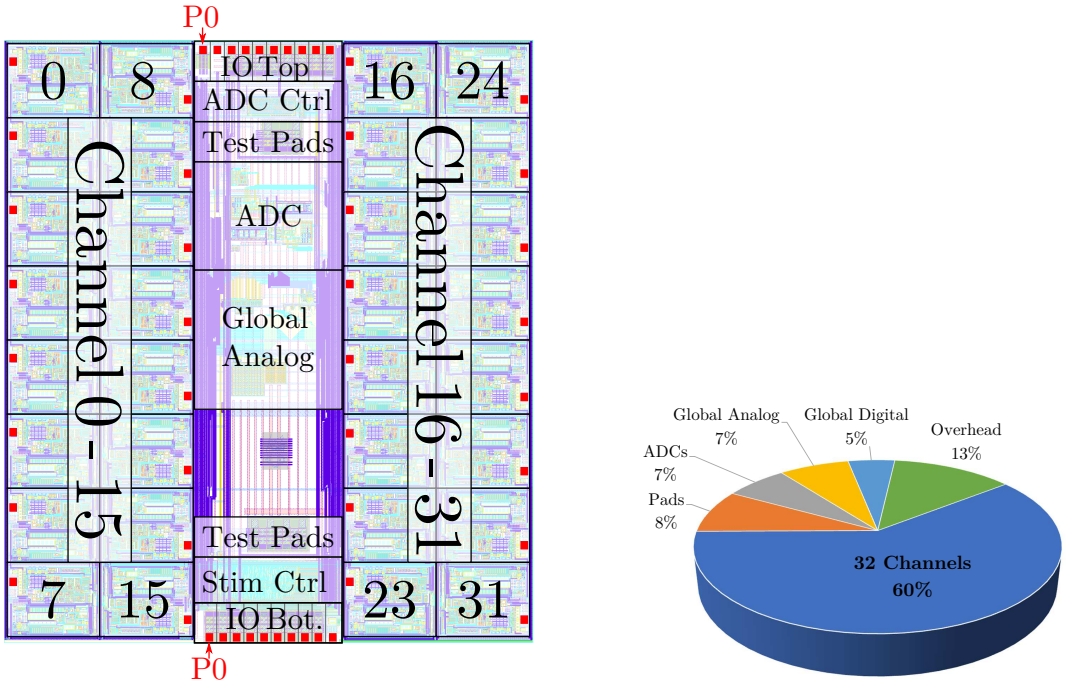
FIGURE 5.2: Block diagram of the neural front-end channel.

Block	**Area [µm²]**
Stimulator	185,500
Recorder	184,000
HV-FE	50,500
LCU	42,000
Total	462,000

TABLE 5.1: Area of the channel blocks.

In order to combine the LV recorder from chapter 3 and the HV stimulator from chapter 4, both parts are connected over the HV compliant protection interface [16]. The resulting connection can be accessed off-chip by one common bonding pad, which provides the interface to the working electrode. Figure 5.1 shows the layout of a single analog front-end channel and the chip photo of a prototype, manufactured in 180 nm HV-CMOS. Each channel requires an area of 770 µm x 600 µm, of which an almost equal share of 40 % is occupied by the stimulator and by the recorder. Another 11 % are required for the HV compliant recorder interface with the bonding pad and 9 % for the LCU. With the almost square form shape of the channel, the floor plan shown in Figure 5.3(a) was created for the SoC.

An improved area utilization could be achieved by flipping the channels 8-15 and 24-31 upside down, which can be seen by the slightly, vertically shifted bond pads indicated in red in Figure 5.3(a). This allows double-row placement while still being able to easily wire-bond all channel pads to the left and right hand side of the chip. This floor plan



(a) Floor plan of the 32 channel SoC.

(b) Area share of the system components..

FIGURE 5.3: Multichannel, bidirectional neural interface.

results in an overall chip area of 4.65 mm x 5.3 mm, which allows the use of commercially available 7 mm x 7 mm QFN-70 packages [107].

The remaining 20 IO pads that are required besides the working electrode pads are split up in 10 pads on the top side and 10 pads on the bottom side of the chip. Their functionality is listed in table 5.2, with *'Pin 0'* starting on the left side, as indicated in Figure 5.3(a). Figure 5.3(b) shows, that almost $^2/_3$ of the chip area are occupied by the front-end channels and only 13 % overhead area is required, which is currently pad limited and could potentially be improved by flip-chip bonding in a future version.

Pin	Pin name	Description
		IO Top
0	*VDD_9*	Positive HV supply ($V_{DD,HV}$), nominal: +9 V
1	*VSS_sub*	Negative HV supply ($V_{SS,sub}$), nominal: -9 V; substrate potential
2	*VDD_3*	Analog LV supply nominal: 3 V
3	*adc_clk*	Clock for the ADCs and SC clock generation nominal: $f_{clk} = 30$ MHz
4	*VSS_0*	Analog LV ground nominal: 0 V
5	*adc_data*	Serial ADC data output synchronous to ADC clk
6	*adc_csb*	Chip select of the serial ADC data out active low
7	*1V5*	Common mode reference voltage V_{CM} nominal: 1.5 V
8	*vref_p*	Reference for recorder tuning and channel estimation nominal: 500 mV
9	*sync_ch_0*	Digital sync signal indicating 'ch. 0' data output active high
		IO Bottom
0	*VDD_1V8*	Digital LV supply nominal: 1.8 V
1	*spi_clk*	Clock signal for the stimulation control nominal: $f_{clk} = 8$ MHz
2	*VSS_digi*	Digital LV ground nominal: 0 V
3	*resetb*	Global, digital reset signal active low
4	*chip_id[0]*	Bit 0 of the 3 bit chip ID
5	*chip_id[1]*	Bit 1 of the 3 bit chip ID
6	*chip_id[2]*	Bit 2 of the 3 bit chip ID
7	*data_io*	Serial data IO for stim. data and rec. set-up synchronous to spi_clk; bidirectional
8	*spi_csb*	Chip select for the serial data IO active low; requires ext. pull-up res. to *VDD_1V8*
9	*ref_el*	Reference electrode input

Table 5.2: IO pin description of the 32 channel SoC.

5.2 Digital stimulation control

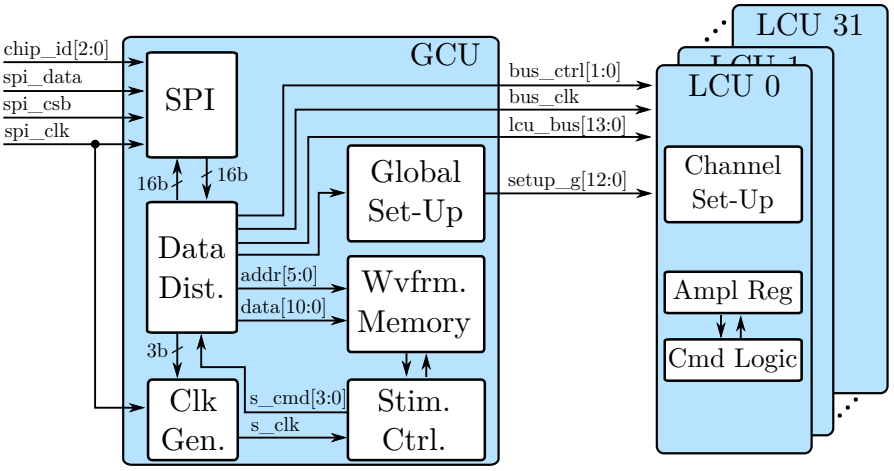


FIGURE 5.4: Block diagram of the digital stimulation control.

The digital control was designed to allow the clustering of up to 7 chips, by assigning a static 3-bit chip-ID to the neural interface chip and the dedicated *3'b000* address to the control master, e.g. a micro controller. The main challenge that arises through this possible large channel count is the trade off between the complexity of the control logic and the flexibility in waveform generation. This forbids to store the complete waveform of each stimulation channel amplitude value by amplitude value with sufficient time resolution, as it would exceed the available area and power budget. Therefore, the approach which was first presented in [73], is adapted. It splits up the digital control into local and global functions.

The local functionality is provided by an individual Local Control Unit (LCU) at each channel and shared, global functions are provided by one Global Control Unit (GCU). The main functionality of the GCU is to provide the digital interface to an off-chip programming unit, which provides the stimulation data (e.g. timing, waveform, amplitude), to store the waveform information and to provide the stimulation timing. Each LCU must store the local amplitude information, as these will differ from channel to channel depending on the required stimulation location and provide the local channel set-up. Figure 5.4 illustrates the combination of GCU/LCUs and shows the communication bus that provides set-up and timing data to the LCUs. Before the different functional blocks are described in detail, first the stimulation process will be described in general to facilitate the explanation.

The principle idea for the waveform generation is based on global timing assignment and local amplitude control. Therefore, an initial stimulation amplitude is stored as a local value in the LCU and locally modified during the stimulation process by commands that

are globally timed and generated by the GCU. Figure 5.5 illustrates this stimulation process, which will be described step-by-step in the following.

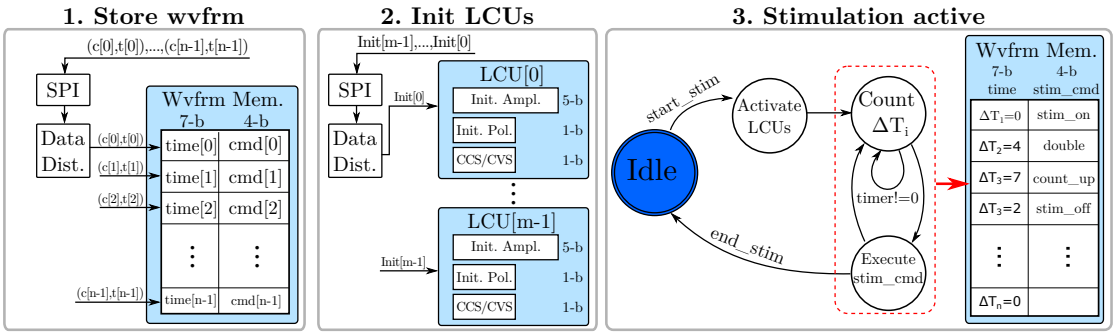


FIGURE 5.5: Stimulation process with global timing and local amplitude control.

1. *Store waveform*

   In the first step, the shape of the stimulation waveform is defined. Therefore, the same set of n 4-bit stimulation commands is stored in the waveform memory of each GCU in the cluster, together with a 7-bit timing value for each command. This information must be provided by the master control device over the SPI bus. A detailed description of the transmission protocol is provided in subsection 5.2.1.

2. *Initialize LCUs*

   Before a stimulation can be started, each LCU which is supposed to stimulate, needs to be initialized with a 5-bit initial amplitude, the initial stimulation polarity (anodic/cathodic) and the desired stimulation type (current/voltage). All initial data must again be provided over the serial interface, together with the desired LCU address, which is composed of a 5-bit, hardwired, on-chip address and the 3-bit chip ID. After initialization, the according LCU is marked as initialized, meaning it will listen to the command bus during stimulation.

3. *Stimulation active*

   After storing the stimulation waveform and initializing the desired LCUs, a stimulation can be started by sending the dedicated *start_stim* command over the SPI bus. This will transfer all GCUs into the *stim_active* state, where they will execute the same stimulation commands in parallel. After activating the LCUs over a dedicated on-chip command line, the stimulation control will read the first set of command/timing data and start to decrement the read timing value. When the timing value reaches zero, the according stimulation command is executed over the control bus and the next command/timing set is read from the waveform memory. This is done until the last, stored entry is reached, which terminates the stimulation process and returns the GCU to the initial *idle* state.

Since all GCUs get the same clock from the master control unit and the same waveform information, a synchronous stimulation process is guaranteed.

5.2.1 Global control unit (GCU)

The main control logic of the GCU is located within the *Data Distribution* block, which manages the complete on-chip data flow. Bidirectional off-chip communication is provided over a Serial Peripheral Interface (SPI) interface, as serial data transmission minimizes the number of required pads.

Serial peripheral interface (SPI)

In the current implementation the communication between the chips in the cluster and the master control unit is realized with a SPI bus. It was designed for a nominal SPI clock speed of $f_{SPI} = 8\,MHz$, which must be provided by the master control unit. Each member of the bus has a synchronized address counter and is only allowed to start a transmission if the address counter is equal to its assigned 3-bit chip ID and no other bus member is currently speaking. The address counter is synchronized after the power-up over the global reset signal, which must be provided by the master control unit. All address counters are synchronized between the members of the SPI bus, by setting them to *0* after startup by the global reset signal and synchronously counting up on every rising clock edge of the common *spi_clk*.

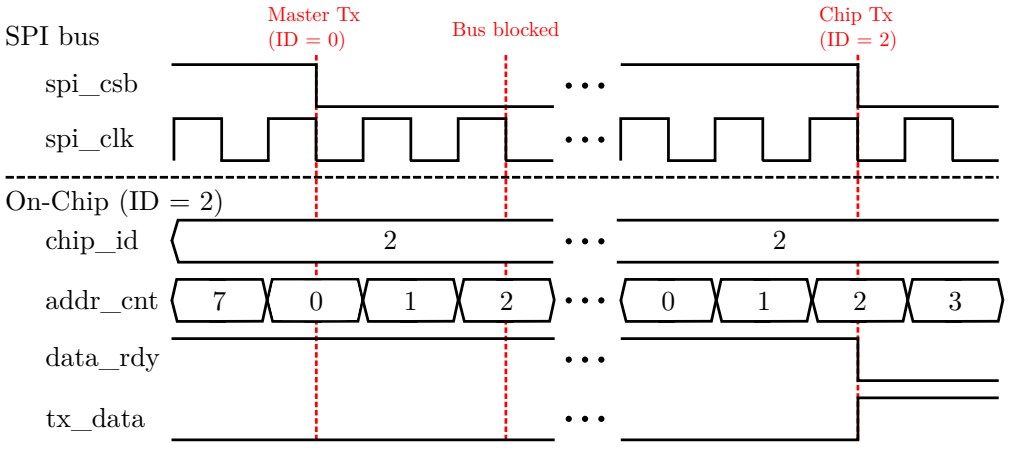


FIGURE 5.6: Exemplary SPI bus management based on chip id.

Figure 5.6 shows the internal signals of a neural interface, which has the statically assigned ID *chip_id = 2*, to illustrate the prioritization of transmissions. Indicated by the first, dotted red line a transmission from the master control unit to one member of SPI bus is started, by pulling the chip select bit *spi_csb* low. The master control has its ID

set to *0* which means it can start a transmission if the address counter *addr_cnt = 0* and the chip select bit *spi_csb* is high, meaning no other transmission is currently happening over the bus. Therefore, the intended transmission is started at the falling edge of the SPI clock.

The second red line indicates the situation, that data is ready to be transmitted from on-chip to the master controller, but the bus is still blocked by a transmission. Since the internal address count equals the chip ID and the *data_rdy* flag is set high, the SPI controller would initialize a transmission if the bus is available. However, since the chip select bit *spi_csb* is already pulled low by the master controller, the new transmission is currently blocked. Therefore, transmissions from chips with a lower chip ID have a higher priority and the master controller has the highest priority. The third red line indicates the instance where the postponed transmission from chip *2* is started, as the address count value is *2* and the SPI bus is unoccupied.

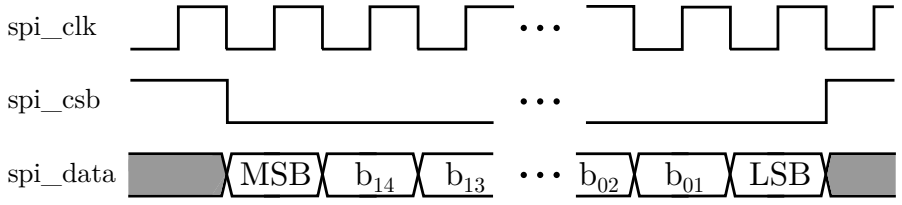


FIGURE 5.7: Timing of the SPI data transmission.

The actual transmission process is shown in detail in Figure 5.7. A transmission is started when the Chip Select Bit (CSB) goes low, after which one SPI word with the MSB first is received, consisting of 16 consecutive bits, read in on the rising clock edge. In order to ease off-chip timing, new data is applied and the CSB state is changed on the falling edge of the SPI clock. The CSB line itself requires an external pull-up resistor to 1.8 V, since it is only actively pulled low by the currently transmitting chip. If no transmission is active, all CSB IOs of the bus members are high-ohmic, thus requiring the external pull-up. If a full word was successfully received, a dedicated *data_rdy* control line signals the Data Distribution Unit (DDU) that new data is available and the data is forwarded via a 16 bit parallel bus.

Data Distribution Unit (DDU)

The DDU contains the main part of the global control logic and manages the whole on-chip data flow. Figure 5.8 shows all connections of the DDU sorted by the adjoining logical blocks.

On the top left, the *chip_id*, *spi_clk* and *resetb* are shown, which must be provided by the external master control unit. Below that, the previously explained bidirectional SPI is

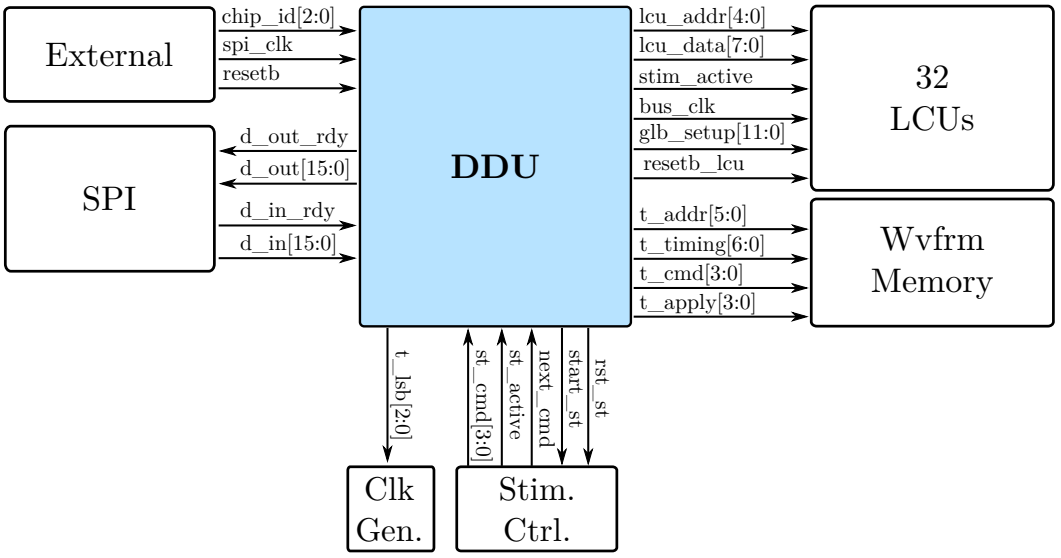
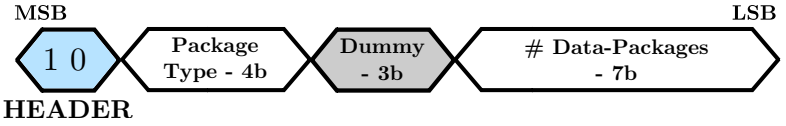
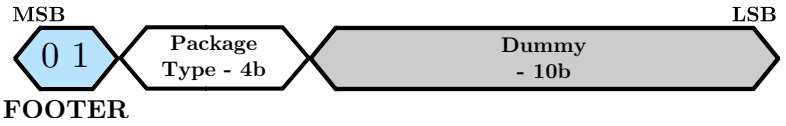


FIGURE 5.8: Data IOs of the Data Distribution Unit (DDU).

shown, which manages the external data IO. It is connected over the 16 bit wide *data_in* bus to the DDU, that provides the received, parallelized input data and the 16 bit wide *data_out* bus that provides return code data. The SPI was implemented in a standalone block to allow an easy replacement in a future version, where an arbitrary on-/off-chip wireless data receiver with clock recovery could be used.



(a) Header control word.



(b) Footer control word.

FIGURE 5.9: Structure of the 16 bit SPI control words.

In general, the 16 bit SPI words can be divided into two subcategories, control words that are illustrated in Figure 5.9 and data words. Control words start the transmission to the DDU via the dedicated header bits, indicate the DDU what type of data will be sent over the 4 bit package type and how many packages will be sent over the 7 bit package count and close the transmission over the dedicated footer bits. The indicated number of packages is sent between a header- and a footer-control-word via data words. The structure and number of data words depend on the type of data that is transmitted to the DDU, each possible type is illustrated and explained in section 5.2.2.

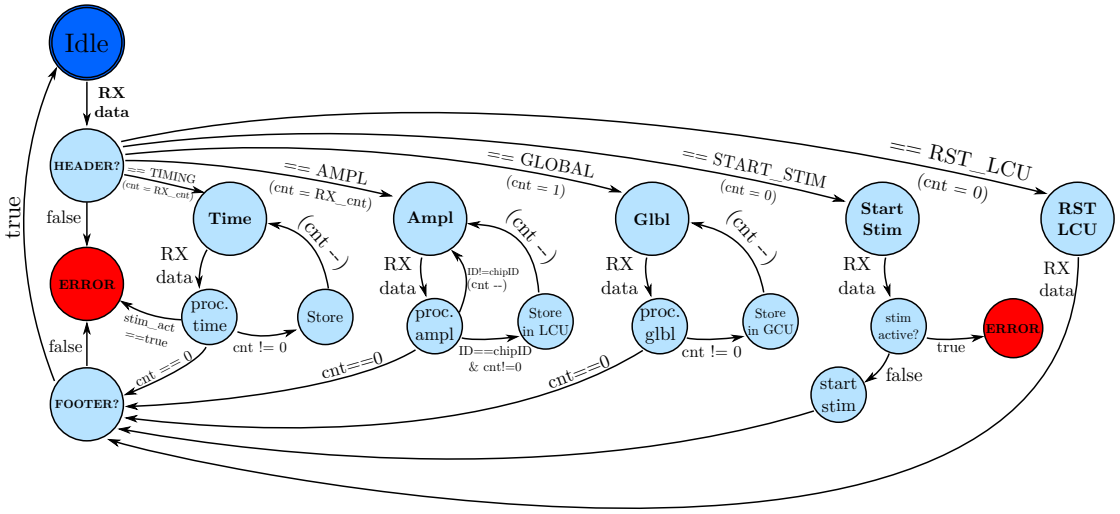


FIGURE 5.10: Finite State Machine (FSM) of the DDU.

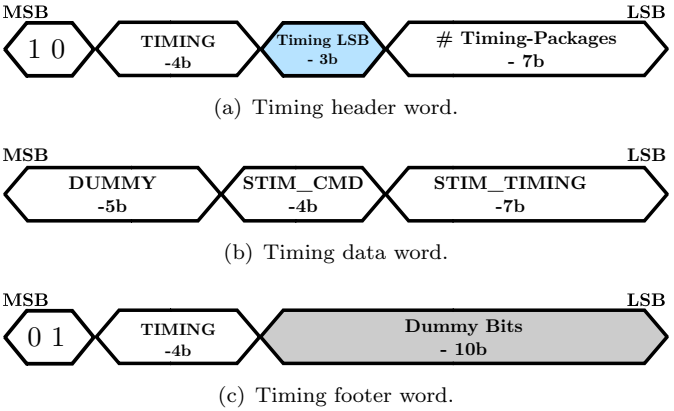
Figure 5.10 shows the Finite State Machine (FSM), which is used to process the data reception within the DDU. Starting in the *Idle* state, the DDU expects one of the 5 header control words, followed by the indicated number of data words. To keep track over the amount of received data, the *RX_cnt* register is set to the initially indicated number of packages and decremented after each received data word until it reaches 0. In order to detect possible package loss or faulty programmed transmissions, each transmission sequence must be closed after the last data package by the according footer command word, otherwise the DDU will discard the received data and enter the *ERROR* state which is described in detail in section 5.2.4.

5.2.2 Data Package Types

In the following section, each data package type will be shown and explained in detail. As previously described, each transmission consists of a header package, a footer package and depending on the information type a variable amount of data word packages.

Package type: TIMING - Receive global timing data

The transmission of global timing data that defines the stimulation waveform, is initialized by sending the timing header word illustrated in Figure 5.11(a). It consists of the 4 bit timing command, a 3 bit timing LSB which sets the internal clock divider described in section 5.2.3 and the 7 bit long number of timing data words. After receiving the timing header word, the DDU receives the indicated amount of stimulation command/timing data sets which are required for waveform



(a) Timing header word.

(b) Timing data word.

(c) Timing footer word.

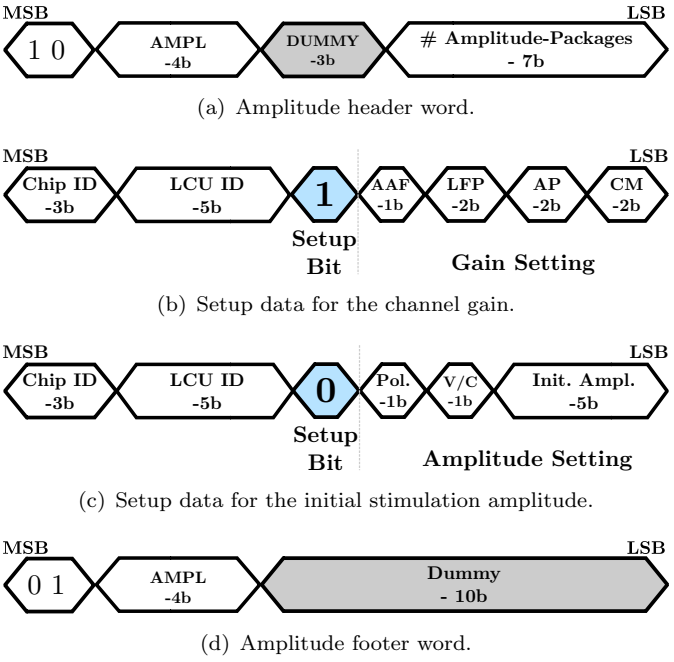
FIGURE 5.11: Bit level structure of a global timing transmission.

synthesis. Each set is consecutively stored in the waveform memory, where the first command receive will be the first command executed during waveform synthesis.

Figure 5.11(b) shows the corresponding data word, which contains the timing value in the 7 LSBs, followed by the 4 bit stimulation command. Since each command/timing pair requires only 11 bit, the 5 MSBs have to be filled up with dummy bits to form a valid SPI word.

The transmission process must be closed by the timing footer word, shown in Figure 5.11. It consists of the two dedicated footer MSBs, followed by the same 4 bit *TIMING_CMD* command used in the header word.

Package type: AMPL - Receive local setup data



(a) Amplitude header word.

(b) Setup data for the channel gain.

(c) Setup data for the initial stimulation amplitude.

(d) Amplitude footer word.

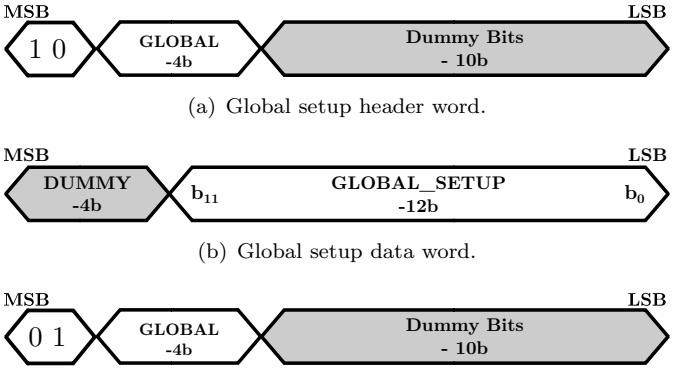
FIGURE 5.12: Bit level structure of LCU setup data transmission.

The transmission of local setup data for the LCUs is similar to the described global timing data transmission. Figure 5.12(a) and Figure 5.12(d) show the corresponding header and footer words that initialize and close the transmission process. The header consists of the two dedicated header MSBs, followed by the *TIMING* command, 3 unused dummy bits and the amount of amplitude packages within the transmission coded in the 7 LSBs. The footer structure is equivalent to the one used in the transmission of global timing data.

Since local data can contain the setup of the recorder channel as well as initial stimulation amplitude and polarity, the data packages are further divided by a dedicated setup bit. Figure 5.12 shows the two possible types of amplitude data words. Depending on this bit, the following 7 bits are either stored in the gain setup register or the initial amplitude register for the next stimulation within the LCU.

Each received amplitude word is checked within the DDU if the sent *chip ID* matches the externally assigned chip ID. If this is the case, the 5 bit LCU ID is applied to the address bus and the remaining 8 bits are transmitted over the data bus, as pictured in Figure 5.8. This avoids unnecessary on-chip data transmission, in case the data is addressed to a different chip within the cluster, in order to reduce dynamic power consumption.

Package type: GLOBAL - Receive global set-up data



(a) Global setup header word.

(b) Global setup data word.

(c) Global setup footer word.

FIGURE 5.13: Bit level structure of a global setup transmission.

In this state, the DDU receives one global setup data word, which overwrites the previous global setup. Figure 5.13(a) and Figure 5.13(c) show the corresponding header and footer word. Since the 12 bit global setup must always consist of exactly one SPI word, no package number is needed within the header, as it was required for the two preceding transmission types.

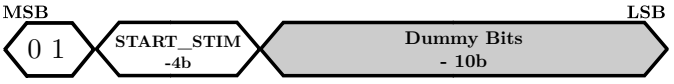
Name	Description	Setup Bit	Default Value
Low Gain Mode	LNA low gain mode for impedance estimation, as described in section 3.4.	b_{11}	0
LNA Tune Off	Switches pseudo resistor tuning of the LNA, as described in section 3.3.	b_{10}	1
Tune DAC Value	Input value of the serial DAC used for pseudo resistor tuning in the LNA.	b_9 - b_6	4'b0000
f_{HP} AP-band	High-pass cutoff frequency of the AP channel biquad filter (c.f. section 3.1).	b_5 - b_4	2'b00
f_{LP} LFP-band	Low-pass cutoff frequency of the LFP channel biquad filter (c.f. section 3.1).	b_3 - b_2	2'b00
Record AP-band	AP band select in the summing S/H.	b_1	1
Record LFP-band	LFP band select in the summing S/H.	b_0	1

TABLE 5.3: Global channel setup configuration.

Table 5.3 lists the 12 setup bits and describes their functionality. As long as no global setup data was received by the DDU, the listed default values are applied after a reset. Each new received set of global setup data overwrites the previously stored setup.

Package type: START_STIM - Start stimulation process

(a) Start stimulation header word.



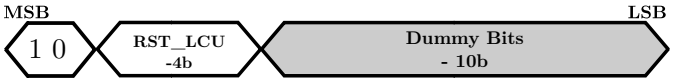
(b) Start stimulation footer word.

FIGURE 5.14: Bit level structure of the stimulation start command.

The *START_STIM* command does not accept any data word inputs, but requires as the next input the corresponding *START_STIM* footer package. If both, header and footer package are received in the correct order, the stimulation process is started with the previously stored timing at each electrode which as initialized with amplitude data. This was implemented to avoid an accidental triggering of the stimulation process, therefore any other input will result in the error state. If

a stimulation is already running and another *START_STIM* command is received, the DDU changes into the error state as well.

Package type: RST_LCU - Reset all LCUs



(a) LCU reset header word.

(b) LCU reset footer word.

FIGURE 5.15: Bit level structure of the LCU reset command.

Similar to the *START_STIM* command, this state does not accept any data word inputs, but requires as the next input the corresponding *RST_LCU* footer package. If both packages are received in the correct order, the stored amplitude data in all LCUs is reset to their default state. In standard operation, LCUs are not reset after a stimulation process, in order to allow the same stimulation pattern several times, without retransmission of the amplitude values after each stimulation. This will be explained in detail in section 5.2.3.

The described transmission protocol was designed to provide the minimum data overhead for transmission of amplitude data. Since the waveform is usually kept constant within an experiment or once it has been adapted to the need of the patient, it has only a small share on the stimulation data required during operation. However, amplitude data has to be constantly updated, depending on the desired stimulation site and intensity, which makes it the largest part of all transmitted packages.

5.2.3 Waveform synthesis

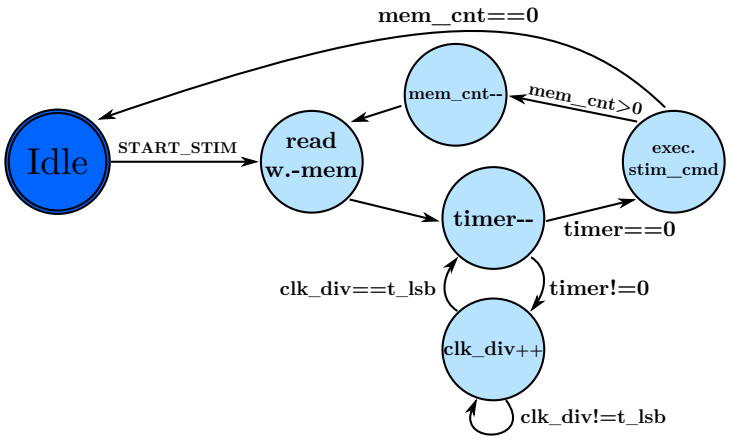


FIGURE 5.16: FSM of the stimulation waveform synthesis.

Once a stimulation has been successfully initialized and triggered by the according command, the stimulation control manages the waveform synthesis. At the beginning of each stimulation event, the HV protection switches at all electrodes that are involved in the stimulation process are automatically opened to protect the recorder from damage. After that, the stimulation control sequentially reads out the stored stimulation commands and timing values from the waveform memory and processes them as illustrated in the FSM in Figure 5.16.

After the timer value for a command has been read from the waveform memory, it is decremented to zero with an adjustable timing LSB that is realized with the 3 bit internal counter *clk_div*. As previously described, the value for this divider is set in the timing header package (c.f. Figure 5.11(a)) whenever new timing data is transmitted to the DDU. This allows to program a minimum time step ranging from 125 ns to 1 µs. When the timer reaches 0, the stimulation command is transfered to the DDU, which forwards and executes it over the on-chip bus at all LCUs simultaneously. Table 5.4 lists all available stimulation commands for amplitude manipulation, which can be realized with a simple shift and count working register in the local units. This results in an area and power efficient implementation, while still providing high flexibility in the waveform design.

Each stimulation process must be closed with the command *c_END_STIM*, which automatically reconnects the recorder over the HV switches, returns the stimulator to the power saving sleep mode and restores the state of the LCU before the stimulation process. This means, that initialized LCUs are not reset after one stimulation process, but the same stimulation pattern can be triggered again by sending another stimulation start command over the SPI bus. However, if this immediate re-initialization of the LCU amplitude values is not desired, an additional *c_RST_LCU* command can be added before

the *c_END_STIM* command, which causes the LCUs to return to the non-initialized state after the stimulation.

Stimulation command	Binary value	Description
c_STIM_OFF	0000	Turn the stimulation current/voltage off
c_STIM_ON	0001	Turn the stimulation current/voltage on
c_LSB_UP	0010	Increase the stimulation current/voltage by 1 LSB
c_LSB_DOWN	0011	Decrease the stimulation current/voltage by 1 LSB
c_DOUBLE	0100	Double the stimulation amplitude.
c_HALF	0101	Half the stimulation amplitude.
c_INV_POL	0110	Invert the polarity of the stimulation current/voltage.
c_INIT_DAC	0111	Load the initially stored stimulation amplitude.
c_DISCH	1000	Toggle the passive discharge switch.
c_RST_LNA	1001	Toggle the reset switch in the LNA/AAF feedback.
c_IDLE	1010	Return to the initial idle state (recording state).
c_RST_LCU	1010	Reset the LCU to the non-initialized state.
c_I_PULSE	1100	Toggle the LSB current pulse for channel estimation.
c_I_PULSE	1101	Toggle the voltage pulse for channel estimation.
c_END_STIM	1110	End of stimulation command.
c_REC	1111	Toggle the HV recording switch.

TABLE 5.4: Stimulation commands for waveform synthesis.

Since the recorder is automatically disconnected at stimulating electrodes during a stimulation event, the additional command *c_REC* has been added to the command set. This allows the user to manually toggle the state of the HV recording switch during a stimulation event. However, this command should be used very carefully, since a wrong switching of the protection switches can damage the recorder, by exceeding its safe input voltage range.

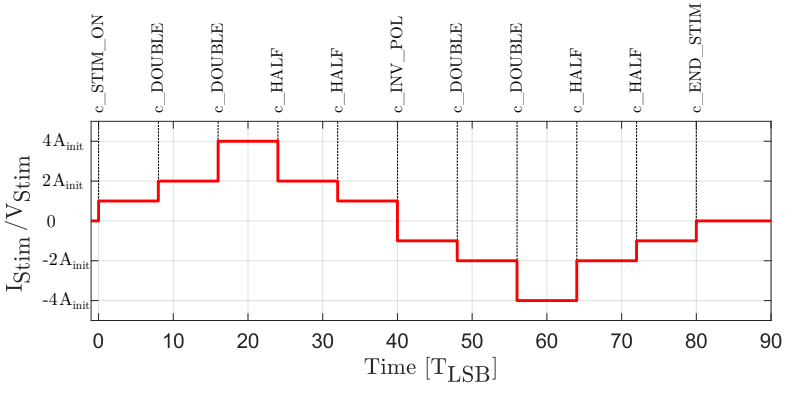


FIGURE 5.17: Default stimulation waveform.

In order to allow direct stimulation after a startup, the default stimulation waveform shown in Figure 5.17 has been implemented. It is by default loaded into the waveform memory after each startup and cannot be changed.

5.2.4 Global Error Handling

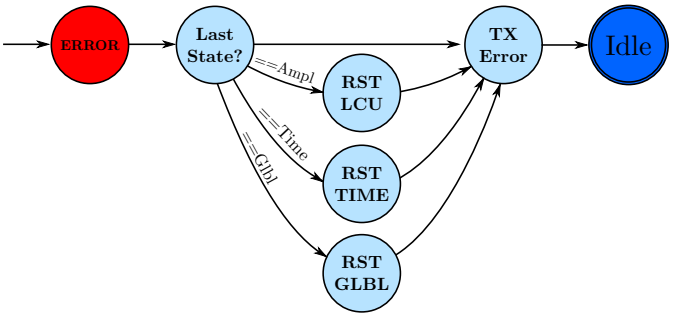


FIGURE 5.18: Global error handling in the DDU.

If the DDU receives an unexpected package, it enters the *ERROR* state. This can either happen if a transmission is started without a header package, the wrong amount of data packages is sent between a header and a footer package, e.g. caused by package loss, or if new timing data is send during an active stimulation. Figure 5.18 shows the implemented FSM for error handling. Depending on the previous state, in which the DDU has been when the error occurred, all data which has been received in the ongoing transmission process is discarded to avoid error propagation. Thereafter, the error message shown in Figure 5.19 is generated from the previous transmission state and sent back over the SPI bus.

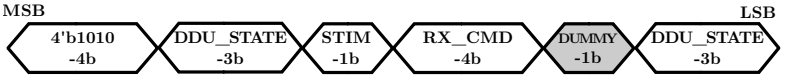


FIGURE 5.19: Generated error message.

Each error word is headed by the 4 bit sequence *4'b1010*, after which the state of the DDU is transmitted from which the error state was reached. The following *STIM* bit indicates, if a stimulation was active while the package that caused the error was received, followed by the received 4 bit stimulation command. The error package is closed by a dummy bit and the repetition of the 3 bit state of the DDU. This error message alleviates debugging, since the external user receives the complete DDU state in which the error was caused. Thereby, it can be seen, whether package loss occurred, a header/footer package was missing, or the transmission conflicted with an ongoing stimulation event.

5.2.5 Local Control Unit (LCU)

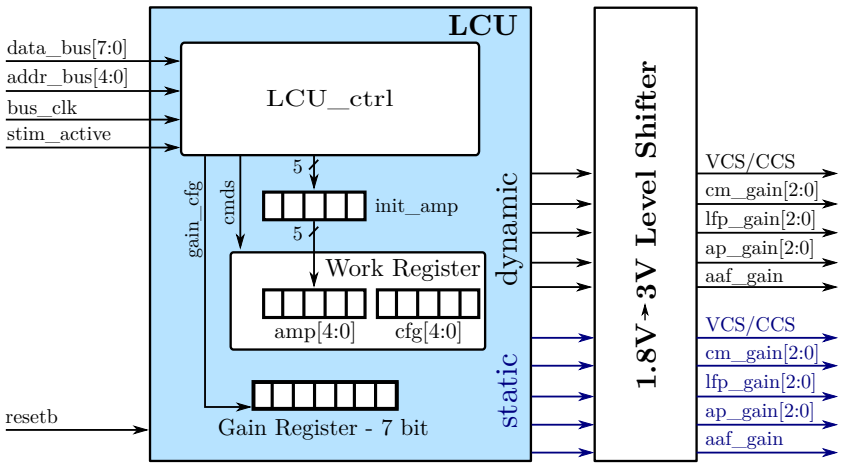


FIGURE 5.20: Block diagram of the Local Control Unit (LCU).

Figure 5.20 shows the block diagram of the LCU, which controls the local amplitude value of the stimulator and the gain set-up of the recorder channel. The main control logic is located within the *LCU_ctrl* block, which controls the internal data flow.

If no stimulation is active, the *stim_active* control line is pulled low by the GCU. When a new command arrives in this state over the 8 bit data bus, the *LCU_ctrl* checks if the 5 bit *data_bus* is equal to its hardwired address. If this is the case, the data is either stored in the 7 bit gain register, defining the record channel gain, or as initial stimulation amplitude data, based on the control bit, as described in the structure of the amplitude data package. All values in the gain register are static and can only be changed by transmitting new configuration data, if no stimulation is currently active.

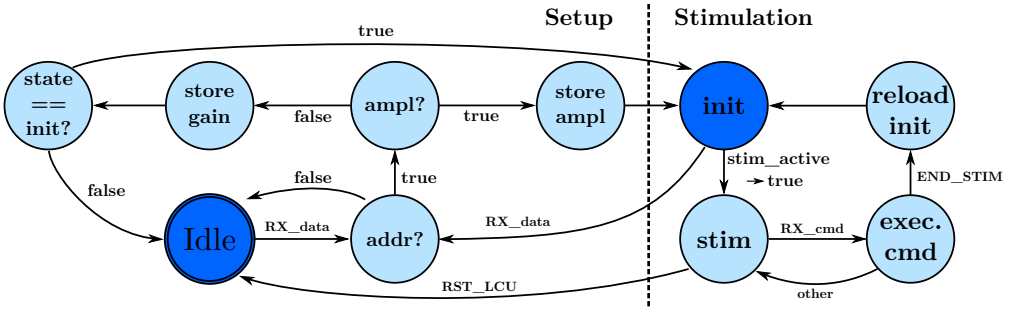


FIGURE 5.21: FSM of the Local Control Unit (LCU).

After the LCU received a set of initial amplitude data (5 bit amplitude, 1 bit polarity, 1 bit voltage/current stim), it changes its state to the initialized state *init*, meaning it will listen to stimulation commands if an active stimulation is indicated by the *stim_active* signal. When a stimulation starts, the amplitude data is loaded from the *init* register into a working register, which has the advantage that the initial value can always be restored

during stimulation. The work register can invert the polarity bit and provides a shift-and-count register for the amplitude value, which allows the hardware efficient execution of the commands listed in Table 5.4. During stimulation the stimulation commands are received and executed by all initialized LCUs simultaneously. The command distribution takes place over the *data_bus*, while the address bus is deactivated, since no addressing is performed during stimulation. Figure 5.21 shows the FSM of the LCU, where the left part illustrates the setup mode, meaning *stim_active* is low and the right part the active stimulation mode.

After a stimulation event, the LCU reloads the stored, initial data and returns to the *init* state. This has the advantage, that consecutive stimulations can be run without the need for re-initialization before every stimulation event as described at the end of section 5.2.3. This reduces the data overhead during experiments, that require the same stimulation waveforms at the same electrodes several times, which is e.g. the case, if an external trigger is used to start a constant stimulation.

As previously described, an automatic reset of the stimulation sites after a stimulation is triggered if the waveform is terminated by the *c_RST_LCU* command. This command returns all previously active LCUs into the uninitialized *idle* state. If said command is included in the timing information, each stimulation requires a new amplitude value at each desired electrode.

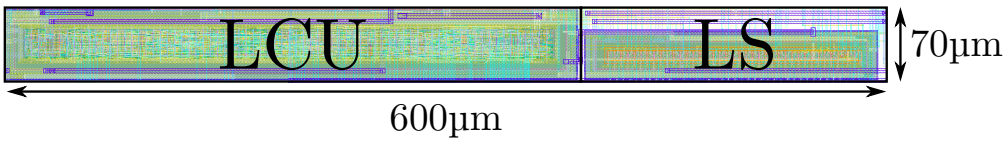


FIGURE 5.22: Layout of the Local Control Unit (LCU).

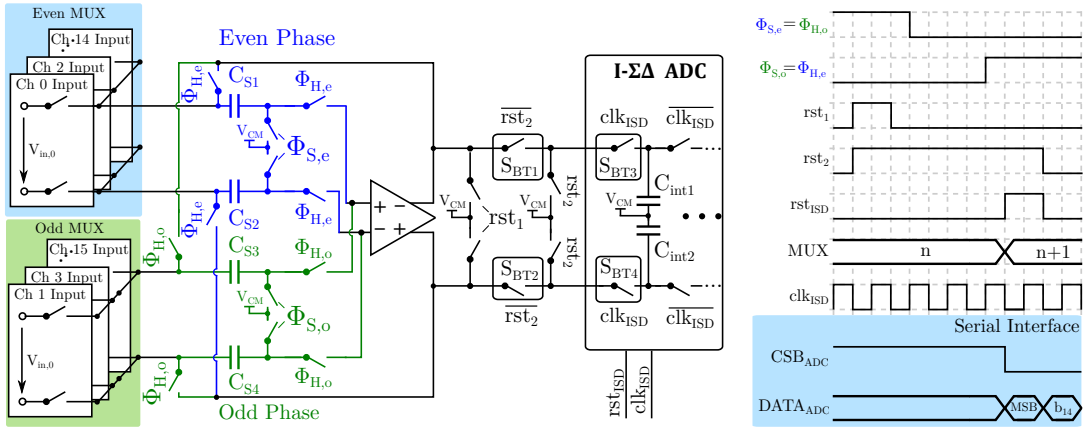
The LCU was synthesized using the 1.8 V standard cells provided by the X-FAB xh018 technology. In order to interface the 3 V analog circuitry, standard LS cells from the technology library were used, resulting in the layout shown in 5.22. The total LCU, including level shifting, requires an area of $600 \times 70\ \mu m^2$. The stretched layout is a result of the channel height of 600 µm, which results in an ideal area utilization of the mixed signal channel, as previously shown.

5.3 On-Chip Analog to Digital Converters (ADCs)

In order to digitize the acquired signals from all 32 channels, two incremental ΣΔ-ADCs were implemented on-chip. The incremental architecture was chosen, as it allows to share one ADC between many channels by multiplexing, since it provides true sample-to-sample conversion at Nyquist rate. Additionally, a high resolution of 14 bit or more

can be achieved, since this type of converter benefits from noise shaping and a trade-off between resolution and Oversampling Ratio (OSR) is possible. The implemented ADC was first presented in [108] were a sampling frequency of $f_S = 30\,MHz$ was used with an OSR of 150, resulting in a Nyquist rate of $f_N = 200\,kS/s$. With these parameters an effective resolution of 15 bit and a power consumption of only 1.1 mW was achieved.

In order to digitize all 32 channels with 2 ADCs at the required sampling rate of 20 kS/s/ch, each ADC needs to provide a sampling rate of 320 kS/s. Therefore, the OSR in the aforementioned ADC was reduced from 150 to 90, which results in an ideal, effective resolution of 14 bits and a maximum Nyquist rate of $f_N = 333kS/s$, which meets the required specifications while leaving the power consumption unchanged. Using two of these modified ADCs the SoC is split up in the middle, where the 16 channels of the left half (channel 0-15) are digitized by ADC 1 and the 16 channels in the right half (channel 16-31) are digitized by ADC 2.



(a) S/H with 16 channel multiplexer.

(b) Timing diagram.

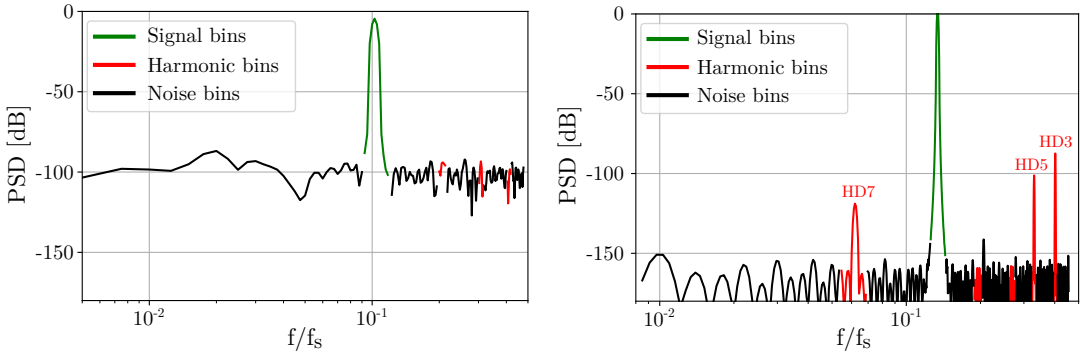
FIGURE 5.23: Multiplexed, 16 channel sample-and-hold for the on-chip ADC.

Figure 5.23 shows one of the two fully differential input Sample-and-Hold amplifiers with its corresponding ADC. The 16 channel multiplexer is realized within the S/H, with one pair of input switches for each of the 16 channels. During each sampling period, only one channel is connected to charge up one of the two sampling capacitor pairs $C_{S1/2}$ or $C_{S3/4}$. The shown "ping pong" implementation allows to constantly operate the ADC, with no idle time between the end of one conversion cycle and the beginning of the next cycle. At the same time, the speed requirements on the previous stage are alleviated, since it has one full conversion cycle, during which it has to charge the corresponding sampling capacitors. The flip-around S/H architecture additionally improves the initial settling, since only parasitic capacitors have to be charged by the OTA when changing from the sample to the hold state, since the sampling capacitors are already pre-charged

during the sample phase. All control signals are generated from the 30 MHz ADC clock clk_{ISD} and are shown in Figure 5.23(b).

After each conversion, the sampling capacitors are discharged by turning rst_1 high, 5 clock cycles before the end of the conversion. During this reset, the ADCs input signal is pulled to 0, with the control signal rst_2, introducing a recuperation phase to the IΔΣ-ADC, as it was proposed in [109]. This slightly improves the performance of the modulator and at the same time alleviates the timing in the S/H. At the end of the conversion, the integrators of the IΔΣ-ADC are reset with the rst_{ISD} signal and the acquired value is streamed out over the serial interface, as indicated in the bottom part of Figure 5.23(b). After the transmission of 16 bits from the first ADC, CSB_{ADC} goes high for one clock cycle, before the 16 bits of the second ADC are transmitted.

All switches could be realized as transmission gates with sufficient linearity, except for switches $S_{BT1/2}$, which required the use of bootstrapped switches. Each sampling capacitor $C_{S1\text{-}4}$ has a size of 200 fF, to meet the required noise specification for a 14 bit resolution. The OTA is realized as a folded cascode wit SC CMFB, since the ADC requires a maximum peak-to-peak differential input voltage of $V_{pp,max} = \pm 2\,V$. It has a total current consumption 57.6 µA and achieves an open-loop gain of $A_0 = 74\,dB$, a gain-bandwidth of $GBW = 200\,MHz$ and a phase margin of 75°, when loaded with the sampling capacitors of the ADCs first integrator $C_{int1/2} = 40\,fF$ and the parasitic capacitance of the bootstrapped switches $S_{BT1\text{-}4}$. This high speed is required, since the OTA must charge the input capacitor of the ADCs first integrator with the full ADC accuracy within $\frac{T_S}{2} = \frac{1}{2 \cdot 30\,MHz} = 16\,ns$, as indicated in the ADC drawing in Figure 5.23.



(a) Simulation with transient noise.

(b) Simulation without noise.

FIGURE 5.24: Simulated performance of the ADC, including the multiplexed S/H.

Figure 5.24 shows the simulated performance of the ADC, which is driven by the presented S/H amplifier. When simulated with transient noise, a Signal-to-Noise-and-Distortion-Ratio (SNDR) of 75.4 dB is achieved with a $4\,V_{pp}$ peak-to-peak input signal, which is limited by the thermal noise of the driving stage. This results in an input

referred noise of less than 0.1 μV_{rms} for both LFP and AP channel, if the maximum gain is selected ($A_{LFP} = 57$ dB, $f_{LFP} = 0.2$ Hz - 200 Hz; $A_{AP} = 69$ dB, $f_{AP} = 200$ Hz - 10 kHz).

The complete recording channel has an input referred noise of 2.9 μV_{rms} in the LFP channel and 3.3 μV_{rms} in the AP channel for the same bandwidth and gain selection as stated above. Therefore, the input referred noise contribution of the designed ADC is negligible. The maximum achievable linearity of the recording channel was measured to be slightly above 60 dB in untuned mode (c.f. section 3.3) for a 4 mV_{pp} input signal, dominated by the pseudo resistor in the LNA feedback. For the ADC, a Total Harmonic Distortion (THD) of 89.6 dB was calculated from the noiseless simulation shown in Figure 5.24(b) for an input signal at the ADC of 4 V_{pp}. This clearly shows, that the linearity of the overall recording chain will be limited by the neural recorder and the overall performance will not be deteriorated by the ADC performance.

Since the overall performance is set by the preceding stages, no further power is spent in the ADC and its driver, since any improvement in noise and linearity would not improve the system performance, but only increase power and area consumption. Figure 5.25 and table 5.5 list the overall power consumption of the ADC, as well as its different building blocks.

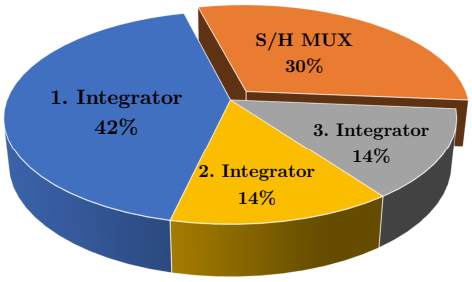


FIGURE 5.25: ADC and S/H power share.

Block	Power
ADC	329 µW
1st integrator	173 µW
2nd integrator	78 µW
3rd integrator	78 µW
S/H-MUX	173 µW

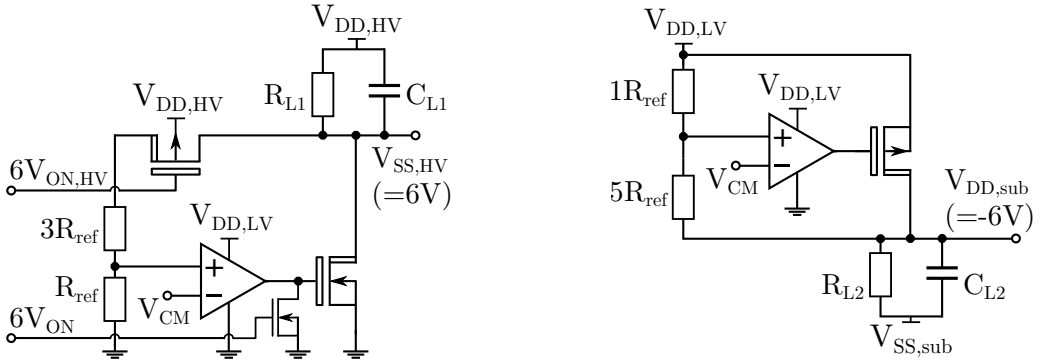
TABLE 5.5: ADC and S/H power consumption.

The total power consumption of one ADC including the multiplexing S/H driver sum up to 570 µW. As shown in Figure 5.25, the largest power consumer is the first integrator of the ADC, followed by the driving circuit. This is reasonable, as in contrast to the second and third integrator, the aforementioned circuits do not profit from noise shaping, which results in the highest noise and speed requirements.

5.4 Supporting analog circuitry

5.4.1 Linear regulators

Two Low Dropout Regulators (LDOs) have been implemented on-chip to generate the ±6 V voltages for the floating HV domains. Figure 5.26 shows the schematic level implementation, where matching poly resistors have been used in the feedback, to adjust the desired output voltage.



(a) +6 V LDO with power down.

(b) -6 V LDO.

FIGURE 5.26: LDOs for the ±6 V supply levels.

Both LDOs have a HV quiescent current of 9 µA under no load condition, which is set by the resistors $R_{L1/2} = 330\,k\Omega$ and require a stabilization capacitor of $C_{L1} = 130\,pF$ and $C_{L2} = 260\,pF$ respectively. The minimum resistor is required to keep the HV devices biased without load, by providing a minimum current of 1.2 µA through the pass devices, since the output current is heavily dependent on the number of active channels and whether the SoC is in recording or stimulation mode. The +6 V LDO can sink a maximum current of 200 µA, which is sufficient to operate all stimulator channels at the same time. Since the -6 V supply is required for all full scale LS, it can supply a maximum current of 400 µA, in order to provide enough headroom for dynamic switching currents. Both error amplifiers are implemented as single stage OTAs with current mirror load and have a combined current consumption of 25 µA from the $V_{DD,LV}$ supply, which can be reduced to 16 µA by shutting down the +6 V supply.

In order to save power, the +6 V LDO offers a sleep mode, where the biasing current of the error amplifier is shut down, the gate of the pass device is tied to ground and the HV switch in the feedback loop is opened. Thereby its power consumption is reduced to negligible leakage currents and the +6 V supply is pulled to $V_{DD,HV}$ over R_{L1}. This state is used to safe power during recording periods, since the +6 V supply is only required for stimulation. However, the -6 V is not implemented with a shut-down, since this voltage is required for a safe operation of the full scale LS, which was described in subsection 4.1.2.

These LSs are required to generate the switching signals for the HV blanking switches and must therefore be working in recording mode as well.

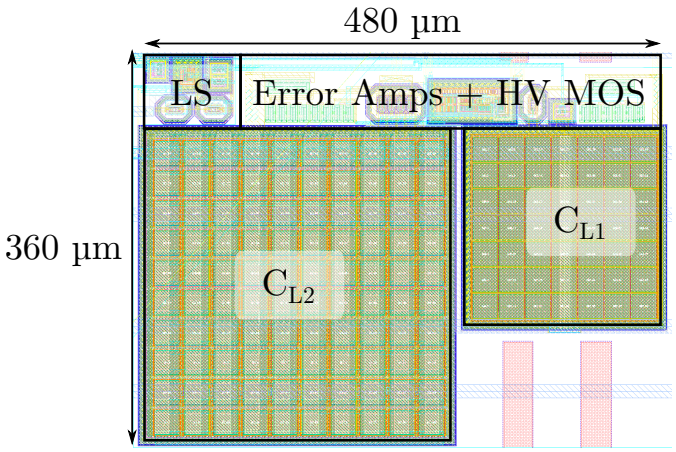


FIGURE 5.27: Layout of the two LDOs.

Figure 5.27 shows the layout of the two LDOs, including the LS required to generate the HV control signal $6V_{ON,HV}$, which has an overall size of 480 µm x 360 µm. It can be clearly seen, that the size is dominated by the big output capacitors $C_{L1/2}$, which have been implemented as MOS capacitors to achieve maximum capacitance per area.

5.4.2 Reference circuits

Reference voltage generator

In order to operate the regulated, triode current mirrors in the stimulator output stage (c.f. section 4.1), reference voltages of $V_{ref1} = V_{DD,LV}$ - 300 mV, $V_{ref2} = V_{DD,HV}$ - 200 mV and $V_{ref3} = V_{SS,sub} + 300$ mV need to be generated. However, the dropout of 200/300 mV is too low, to use a simple MOS diode which is driven by a current source, since the used transistors have a threshold voltage of more than 600 mV. Therefore, the circuit shown in Figure 5.28 was implemented.

As both implementations work in the same way, only the voltages of the left circuit will be calculated. Additionally, it is assumed, that all transistors have approximately the same threshold voltage V_{th} and that $(W/L)_1 \leq (W/L)_2$. Applying Kirchhoff's loop law leads to the following relation:

$$\begin{aligned} V_{out} &= V_{SS} + (V_{GS1} - V_{GS2}) \\ \Rightarrow V_{out} &= V_{SS} + (V_{OD1} + V_{th} - (V_{OD2} + V_{th})) \end{aligned} \tag{5.1}$$

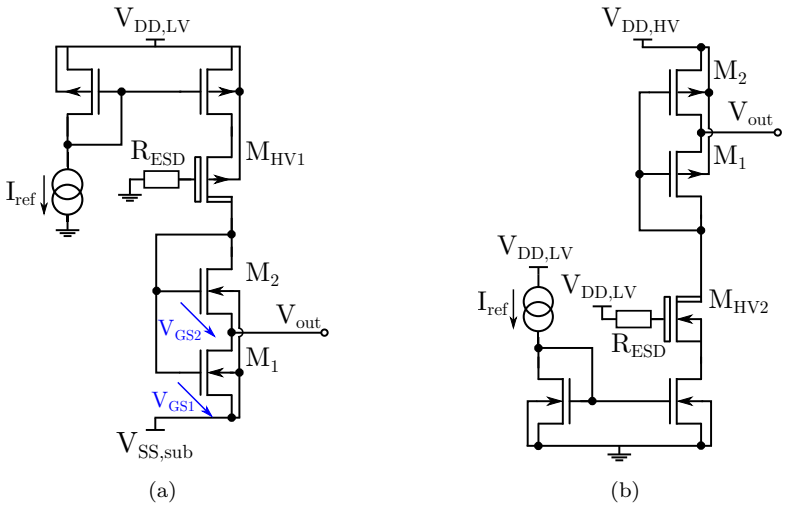


FIGURE 5.28: Reference voltage generation for the regulated, triode current mirror.

Therefore, the limiting threshold voltage cancels out in this implementation and V_{Out} can be set to the desired value over the different sizing of the two transistors.

Reference current generator

The standard gm-reference circuit, shown in Figure 5.29, is used to generate the biasing current for the whole chip. Since the implant will be operated in a temperature stable environment, no ambient temperature compensation was used for the sake of simplicity.

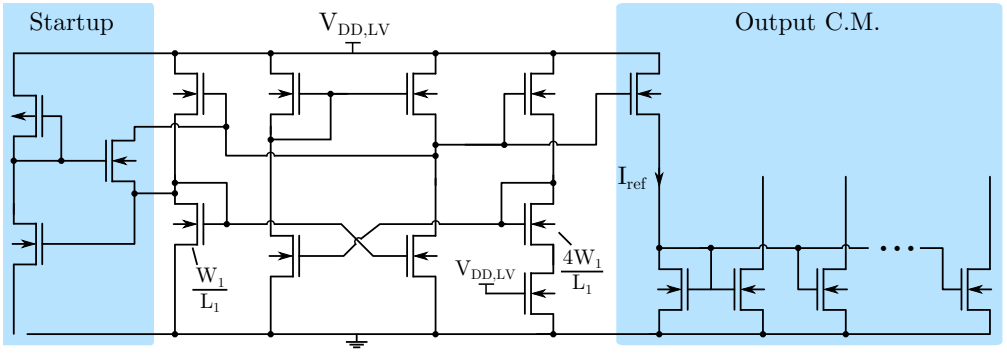


FIGURE 5.29: Beta multiplier for reference current generation.

The gm-reference generates a nominal reference current $I_{ref} = 15\,\mu A$, which is mirrored with a 3:1 ratio in the output current mirror. The resulting 5 µA reference currents are further distributed to 5 reference current mirrors, which generate the required 1 µA, switchable reference currents for the single channels.

5.5 Summary

In this chapter, the final, fully integrated, bidirectional neuromodulator was presented. It includes 32 front-end channels, which provide recording with a gain of up to 57 dB in the LFP band and 69 dB in the AP band with an integrated noise of 2.9 μV_{rms} (0.5 Hz - 200 Hz) and 3.3 μV_{rms} (200 Hz - 7.5 kHz) respectively. Each channel features an independent, biphasic HV stimulator, which can be reconfigured between current and voltage mode stimulation. By using a $\pm$ 9 V stimulation supply, a maximum stimulation voltage of $\pm$ 8 V can be generated, while the current stimulator features a maximum output current of $\pm$ 10.2 mA. In order to provide almost arbitrary stimulation waveforms, a dedicated, on-chip control logic provides programmable, digital waveform synthesis.

Two multiplexed, incremental $\Delta\Sigma$-ADCs were implemented to digitize the acquired neural signals from all 32 channels with a sampling rate of 20 $\frac{kS/s}{ch}$. The ADC together with the multiplexing driver S/H was simulated with a THD of 90 dB and a SNDR of 75 dB, resulting in an effective resolution of more than 12.1 bit.

Table 5.6 compares the implemented SoC to the SoA. Except for the ADC, all listed values are measured values from the implemented, low-channel count prototypes.

	JSSC '11 [81]	ISSCC '16 [21]	VLSI '17 [44]	JSSC '14 [82]	ESSCIRC '14 [55]	TBioCAS '16 [83]	This work
No. Ch. (Rec/Stim)	8/8	16/160†	64/4	4/2+8	32/1	4/4	32/32
Area/ch.	0.51 mm^2	-	-	0.18 mm^2††	0.33 mm^2	0.12 mm^2	0.46 mm^2
Tech.	0.35 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Stimulator							
On-Chip /Ext.	On-Chip	On-Chip	On-Chip	On-Chip	Ext.	On-Chip	On-Chip
Supply [V]	5.05	±(6...12)	12	5	18	5	±9 V
Stim. mode	CCS	CCS	CCS	CCS	CCS/CVS	CCS	CCS/CVS
$I_{Stim,MAX}$	94.5 µA	0.5 mA	5.04 mA	116 µA/ 4.2 mA	15 mA	0.25 mA	10.2 mA
$V_{Stim,MAX}$	-	-	-	-	18 V	-	±8 V
Stim. wvfrm.	Square	Square	Arbitrary	Arbitrary	Arbitrary	Arbitrary	Arbitrary
Wvfrm. gen.	On-Chip	On-Chip	On-Chip	On-Chip	Ext. analog	On-Chip	On-Chip
Recorder							
Power [µW/ch]	19.9 LNA + HP	5.4 LNA + LP	8 LNA + ADC	245 LNA + ADC	2 · 48 Ch. + Driver	5.5 bioADC	11.8 + 40 LNA + SC-filter
Input noise [μV_{rms}]	3.12	7.68	1.6	6.3	4.67	1.0	2.9/3.2 LFP/AP
BW	1.1 Hz - 12 kHz	5 Hz - 7 kHz	<1 Hz - 500 Hz	0.6 Hz - 6 kHz	0.2 Hz - 7.5 kHz	0.25 Hz - 250 Hz	0.2 Hz - 7.5 kHz
NEF	2.68 LNA+HP	6.2	7.8 LNA+ADC	3.76	3.19 LNA*	4.67 ADC	3.19 LNA*
ADC	On-Chip	On-Chip	On-Chip	On-Chip	Ext.	On-Chip	On-Chip
ENoB	9.2 bit	8.5 bit	12 bit**	8 bit	12 bit	9.4 bit	12.1 bit
f_S/Ch.	35.7 kS/s	nA	1 kS/s	25 kS/s	20 kS/s	0.5 kS/s	20 kS/s

†: 40 current drivers with 1:4 Demux ††: Stim. output stage
*: AP band only **: Estimated from spectrum

TABLE 5.6: Performance compared to the state of the art

Chapter 6

Conclusion and outlook

6.1 Conclusion

In this work, a fully integrated, bidirectional neural interface SoC has been developed and is manufactured, with an overall die size of 4.65 mm x 5.3 mm. It features 32 independent, AC coupled recording channels, which achieve a SoA noise efficiency factor and feature a digitally adjustable gain and recording bandwidth for maximum flexibility. Two on-chip I$\Delta\Sigma$-ADCs were implemented, which digitize the acquired signals with a sampling rate of $\frac{20^{\mathrm{kS/s}}}{\mathrm{channel}}$, achieving a SNDR of 75.4 dB and a linearity of 89.6 dB. A HV compliant interface circuit allows the on-chip combination of each recording channel with a novel HV stimulator that provides an independent, arbitrary stimulation waveform at each recording channel with outstandingly low area and power consumption in voltage or current mode.

The development of the recording channel was based on the work presented in [12] and is an improved version with extended functionality. By careful redesign, $1/f$ noise could be reduced in the LFP band, without sacrificing additional power. This led to an overall power consumption of 52 µW per channel, including the spectral separation filters and an input referred noise of 2.9 μV_{rms} in the LFP band (0.2 Hz - 200 Hz) and 3.2 μV_{rms} in the AP band (0.2 kHz - 7.5 kHz).

Since the used pseudo-resistor based architecture comes with a relatively large uncertainty in the location of the high-pass cut-off frequency, an on-chip tuning mechanism was implemented. It uses a SC charge redistribution DAC, which allows to digitally adjust the gate-source voltage V_{GS} of the pseudo-resistor and thereby change its absolute value. This architecture comes with three major advantages: First, the tuning requires an additional power consumption of only 4.9 µW for the tuning of 4 pseudo resistors,

including the analog to digital conversion. Second, the linear adjustment of V_{GS} results in an exponential tuning characteristic, which provides small tuning steps for low cut-off frequencies together with a large tuning range from 200 mHz to 4 kHz. Third, the SC implementation allows to almost completely shut down the tuning circuitry, which results in a standby power consumption of only 600 nW if no tuning is required.

In addition to the improvement in signal quality, a novel electrode estimation technique was implemented in the recorder front-end. Similar to the approach first presented in [95] it uses an impedance estimation, based on the impulse response of the electrode. However, in contrast to this implementation, we added a low gain mode to the low noise amplifier of the recorder channel, which allows to reuse it to record said impulse response. This allows to monitor the impedance at every electrode site, thus further improving patient safety.

The on-chip neural stimulator was implemented with a separate HV output supply of ± 9 V, while leaving the recording circuitry and the stimulation waveform generation in the LV domain. Thereby an area consumption of only 0.46 mm^2 per channel could be achieved, for a maximum stimulation current as high as $\pm$ 10.2 mA with a voltage compliance of ± 8 V. Together with a dynamic range of 50 dB in the stimulation currents, this provides a large degree of freedom in the design of experiments.

Lastly, a semi-digital feedback loop that allows to reconfigure the stimulator from current mode into voltage mode was developed. This allows to fully reuse the area consuming HV output stage of the stimulator, while achieving power efficient class-B operation. Thereby, the stimulator is amongst the few published systems that allow both, current and voltage mode stimulation, while significantly improving power and area consumption. Additionally, the implementation provides improved patient safety, since its stability can be analyzed using well known concepts from SDM theory, which has been presented within this thesis. This reconfigurability gives neurologists the chance to directly compare the effects of voltage and current mode stimulation, which allows to transfer knowledge from previous experiments to new, safer stimulation methods.

6.2 Outlook

As mentioned several times throughout the thesis, wireless, transcutaneous data transmission becomes a major challenge for multichannel neural implants. If we want to assure, that no useful information is lost, the two ADCs of the developed SoC produce a minimum, combined data rate of $20\,\frac{\mathrm{kS/s}}{\mathrm{ch}} \cdot 32\,\mathrm{ch} \cdot 14\,\mathrm{bit} = 8.96\,\mathrm{Mbit/s}$, which is way beyond the data rate of commercial, low power data transmitters, e.g. Bluetooth low energy. Although the implemented filter structure allows to simply reduce the data rate, by sub-sampling if only the LFP band is selected, however it is usually desired to extract the whole neural signal during experiments, in order to acquire as much information as possible. Therefore, the work on an IR-UWB data link was already started during this thesis.

FIGURE 6.1: Miniaturized IR-UWB transmitter [18].

An existing IR-UWB transmitter, which was realized in a 0.8 µm SiGe technology and published in [110], was used to realize a first, miniaturized transmitter prototype, shown in Figure 6.1. Based on the promising results, a CMOS based transmitter and receiver is currently designed in the same technology as the SoC. This would allow data rates of more than 100 Mbit/s with a power consumption of less than 10 mW, providing sufficient bandwidth for more several hundred channels. Additionally, the use of the same CMOS technology allows to integrate the telemetry unit on the same chip in future implementations, allowing to further shrink the implant size.

A second, major opportunity for size and power improvements is the implants power management. At the moment it is realized using discrete, linear regulators and charge pumps, which consume a relatively large amount of space and lack in flexibility. An integrated power management solution would first of all reduce the amount of components within the implant and thereby reduce its size, while improving the reliability. Second, an application specific implementation can provide a feedback input, which would allow to adjust the stimulators supply voltage to the electrode impedance, as it was presented

in [73]. This would yield a significant improvement in overall power efficiency, thus decreasing potentially harmful heat dissipation to the surrounding tissue and increasing battery lifetime.

With these improvements, a new generation of neural implants is possible, which allows a more detailed insight into the working mechanisms of the CNS, by providing increased spatiotemporal resolution. Furthermore reduced power consumption, improved reliability and new safety features allow longterm implantation, making the next step towards a broad, clinical application.

Bibliography

[1] Wikipedia. Action potential. http://www.wikipedia.org, April 2019. URL https://en.wikipedia.org/wiki/Action_potential.

[2] Norberto M. Grzywacz and Mónica Padilla. *Biological Neural Control*. American Cancer Society, 2006. ISBN 9780471740360. doi: 10.1002/9780471740360.ebs0828. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/9780471740360.ebs0828.

[3] Christian Henle, Martin Schuettler, Jörn Rickert, and Thomas Stieglitz. *Towards Electrocorticographic Electrodes for Chronic Use in BCI Applications*, pages 85–103. Springer Berlin Heidelberg, Berlin, Heidelberg, 2013. ISBN 978-3-642-29746-5. doi: 10.1007/978-3-642-29746-5_5. URL https://doi.org/10.1007/978-3-642-29746-5_5.

[4] Shigeyoshi Fujisawa, Asohan Amarasingham, Matthew T. Harrison, and György Buzsáki. Behavior-dependent short-term assembly dynamics in the medial prefrontal cortex. *Nature Neuroscience*, 11:823 EP –, May 2008. URL https://doi.org/10.1038/nn.2134. Article.

[5] Shigeyoshi Fujisawa, Asohan Amarasingham, Matthew T. Harrison, and György Buzsáki. Simultaneous electrophysiological recordings of ensembles of isolated neurons in rat medial prefrontal cortex and intermediate CA1 area of the hippocampus during a working memory task. CRCNS.org, 2015. URL http://dx.doi.org/10.6080/K01V5BWK.

[6] Kenneth W. Horch and Gurpreet S. Dhillon, editors. *Neuroprosthetics - Theory and Practice*, chapter 3.1, pages 477–480. World Scientific Publishing Co. Pte. Ltd., 2004.

[7] Rajmohan Bhandari, Sandeep Negi, and Florian Solzbacher. Wafer-scale fabrication of penetrating neural microelectrode arrays. *Biomedical Microdevices*, 12(5): 797–807, October 2010. ISSN 1572-8781. doi: 10.1007/s10544-010-9434-1. URL https://doi.org/10.1007/s10544-010-9434-1.

[8] CorTEC GmbH. AirRay Cortical Electrode - Soft, Thin and Flexible Material Structure. cortec-neuro.com, 2018. URL `https://cortec-neuro.com/solutions/clinical-use`.

[9] R. R. Harrison. A Versatile Integrated Circuit for the Acquisition of Biopotentials. In *2007 IEEE Custom Integrated Circuits Conference*, pages 115–122, September 2007. doi: 10.1109/CICC.2007.4405694.

[10] H. Chandrakumar and D. Marković. An 80-mVpp Linear-Input Range, 1.6- GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference. *IEEE Journal of Solid-State Circuits*, 52(11):2811–2828, November 2017. ISSN 0018-9200. doi: 10.1109/JSSC.2017.2753824.

[11] H. Lee, K. Y. Kwon, W. Li, and M. Ghovanloo. A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep Brain Stimulation. *IEEE Journal of Solid-State Circuits*, 50(1):360–374, January 2015. ISSN 0018-9200. doi: 10.1109/JSSC.2014.2355814.

[12] Ulrich Bihr. *Low Power Multichannel IC for Biomedical Bidirectional Neural Implants*. PhD thesis, University of Ulm, 2014.

[13] M. Haas, J. Anders, and M. Ortmanns. A bidirectional neural interface featuring a tunable recorder and electrode impedance estimation. In *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 372–375, October 2016. doi: 10.1109/BioCAS.2016.7833809.

[14] M. Haas, P. Vogelmann, and M. Ortmanns. A Neuromodulator Frontend With Reconfigurable Class-B Current and Voltage Controlled Stimulator. *IEEE Solid-State Circuits Letters*, 1(3):54–57, March 2018. ISSN 2573-9603. doi: 10.1109/LSSC.2018.2827885.

[15] M. Haas and M. Ortmanns. A floating high-voltage level-shifter with high area efficiency for biomedical implants. In *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pages 1–4, June 2016. doi: 10.1109/PRIME.2016.7519451.

[16] M. Haas, U. Bihr, J. Anders, and M. Ortmanns. A bidirectional neural interface IC with high voltage compliance and spectral separation. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2743–2746, May 2016. doi: 10.1109/ISCAS.2016.7539160.

[17] M. Haas and M. Ortmanns. Efficient Implementation and Stability Analysis of a HV-CMOS Current/Voltage Mode Stimulator. In *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, October 2018.

[18] M. Haas, B. Schweizer, J. Anders, and M. Ortmanns. A miniaturized UWB antenna for implantable data telemetry. In *2017 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 1086–1089, July 2017. doi: 10.1109/EMBC.2017.8037016.

[19] Leigh R. Hochberg, Mijail D. Serruya, Gerhard M. Friehs, Jon A. Mukand, Maryam Saleh, Abraham H. Caplan, Almut Branner, David Chen, Richard D. Penn, and John P. Donoghue. Neuronal ensemble control of prosthetic devices by a human with tetraplegia. *Nature*, 442:164 EP –, July 2006. URL `https://doi.org/10.1038/nature04970`. Article.

[20] S. Ha, A. Akinin, J. Park, C. Kim, H. Wang, C. Maier, P. P. Mercier, and G. Cauwenberghs. Silicon-Integrated High-Density Electrocortical Interfaces. *Proceedings of the IEEE*, 105(1):11–33, January 2017. ISSN 0018-9219. doi: 10.1109/JPROC.2016.2587690.

[21] Y. Lo, C. Chang, Y. Kuan, S. Culaclii, B. Kim, K. Chen, P. Gad, V. R. Edgerton, and W. Liu. 22.2 A 176-channel 0.5cm3 0.7g wireless implant for motor function recovery after spinal cord injury. In *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 382–383, January 2016. doi: 10.1109/ISSCC.2016.7418067.

[22] H. Kassiri, N. Soltani, M. T. Salam, J. L. P. Velazquez, and R. Genov. Battery-less modular responsive neurostimulator for prediction and abortion of epileptic seizures. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1298–1301, May 2016. doi: 10.1109/ISCAS.2016.7527486.

[23] X. Liu, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel. Design of a Closed-Loop, Bidirectional Brain Machine Interface System With Energy Efficient Neural Feature Extraction and PID Control. *IEEE Transactions on Biomedical Circuits and Systems*, 11(4):729–742, August 2017. ISSN 1932-4545. doi: 10.1109/TBCAS.2016.2622738.

[24] J. Massachi, Y. Lo, P. Wang, and W. Liu. A Wireless Platform to Support Pre-Clinical Trial of Neural Implant for Spinal Cord Injury. In *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 5487–5490, July 2018. doi: 10.1109/EMBC.2018.8513636.

[25] Sumio Uematsu, Kunitada Hara, Robert S. Fisher, Ronald Lesser, Gregory L. Krauss, Robert W. Webber, Eileen P. Vining, and Barry Gordon. Motor and Sensory Cortex in Humans: Topography Studied with Chronic Subdural Stimulation. *Neurosurgery*, 31(1):59–72, July 1992. ISSN 0148-396X. doi: 10.1097/00006123-199207000-00009. URL `https://dx.doi.org/10.1097/00006123-199207000-00009`.

[26] Aysegul Gunduz, Peter Brunner, Amy Daitch, Eric Leuthardt, Anthony Ritaccio, Bijan Pesaran, and Gerwin Schalk. Neural Correlates of Visual–Spatial Attention in Electrocorticographic Signals in Humans. *Frontiers in Human Neuroscience*, 5: 89, 2011. ISSN 1662-5161. doi: 10.3389/fnhum.2011.00089. URL `https://www.frontiersin.org/article/10.3389/fnhum.2011.00089`.

[27] M. R. Pazhouhandeh, H. Kassiri, A. Shoukry, I. Wesspapir, P. Carlen, and R. Genov. Artifact-Tolerant Opamp-Less Delta-Modulated Bidirectional Neuro-Interface. In *2018 IEEE Symposium on VLSI Circuits*, pages 127–128, June 2018. doi: 10.1109/VLSIC.2018.8502286.

[28] H. Kassiri, M. T. Salam, M. R. Pazhouhandeh, N. Soltani, J. L. Perez Velazquez, P. Carlen, and R. Genov. Rail-to-Rail-Input Dual-Radio 64-Channel Closed-Loop Neurostimulator. *IEEE Journal of Solid-State Circuits*, 52(11):2793–2810, November 2017. ISSN 0018-9200. doi: 10.1109/JSSC.2017.2749426.

[29] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni. A Miniaturized System for Spike-Triggered Intracortical Microstimulation in an Ambulatory Rat. *IEEE Transactions on Biomedical Engineering*, 58(9):2589–2597, September 2011. ISSN 0018-9294. doi: 10.1109/TBME.2011.2159603.

[30] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher. A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System. *IEEE Journal of Solid-State Circuits*, 42(1):123–133, January 2007. ISSN 0018-9200. doi: 10.1109/JSSC.2006.886567.

[31] L. H. Jung, N. Shany, T. Lehmann, P. Preston, N. H. Lovell, and G. J. Suaning. Towards a chip scale neurostimulator: System architecture of a current-driven 98 channel neurostimulator via a two-wire interface. In *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pages 6737–6740, August 2011. doi: 10.1109/IEMBS.2011.6091662.

[32] Y. Lo, K. Chen, P. Gad, and W. Liu. A Fully-Integrated High-Compliance Voltage SoC for Epi-Retinal and Neural Prostheses. *IEEE Transactions on Biomedical Circuits and Systems*, 7(6):761–772, December 2013. ISSN 1932-4545. doi: 10.1109/TBCAS.2013.2297695.

[33] Mesut Sahin and Yanmei Tie. Non-rectangular waveforms for neural stimulation with practical electrodes. *Journal of Neural Engineering*, 4(3):227, 2007. URL http://stacks.iop.org/1741-2552/4/i=3/a=008.

[34] Amorn Wongsarnpigoon and Warren M Grill. Energy-efficient waveform shapes for neural stimulation revealed with a genetic algorithm. *Journal of Neural Engineering*, 7(4):046009, 2010. URL http://stacks.iop.org/1741-2552/7/i=4/a=046009.

[35] F. Preda, C. Cavandoli, C. Lettieri, M. Pilleri, A. Antonini, R. Eleopra, M. Mondani, A. Martinuzzi, S. Sarubbo, G. Ghisellini, A. Trezza, M. A. Cavallo, A. Landi, and M. Sensi. Switching from constant voltage to constant current in deep brain stimulation: a multicenter experience of mixed implants for movement disorders. *European Journal of Neurology*, 23(1):190–195, 2016. doi: 10.1111/ene.12835. URL https://onlinelibrary.wiley.com/doi/abs/10.1111/ene.12835.

[36] Peter Langhorne, Fiona Coupar, and Alex Pollock. Motor recovery after stroke: a systematic review. *The Lancet Neurology*, 8(8):741–754, 2009. ISSN 1474-4422. doi: https://doi.org/10.1016/S1474-4422(09)70150-4. URL http://www.sciencedirect.com/science/article/pii/S1474442209701504.

[37] Antal Berenyi, Mariano Belluscio, Dun Mao, and György Buzsaki. Closed-Loop Control of Epilepsy by Transcranial Electrical Stimulation. *Science*, 337(6095): 735–737, 2012. ISSN 0036-8075. doi: 10.1126/science.1223154. URL http://science.sciencemag.org/content/337/6095/735.

[38] Martha J. Morrell. Responsive cortical stimulation for the treatment of medically intractable partial epilepsy. *Neurology*, 2011. ISSN 0028-3878. doi: 10.1212/WNL.0b013e3182302056. URL http://n.neurology.org/content/early/2011/09/14/WNL.0b013e3182302056.

[39] A. Wagle Shukla and M. S. Okun. State of the Art for Deep Brain Stimulation Therapy in Movement Disorders: A Clinical and Technological Perspective. *IEEE Reviews in Biomedical Engineering*, 9:219–233, 2016. ISSN 1937-3333. doi: 10.1109/RBME.2016.2588399.

[40] A. Mohammed, M. Zamani, R. Bayford, and A. Demosthenous. Toward On-Demand Deep Brain Stimulation Using Online Parkinson's Disease Prediction Driven by Dynamic Detection. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 25(12):2441–2452, December 2017. ISSN 1534-4320. doi: 10.1109/TNSRE.2017.2722986.

[41] Patrick Kwan, Steven C. Schachter, and Martin J. Brodie. Drug-Resistant Epilepsy. *New England Journal of Medicine*, 365(10):919–926, 2011. doi: 10.1056/NEJMra1004418. URL `https://doi.org/10.1056/NEJMra1004418`. PMID: 21899452.

[42] Kelly E. Lyons and Rajesh Pahwa. Deep brain stimulation and tremor. *Neurotherapeutics*, 5(2):331–338, April 2008. ISSN 1878-7479. doi: 10.1016/j.nurt.2008.01.004. URL `https://doi.org/10.1016/j.nurt.2008.01.004`.

[43] M. E. Halpern* and J. Fallon. Current Waveforms for Neural Stimulation-Charge Delivery With Reduced Maximum Electrode Voltage. *IEEE Transactions on Biomedical Engineering*, 57(9):2304–2312, September 2010. ISSN 0018-9294. doi: 10.1109/TBME.2010.2053203.

[44] B. C. Johnson, S. Gambini, I. Izyumin, A. Moin, A. Zhou, G. Alexandrov, S. R. Santacruz, J. M. Rabaey, J. M. Carmena, and R. Muller. An implantable 700µW 64-channel neuromodulation IC for simultaneous recording and stimulation with rapid artifact recovery. In *2017 Symposium on VLSI Circuits*, pages C48–C49, June 2017. doi: 10.23919/VLSIC.2017.8008543.

[45] J. N. Y. Aziz, K. Abdelhalim, R. Shulyzki, R. Genov, B. L. Bardakjian, M. Derchansky, D. Serletis, and P. L. Carlen. 256-Channel Neural Recording and Delta Compression Microsystem With 3D Electrodes. *IEEE Journal of Solid-State Circuits*, 44(3):995–1005, March 2009. ISSN 0018-9200. doi: 10.1109/JSSC.2008.2010997.

[46] S. Kim, P. Tathireddy, R. A. Normann, and F. Solzbacher. In vitro and in vivo study of temperature increases in the brain due to a neural implant. In *2007 3rd International IEEE/EMBS Conference on Neural Engineering*, pages 163–166, May 2007. doi: 10.1109/CNE.2007.369637.

[47] S. Kim, R. A. Normann, R. Harrison, and F. Solzbacher. Preliminary Study of the Thermal Impact of a Microelectrode Array Implanted in the Brain. In *2006 International Conference of the IEEE Engineering in Medicine and Biology Society*, pages 2986–2989, August 2006. doi: 10.1109/IEMBS.2006.260307.

[48] Amos Arieli, Alexander Sterkin, Amiram Grinvald, and Ad Aertsen. Dynamics of Ongoing Activity: Explanation of the Large Variability in Evoked Cortical Responses. *Science*, 273(5283):1868–1871, 1996. ISSN 0036-8075. doi: 10.1126/science.273.5283.1868. URL `http://science.sciencemag.org/content/273/5283/1868`.

[49] R. R. Harrison. The Design of Integrated Circuits to Observe Brain Activity. *Proceedings of the IEEE*, 96(7):1203–1216, July 2008. ISSN 0018-9219. doi: 10.1109/JPROC.2008.922581.

[50] Medtronic GmbH. Neurostimulationssysteme - Activa PC. cmedtronic.com, 2018. URL `https://www.medtronic.com/de-de/fachkreise/produkte/neurologie-schmerztherapie/neurostimulationssysteme-zur-tiefen-hirnstimulation.html`.

[51] S. Brenna, F. Padovan, A. Neviani, A. Bevilacqua, A. Bonfanti, and A. L. Lacaita. A 64-Channel 965-μWNeural Recording SoC With UWB Wireless Transmission in 130-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 63(6):528–532, June 2016. ISSN 1549-7747. doi: 10.1109/TCSII.2016.2530882.

[52] N. Soltani, H. Kassiri, H. M. Jafari, K. Abdelhalim, and R. Genov. 0.13μm CMOS 230Mbps 21pJ/b UWB-IR transmitter with 21.3efficiency. In *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, pages 352–355, September 2015. doi: 10.1109/ESSCIRC.2015.7313900.

[53] Y. Lin, S. Park, X. Chen, D. Wentzloff, and E. Yoon. 4.32-pJ/b, Overlap-Free, Feedforward Edge-Combiner-Based Ultra-Wideband Transmitter for High-Channel-Count Neural Recording. *IEEE Microwave and Wireless Components Letters*, 28(1):52–54, January 2018. ISSN 1531-1309. doi: 10.1109/LMWC.2017.2776947.

[54] M. R. Yuce, W. Liu, M. S. Chae, and J. S. Kim. A Wideband Telemetry Unit for Multi-Channel Neural Recording Systems. In *2007 IEEE International Conference on Ultra-Wideband*, pages 612–617, September 2007. doi: 10.1109/ICUWB.2007.4381017.

[55] U. Bihr, J. Anders, J. Rickert, M. Schuettler, A. Moeller, K. H. Boven, J. Becker, and M. Ortmanns. A neural recorder IC with HV input multiplexer for voltage and current stimulation with 18V compliance. In *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, pages 103–106, September 2014. doi: 10.1109/ESSCIRC.2014.6942032.

[56] M. Trepel. *Neuroanatomie - Struktur und Funktion*. Urban & Fischer, 2004.

[57] M. Schünke, E. Schulte, U. Schumacher, M. Voll, and K. Wesker. *Prometheus - Kopf und Neuroa*. Thieme, 2006.

[58] M. H. Nazari, H. Mazhab-Jafari, L. Leng, A. Guenther, and R. Genov. CMOS Neurotransmitter Microarray: 96-Channel Integrated Potentiostat With On-Die

Microsensors. *IEEE Transactions on Biomedical Circuits and Systems*, 7(3):338–348, June 2013. ISSN 1932-4545. doi: 10.1109/TBCAS.2012.2203597.

[59] Nikos K. Logothetis. What we can do and what we cannot do with fMRI. *Nature*, 453:869 EP –, June 2008. URL `https://doi.org/10.1038/nature06976`. Review Article.

[60] R. Quian Quiroga, Z. Nadasdy, and Y. Ben-Shaul. Unsupervised Spike Detection and Sorting with Wavelets and Superparamagnetic Clustering. *Neural Computation*, 16(8):1661–1687, 2004. doi: 10.1162/089976604774201631. URL `https://doi.org/10.1162/089976604774201631`.

[61] Stuart F. Cogan. Neural Stimulation and Recording Electrodes. *Annual Review of Biomedical Engineering*, 10(1):275–309, 2008. doi: 10.1146/annurev.bioeng.10.061807.160518. URL `https://doi.org/10.1146/annurev.bioeng.10.061807.160518`. PMID: 18429704.

[62] John Edward Brough Randles. Kinetics of rapid electrode reactions. *Discussions of the faraday society*, 1:11–19, 1947.

[63] W. Franks, I. Schenker, P. Schmutz, and A. Hierlemann. Impedance characterization and modeling of electrodes for biomedical applications. *IEEE Transactions on Biomedical Engineering*, 52(7):1295–1302, July 2005. ISSN 0018-9294. doi: 10.1109/TBME.2005.847523.

[64] Eric C Leuthardt, Gerwin Schalk, Jonathan R Wolpaw, Jeffrey G Ojemann, and Daniel W Moran. A brain–computer interface using electrocorticographic signals in humans. *Journal of Neural Engineering*, 1(2):63, 2004. URL `http://stacks.iop.org/1741-2552/1/i=2/a=001`.

[65] J D Simeral, S-P Kim, M J Black, J P Donoghue, and L R Hochberg. Neural control of cursor trajectory and click by a human with tetraplegia 1000 days after implant of an intracortical microelectrode array. *Journal of Neural Engineering*, 8(2):025027, 2011. URL `http://stacks.iop.org/1741-2552/8/i=2/a=025027`.

[66] T. Delbruck and C. A. Mead. Adaptive photoreceptor with wide dynamic range. In *Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94*, volume 4, pages 339–342 vol.4, May 1994. doi: 10.1109/ISCAS.1994.409266.

[67] R. R. Harrison and C. Charles. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE Journal of Solid-State Circuits*, 38(6):958–965, June 2003. ISSN 0018-9200. doi: 10.1109/JSSC.2003.811979.

[68] C. C. Enz and E. A. Vittoz. Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design. 2006. URL `http://infoscience.epfl.ch/record/149582`.

[69] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley, and A. Kelly. A 2μW100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials. *IEEE Journal of Solid-State Circuits*, 42(12): 2934–2945, December 2007. ISSN 0018-9200. doi: 10.1109/JSSC.2007.908664.

[70] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan. A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System. *IEEE Journal of Solid-State Circuits*, 45(4):804–816, April 2010. ISSN 0018-9200. doi: 10.1109/JSSC.2010.2042245.

[71] J. Xu, R. F. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, and C. Van Hoof. A160 μW8-Channel Active Electrode System for EEG Monitoring. *IEEE Transactions on Biomedical Circuits and Systems*, 5(6):555–567, December 2011. ISSN 1932-4545. doi: 10.1109/TBCAS.2011.2170985.

[72] J. Lee, Hyo-Gyuem Rhew, D. Kipke, and M. Flynn. A 64 Channelprogrammable closed-loop deep brain stimulator with 8 channel neural amplifier and logarithmic ADC. In *2008 IEEE Symposium on VLSI Circuits*, pages 76–77, June 2008. doi: 10.1109/VLSIC.2008.4585958.

[73] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns. A Neural Stimulator Frontend With High-Voltage Compliance and Programmable Pulse Shape for Epiretinal Implants. *IEEE Journal of Solid-State Circuits*, 47(1): 244–256, January 2012. ISSN 0018-9200. doi: 10.1109/JSSC.2011.2164667.

[74] I. Williams and T. G. Constandinou. An Energy-Efficient, Dynamic Voltage Scaling Neural Stimulator for a Proprioceptive Prosthesis. *IEEE Transactions on Biomedical Circuits and Systems*, 7(2):129–139, April 2013. ISSN 1932-4545. doi: 10.1109/TBCAS.2013.2256906.

[75] C. Lin, W. Chen, and M. Ker. Implantable Stimulator for Epileptic Seizure Suppression With Loading Impedance Adaptability. *IEEE Transactions on Biomedical Circuits and Systems*, 7(2):196–203, April 2013. ISSN 1932-4545. doi: 10.1109/TBCAS.2012.2200481.

[76] H. Kassiri, G. Dutta, N. Soltani, C. Liu, Y. Hu, and R. Genov. An impedance-tracking battery-less arbitrary-waveform neurostimulator with load-adaptive 20V voltage compliance. In *ESSCIRC Conference 2016: 42nd European Solid-State*

Circuits Conference, pages 225–228, September 2016. doi: 10.1109/ESSCIRC.2016.7598283.

[77] M. S. J. Steyaert and W. M. C. Sansen. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *IEEE Journal of Solid-State Circuits*, 22 (6):1163–1168, December 1987. ISSN 0018-9200. doi: 10.1109/JSSC.1987.1052869.

[78] R. Muller, S. Gambini, and J. M. Rabaey. A 0.013mm^2, 5μW, DC-Coupled Neural Signal Acquisition IC With 0.5 V Supply. *IEEE Journal of Solid-State Circuits*, 47(1):232–243, January 2012. ISSN 0018-9200. doi: 10.1109/JSSC.2011.2163552.

[79] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs. Sub-μVrms-Noise Sub-μW/Channel ADC-Direct Neural Recording With 200-mV/ms Transient Recovery Through Predictive Digital Autoranging. *IEEE Journal of Solid-State Circuits*, 53(11):3101–3110, November 2018. ISSN 0018-9200. doi: 10.1109/JSSC.2018.2870555.

[80] D. Han, Y. Zheng, R. Rajkumar, G. S. Dawe, and M. Je. A 0.45 V 100-Channel Neural-Recording IC With Sub-μW/Channel Consumption in 0.18 μm CMOS. *IEEE Transactions on Biomedical Circuits and Systems*, 7(6):735–746, December 2013. ISSN 1932-4545. doi: 10.1109/TBCAS.2014.2298860.

[81] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni. A Battery-Powered Activity-Dependent Intracortical Microstimulation IC for Brain-Machine-Brain Interface. *IEEE Journal of Solid-State Circuits*, 46(4):731–745, April 2011. ISSN 0018-9200. doi: 10.1109/JSSC.2011.2108770.

[82] H. Rhew, J. Jeong, J. A. Fredenburg, S. Dodani, P. G. Patil, and M. P. Flynn. A Fully Self-Contained Logarithmic Closed-Loop Deep Brain Stimulation SoC With Wireless Telemetry and Wireless Power Management. *IEEE Journal of Solid-State Circuits*, 49(10):2213–2227, October 2014. ISSN 0018-9200. doi: 10.1109/JSSC.2014.2346779.

[83] E. Greenwald, E. So, Q. Wang, M. Mollazadeh, C. Maier, R. Etienne-Cummings, G. Cauwenberghs, and N. Thakor. A Bidirectional Neural Interface IC With Chopper Stabilized BioADC Array and Charge Balanced Stimulator. *IEEE Transactions on Biomedical Circuits and Systems*, 10(5):990–1002, October 2016. ISSN 1932-4545. doi: 10.1109/TBCAS.2016.2614845.

[84] P. Amami, M. M. Mascia, A. Franzini, F. Saba, and A. Albanese. Shifting from constant-voltage to constant-current in Parkinson's disease patients with chronic stimulation. *Neurological Sciences*, 38(8):1505–1508, August 2017. ISSN

1590-3478. doi: 10.1007/s10072-017-2961-2. URL https://doi.org/10.1007/s10072-017-2961-2.

[85] C. Lettieri, S. Rinaldo, G. Devigili, F. Pisa, M. Mucchiut, E. Belgrado, M. Mondani, S. D'Auria, T. Ius, M. Skrap, and R. Eleopra. Clinical outcome of deep brain stimulation for dystonia: constant-current or constant-voltage stimulation? A non-randomized study. *European Journal of Neurology*, 22(6):919–926, 2015. doi: 10.1111/ene.12515. URL https://onlinelibrary.wiley.com/doi/abs/10.1111/ene.12515.

[86] M. Ortmanns, A. Rocke, M. Gehrke, and H. Tiedtke. A 232-Channel Epiretinal Stimulator ASIC. *IEEE Journal of Solid-State Circuits*, 42(12):2946–2959, December 2007. ISSN 0018-9200. doi: 10.1109/JSSC.2007.908693.

[87] Kriangkrai Sooksood, T. Stieglitz, and M. Ortmanns. An active approach for charge balancing in functional electrical stimulation. In *2009 IEEE International Symposium on Circuits and Systems*, pages 341–344, May 2009. doi: 10.1109/ISCAS.2009.5117755.

[88] K. Sooksood, T. Stieglitz, and M. Ortmanns. An Active Approach for Charge Balancing in Functional Electrical Stimulation. *IEEE Transactions on Biomedical Circuits and Systems*, 4(3):162–170, June 2010. ISSN 1932-4545. doi: 10.1109/TBCAS.2010.2040277.

[89] N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl. A 22 V Compliant 56μW Twin-Track Active Charge Balancing Enabling 100Correction in Biphasic Neural Stimulators. *IEEE Journal of Solid-State Circuits*, 53(8):2298–2310, August 2018. ISSN 0018-9200. doi: 10.1109/JSSC.2018.2828823.

[90] Willy M. C. Sansen, editor. *Analog design essentials*. Kluwer international series in engineering and computer science ; 859. Springer, Dordrecht, 2006. ISBN 0-387-25746-2. 777 Seiten.

[91] H. Kassiri, K. Abdelhalim, and R. Genov. Low-distortion super-GOhm subthreshold-MOS resistors for CMOS neural amplifiers. In *2013 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 270–273, October 2013. doi: 10.1109/BioCAS.2013.6679691.

[92] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad, and A. M. Sodagar. Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 1(4):546–556, December 2011. ISSN 2156-3357. doi: 10.1109/JETCAS.2011.2174492.

[93] A. Tajalli, Y. Leblebici, and E. J. Brauer. Implementing ultra-high-value floating tunable CMOS resistors. *Electronics Letters*, 44(5):349–350, February 2008. ISSN 0013-5194. doi: 10.1049/el:20082538.

[94] A. Uranga, J. Sacristan, T. Oses, and N. Barniol. Electrode–Tissue Impedance Measurement CMOS ASIC for Functional Electrical Stimulation Neuroprostheses. *IEEE Transactions on Instrumentation and Measurement*, 56(5):2043–2050, October 2007. ISSN 0018-9456. doi: 10.1109/TIM.2007.904479.

[95] Y. Lo, C. Chang, and W. Liu. Bio-impedance characterization technique with implantable neural stimulator using biphasic current stimulus. In *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pages 474–477, August 2014. doi: 10.1109/EMBC.2014.6943631.

[96] Michael Haas. Design and Layout of a Neural Stimulator Front-End in a 180nm HVCMOS Technology. Master's thesis, University of Ulm, 2013.

[97] N. Laotaveerungrueng, R. R. Lahiji, S. L. Garverick, and M. Mehregany. A high-voltage, high-current CMOS pulse generator ASIC for deep brain stimulation. In *2010 Annual International Conference of the IEEE Engineering in Medicine and Biology*, pages 1519–1522, August 2010. doi: 10.1109/IEMBS.2010.5626836.

[98] Y. Moghe, T. Lehmann, and T. Piessens. Nanosecond Delay Floating High Voltage Level Shifters in a 0.35 μm HV-CMOS Technology. *IEEE Journal of Solid-State Circuits*, 46(2):485–497, February 2011. ISSN 0018-9200. doi: 10.1109/JSSC.2010.2091322.

[99] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel. Low-power static and dynamic high-voltage CMOS level-shifter circuits. In *2008 IEEE International Symposium on Circuits and Systems*, pages 1946–1949, May 2008. doi: 10.1109/ISCAS.2008.4541825.

[100] R. Jacob Baker. *CMOS Circuit Design, Layout, and Simulation*, chapter Data Converter Architectures, pages 973–975. Wiley-IEEE Press, 2010.

[101] M. Ghovanloo and K. Najafi. A Modular 32-site wireless neural stimulation microsystem. *IEEE Journal of Solid-State Circuits*, 39(12):2457–2466, December 2004. ISSN 0018-9200. doi: 10.1109/JSSC.2004.837026.

[102] National Instruments. PCIe-6363 Multifunction I/O Device. ni.com, 2018. URL `http://www.ni.com/en-us/support/model.pcie-6363.html`.

[103] U. Bihr, T. Ungru, H. Xu, J. Anders, J. Becker, and M. Ortmanns. A bidirectional neural interface with a HV stimulator and a LV neural amplifier. In *2013 IEEE*

International Symposium on Circuits and Systems (ISCAS2013), pages 401–404, May 2013. doi: 10.1109/ISCAS.2013.6571865.

[104] Maurits Ortmanns and Friedel Gerfers. *Continuous-time sigma-delta A/D conversion: fundamentals, performance limits and robust implementations*. Springer series in advanced microelectronics ; 21. Springer, Berlin ; Heidelberg [u.a.], 2006. ISBN 978-3-540-28406-2.

[105] Gabor C. Temes Richard Schreier. *Understanding Delta-Sigma Data Converters*, chapter 4, page 100. Wiley - IEEE Press, 2004. ISBN 978-0-471-46585-0.

[106] R. T. Baird and T. S. Fiez. Stability analysis of high-order delta-sigma modulation for ADC's. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 41(1):59–62, January 1994. ISSN 1057-7130. doi: 10.1109/82.275660.

[107] Quik-Pak. Air Cavity QFN Packages - Open-molded Plastic Packages. www.icproto.com, 2018. URL `http://www.icproto.com/cap-ic-open-cavity-qfn.html`.

[108] P. Vogelmann, J. Wagner, M. Haas, and M. Ortmanns. A Dynamic Power Reduction Technique for Incremental $\Delta\Sigma$ Modulators. *IEEE Journal of Solid-State Circuits*, pages 1–13, 2019. ISSN 0018-9200. doi: 10.1109/JSSC.2019.2892602.

[109] P. Vogelmann, J. Wagner, A. Hänsler, and M. Ortmanns. Improved SQNR and MSA in Incremental$\Delta\Sigma$Modulators by Using a Recuperation Phase. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65(5):557–561, May 2018. ISSN 1549-7747. doi: 10.1109/TCSII.2018.2821365.

[110] D. Lin, A. Trasser, and H. Schumacher. A fully differential IR-UWB front-end for noncoherent communication and localization. In *2011 IEEE International Conference on Ultra-Wideband (ICUWB)*, pages 116–120, September 2011. doi: 10.1109/ICUWB.2011.6058807.

List of Author Publications

In this work the author has performed theoretical analysis, simulation, implementation and measurements of the circuits presented. This has led to publications at top conferences and journals demonstrating the presented work and is summarized here.

- **M. Haas**, U. Bihr, J. Anders, and M. Ortmanns, "A bidirectional neural interface IC with high voltage compliance and spectral separation," IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, May 2016.

- **M. Haas**, and M. Ortmanns, "A floating high-voltage level-shifter with high area efficiency for biomedical implants," 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Lisbon, Portugal, June 2016.

- **M. Haas**, J. Anders, and M. Ortmanns, "A bidirectional neural interface featuring a tunable recorder and electrode impedance estimation," IEEE Biomedical Circuits and Systems Conference (BioCAS), Shanghai, China, October 2016.

- **M. Haas**, B. Schweizer, J. Anders, and M. Ortmanns, "A miniaturized UWB antenna for implantable data telemetry," 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), JeJu Island, South Korea, July 2017.

- P. Vogelmann, **M. Haas**, and M. Ortmanns, "A 1.1mW 200kS/s incremental $\Delta\Sigma$ ADC with a DR of 91.5 dB using integrator slicing for dynamic power reduction," IEEE International Solid - State Circuits Conference (ISSCC), San Francisco, USA, February 2018.

- **M. Haas**, P. Vogelmann, and M. Ortmanns, "A Neuromodulator Frontend With Reconfigurable Class-B Current and Voltage Controlled Stimulator," IEEE Solid-State Circuits Letters (SSC-L), March 2018.

- **M. Haas**, and M. Ortmanns, "Efficient Implementation and Stability Analysis of a HV-CMOS Current/Voltage Mode Stimulator," IEEE Biomedical Circuits and Systems Conference (BioCAS), Cleveland, USA, October 2018.

- P. Vogelmann, **M. Haas**, and M. Ortmanns, "A Dynamic Power Reduction Technique for Incremental $\Delta\Sigma$ Modulators," IEEE Journal of Solid-State Circuits (JSSC), 2019.

Related publications not included in this thesis:

- M. Pagin, **M. Haas**, J. Becker, and M. Ortmanns, "Delta compression in time-multiplexed multichannel neural recorders," 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Lisbon, Portugal June 2016.

- **M. Haas**, M. Rajabzadeh, and M. Ortmanns, "Performance evaluation of state-of-the-art neural recorder SoCs," Biomedical Engineering / Biomedizinische Technik (BMT), Dresden, Germany, September 2017.

Resume

MICHAEL HAAS

06.02.1988 - Ochsenhausen

EXPERIENCE

University of Ulm, Ulm Germany 2014 - Present
PhD Student/Researcher - Analog Mixed Signal IC Design

- Design and implementation of a fully integrated, bidirectional neural interface, featuring a low noise recording front-end and a biphasic, high voltage current stimulator with outstanding voltage compliance. A single channel prototype of the design has been manufactured (X-FAB 180ñm HV-CMOS) and all results have been published at international conferences.
- Designed and manufactured (X-FAB 180ñm HV-CMOS) a new, semi-digital feedback technique for neural stimulators, which allows reconfiguration between voltage and current mode stimulation, which results in an outstanding area efficiency of the stimulator. In the manufactured design, the stimulator was combined with a low noise neural recorder to form a bidirectional channel and the results where published in JSSC-L, March 2018.
- Designed and manufactured (X-FAB 180ñm HV-CMOS) a 32 channel, bidirectional neural interface SoC, including ADC, digital interface and stimulation/recording process control.

Rohde & Schwarz GmbH & Co. KG, Memmingen, Germany 2013 - 2014
Antenna test range engineer

- Initial operation and planing of a novel, anechoic antenna measurement chamber. Including specification, evaluation and certification of the RF measurement setup and the design of measurement procedures for 3D antenna evaluation.
- Data processing of the acquired raw data for radio direction-finding systems.

EDUCATION

University of Ulm, Ulm, Germany Expected 2019
PhD (Dr.-Ing.) Electrical Engineering

- Thesis: Fully Integrated, Multichannel IC for Brain Machine Interfaces.

University of Ulm, Ulm, Germany September 2013
M.Sc. Electrical Engineering

- Thesis: Design and Layout of a Neural Stimulator Front-End in a 180nm HVCMOS Technology.

University of Ulm, Ulm, Germany September 2011
B.Sc. Electrical Engineering

- Thesis: Aufbau eines Messplatzes zur Charakterisierung magnetoresistiver Sensoren.

Gymnasium Ochsenhausen, Ochsenhausen, Germany June 2007
Allgemeine Hochschulreife

SKILLS

Programing Languages:

- C/C++
- Verilog
- Labview
- Matlab
- Python

IC/PCB design tools:

- Cadence Virtuoso platform
- LTSpice
- Altium PCB Design

Languages:

- German: Native speaker
- English: Fluent
- French: Basic communication skills