A 14b, Twofold Time-Interleaved Incremental ΔΣ ADC using Hardware Sharing

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***Abstract*—High-resolution, single-loop incremental Delta-Sigma (I-ΔΣ) ADCs require large oversampling ratios to sufficiently suppress quantization noise. This limits the bandwidth of most designs to the low-kHz range. To overcome this problem, the presented proof-of-concept design makes use of time interleaving two third-order I-ΔΣ modulators with embedded hardware sharing that helps to enhance the efficiency of the presented modulator. The modulator is fully reconfigurable in a way that both channels can either be operated time-interleaved, independently or averaged. This is a means of enhancing the flexibility and efficiency of the modulator depending on the application scenario. The presented design was fabricated in a 180 nm technology node and operates from a 3 V supply consuming 1.35 mW of power. The achieved bandwidth of 100 kHz together with a DR of 87.2 dB yields a Schreier FoM of 165.9 dB.**

***Index Terms*—Incremental ADC, Incremental ΔΣ, Delta Sigma, Time Interleaving, Hardware Sharing**

I. Introduction

A possible ADC architecture for high resolution yet offering a sample-by-sample correspondence is the incremental Delta-Sigma (I-ΔΣ) ADC. Although this type of ADC has already been introduced in the late 70s [1], by far not as much research has been dedicated to it compared to free-running ΔΣs.

An I-ΔΣ modulator features known properties like its free-running counterpart such as oversampling and noise shaping to a certain extend. To modify a conventional ΔΣ ADC to become incremental, two major architectural changes have to be made. First, all memory elements within the modulator, such as the integrators, have to be reset. Second, a resettable reconstruction filter has to be used alongside. This filter comes with the drawback of an increased quantization- and thermal-noise penalty becoming worse for higher-order modulators [2]. This is one of the main reasons for the decreased power-efficiency of I-ΔΣ ADCs with large oversampling ratio (OSR). Therefore, it becomes conclusive why this kind of ADC lacks behind the performance of state-of-the-art free-running ΔΣ ADCs [3]. However, recent publications try to close this performance gap by introducing new techniques that are not possible in conventional ΔΣ ADCs [4]–[7]. The ADC proposed in [4], for example, uses a coarse SAR ADC upfront to convert the input voltage and uses this information to subtract this coarse part from the analog input signal. Thus only a small residual error remains that is converted by an I-ΔΣ ADC. Adjacently, the coarse and the fine result are combined. This features the advantage that a single-bit quantizer can be used within the I-ΔΣ, still featuring very low dynamics. The

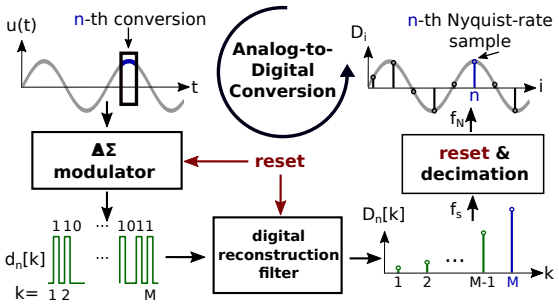

Fig. 1. Simplified block diagram of the operation of an I-ΔΣ ADC. For the sake of clarity, it is assumed that the n-th Nyquist-rate sample is being converted.

design offers a Nyquist-rate of 25 S/s and consumes 6.3 μW thereby achieving an SNR of 119.8 dB which leads to a Schreier FoM of 182.7 dB. The design, as presented in [5], makes use of a linear-exponential conversion technique that greatly reduces the quantization error during the exponential phase at the end of every conversion cycle. A first-order architecture together with a multi-bit quantizer and DWA leads to an SNDR of 100.8 dB at a Nyquist rate of 40 kS/s thereby consuming 550 μW. This gives a Schreier FoM of 176.4 dB. The design from [6] makes use of a multi-step approach. The conversion consists of three steps. First, a first-order I-ΔΣ converts the input signal. As the residual error is bounded after this step, the gain of the feedback can be increased while the input is disabled to keep the modulator stable. In this phase, the residual error is converted. After another 32 cycles, the gain is increased another time.The protoype achieves a sampling rate of 2 kS/s and achieves an SNDR of 96.8 dB at a total power consumption of 34.6 μW. This design achieves a FoM of 174.6 dB. The last architecture to be mentioned is the one presented in [7]. This architecture makes use of unequal weighting in the reconstruction filter and uses this property to successively increase circuit noise towards later cycles in the conversion to dynamically save power and improve the efficiency of the modulator. This design achieves a peak SNDR of 85.1 dB at a sampling rate of 200 kS/s while consuming 1.1 mW of power resulting in a Schreier FoM of 166.2 dB. An advantage of I-ΔΣ ADCs is that they can be used in multiplexed environments due to their true Nyquist-rate behavior. Also the digital reconstruction filter, which is usually not included in the figures-of-merit (FoMs), can now be implemented in a more efficient way [8]. However, the recent state of the art in I-ΔΣ ADCs predominantly confines

itself to the low-speed range [3]. This paper proposes a proof-of-concept time-interleaved (TI) I-$\Delta\Sigma$ ADC making use of hardware sharing with a modulator similar to the ones proposed in [7] and [9]. The remainder of this paper is organized as follows: Section II introduces the operation principles of an I-$\Delta\Sigma$ ADC and explains the concept of time-interleaved I-$\Delta\Sigma$ ADCs including hardware. Section III discusses architectural decisions on system level. Subsequently, Section IV treats the circuit design of the presented prototype IC while Section V presents simulation and measurement results. Finally, Section VI concludes the paper.

II. Theoretical Background

A. Conventional Operation of an I-$\Delta\Sigma$ Modulator

I-$\Delta\Sigma$ ADCs offer true Nyquist-rate properties. To understand the principle of operation, Fig. 1 illustrates the conversion process at hands of a single Nyquist-rate conversion. As it can be seen top left, a continuously running input signal $u(t)$ is fed to the $\Delta\Sigma$ modulator. For the sake of clarity, it is assumed that the n-th Nyquist-rate sample is being converted. The chosen architecture inside the I-$\Delta\Sigma$ modulator block can practically be any $\Delta\Sigma$ modulator with reset switches added to all memory elements, i.e. the integrators.
This modulator is clocked at rate f_s, which is referred to as sampling rate in the following. The modulator operates for M cycles, where M is the OSR. Its output sequence $d_n[k]$ is directly fed to a digital reconstruction filter. The most common types of reconstruction filters are the chain-of-integrators filter (CoI) or the Sinc filter, if line-noise suppression is desired [4]. Moreover, it is also possible to use algorithmic filters such as the optimal filter [10] to enhance signal-reconstruction quality. However, the latter come with the drawback of increased implementation complexity and often lack robustness against thermal noise. Therefore, this paper solely focuses on CoI filters as they yield good signal reconstruction with little increase in noise together with a simple and efficient implementation. As presented in [11], the maximum error ϵ due to quantization noise at the end of a Nyquist-rate conversion, assuming a stable higher-order loopfilter together with a CoI filter of the same order, is bounded by

$$\epsilon \leq c \cdot V_{ref} \cdot \frac{1}{\sum_{k=1}^{M} w_L[k]}, \tag{1}$$

where c is a constant determined by the loopfilter coefficients. V_{ref} is the reference voltage of the modulator and $w_L[k]$ are the filter weights of an L-th order CoI filter at time instant k. In [7] it was shown that the weights for an L-th order CoI filter can be calculated as

$$w_L[k] = \frac{1}{(L-1)!} \prod_{i=0}^{L-2} (M-k+i+1) \quad , 1 \leq k \leq M. \tag{2}$$

The sum of (2) as needed for (1) can easily be calculated with help of the following relation

$$\sum_{k=1}^{M} w_L[k] = w_{L+1}[1]. \tag{3}$$

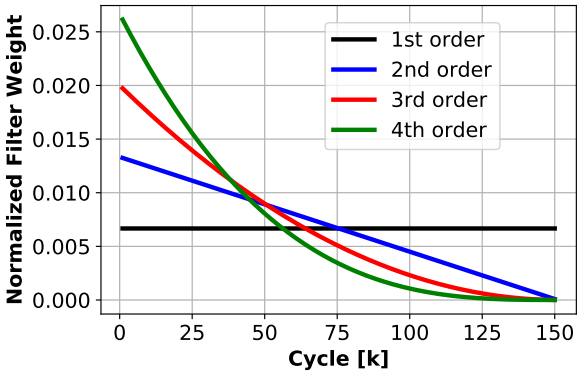

Fig. 2. Weighting of the individual samples for an exemplary M=150 for CoI filters of first to fourth order.

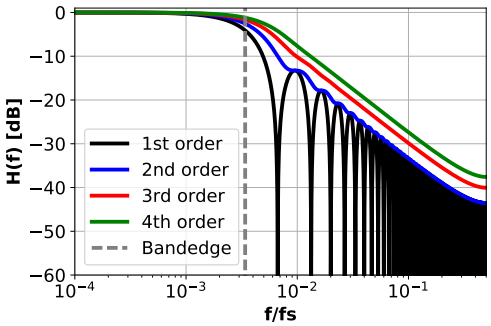

Fig. 3. Transfer function for CoI filters of first to fourth order before decimation for an exemplary M=150.

This already gives an indication that the signal reconstruction using CoI filters can be very precise assuming a higher order ADC at a reasonably large OSR. The normalized filter coefficients can be seen in Fig. 2. For the sake of clarity, they have been normalized such that the sum of all coefficients is one. To understand how these filters affect the STF and the noise performance of the ADC, it is of interest to have a look at the transfer function H(f) for different filter orders. This transfer function can be derived from the filter weights. As shown in [12], the front-end sample-and-hold (S/H) element can be omitted to save power. However, this leads to a modification of the signal transfer function (STF) of the whole ADC which is no longer flat. In this case, the work of [13] shows that the STF of a single-loop ADC can be assumed to be equal to the transfer function of the reconstruction filter. This especially holds true for large OSRs, 150 in this example. The transfer functions for CoI filters of first to fourth order can be seen in Fig. 3. This transfer function is valid only for the non-decimated output sequence of the digital filter, yet including the reset. The decimation operation will result in a foldover of all sidebands to the baseband. As it can easily be observed, higher-order filters have a less sharp roll-off after the bandedge. Thus it is obvious that they suffer from an increased noise foldover and consequently have a higher noise penalty factor [2], [7].

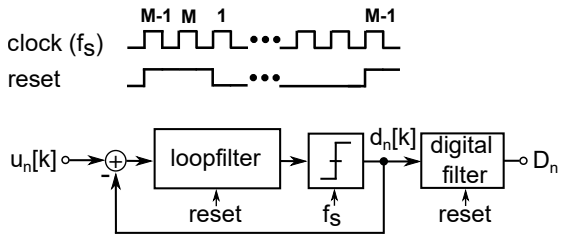

Fig. 4. Block diagram of an I-$\Delta\Sigma$ ADC including timing diagram for an OSR of M.

As shown top right in Fig. 1, the digital output of the reconstruction filter D_i is a decimated version of the output of the reconstruction filter. The decimated output of the reconstruction filter is clocked at a rate of $f_\mathrm{N} = f_s/M$ if the reset is assumed to happen in an instant. This rate leads to the effective bandwidth $f_{bw} = f_\mathrm{N}/2$. This yields a one-by-one correspondence between input signal and digital output D_i.
A block diagram including the respective clocking of an exemplary modulator can be seen in Fig. 4. The clock cycles are enumerated from 1 to M for each period. After the reset, the next conversion starts and the clock counter is reset to 1. During the M-th clock cycle of the n-th Nyquist-rate conversion, the output of the reconstruction filter D_n is stored and the loopfilter as well as the digital reconstruction filter are entirely reset. Without the loss of generality it is assumed that two clock cycles are used for the reset to give enough time to fully discharge the capacitors.

B. Extension to Time-Interleaved Operation

Different schemes for TI free-running $\Delta\Sigma$ ADCs have been presented, which try to counteract the memory behavior of $\Delta\Sigma$s, which would prevent a TI implementation; e.g. the block digital filtering method from [14], whose drawback is that it becomes impractical for a larger TI factors due to the domino effect. The work from [15] introduced a four-path TI scheme counteracting this effect. This is achieved by using prediction paths that require additional multi-bit quantizers. A prototype IC [16] requires individual level averaging (ILA) to suppress the nonlinearity arising from the need for the multi-bit architecture.
On the contrary, the aforementioned techniques are not required for TI I-$\Delta\Sigma$ ADCs as it comes with an inherent sample-by-sample correspondence; thus it should be possible to time interleave multiple ADCs to increase the effective Nyquist rate. In theory it is possible, to increase the effective Nyquist rate by an arbitrarily large factor that is equal to the number of ADCs that are used for time interleaving without any of the problems arising from using free-running $\Delta\Sigma$ modulators. Assuming two discrete-time (DT), TI I-$\Delta\Sigma$ modulators, the block diagram with respective clocking scheme may look like the one in Fig. 5. Again, the clock cycles are labeled from 1 to M. Both ADCs are driven by the same clock at rate f_s to minimize clock circuitry and reduce the risk of timing errors. The reset of the first and the second modulator have to be shifted by $M/2$ such that the digital outputs do not show any timing error with respect to the ideal sampling instants of the

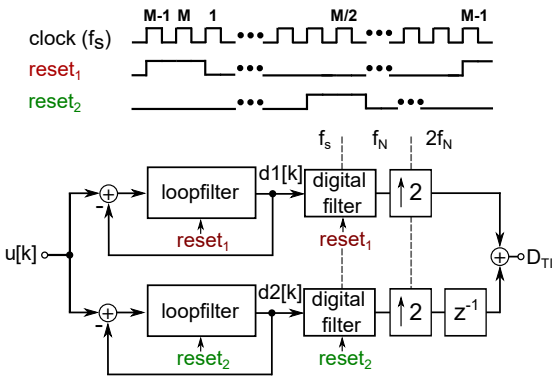

Fig. 5. Block diagram of a TI I-$\Delta\Sigma$ ADC including the respective clock scheme.

TABLE I
SIGNAL ATTENUATION OF THE COI FILTER AT DIFFERENT FREQUENCIES.

f_{sig} \ Order	1	2	3	4
fs/2M	-3.9 dB	-2.5 dB	-1.6 dB	-1.1 dB
fs/M	-∞	-10 dB	-6.1 dB	-4.2 dB

TI output sequence D_{TI}. Thus it is preferable to choose M to be an even number. However, this is no real infringement for most of the designs. In this example, two clock cycles are assumed for the reset to make sure, the integrators are properly reset. Nevertheless, this doesn't play a noticeable role as the last cycles of the conversion do barely contribute to the digital output for higher order ADCs with a reasonably large OSR. Both modulators are connected to the same input signal $u[k]$. The digital output of the reconstruction filters are both running at Nyquist rate f_N. To combine the TI outputs, both outputs have to be sampled up by a factor of two - now running at $2f_\mathrm{N}$. The lower channel is delayed by one clock cycle of $2f_\mathrm{N}$. Next, both outputs are added yielding a TI digital output word D_{TI} running at twice the rate of the individual ADCs.
However, referring again to Fig. 3 imposes requirements on the modulator and reconstruction filter order as it is highly desired to have as less attenuation as possible for signals in the first and second Nyquist zone of the individual I-$\Delta\Sigma$ modulators. It is for example not possible to use two first-order modulators for the time interleaved operation as signals that are close to the twofold bandwidth of the individual modulators are entirely suppressed. A correction filter that is flattening the inband response would result in a raised noise floor. Tab.I summarizes the attenuation at the bandedge of the modulator and at twice the bandedge for a twofold TI operation. The low attenuation at the twofold bandedge makes higher order architectures more appealing. Another option is to use a sample-and-hold (S/H) amplifier in front of every individual modulator. However, this would lead to a significantly increased power consumption.

C. Hardware-Sharing TI ADC

As presented in [7] and [9], the property of the unequal weighting of the reconstruction filter, as shown in Fig. 2, can be used to dynamically save power within the ADC. In

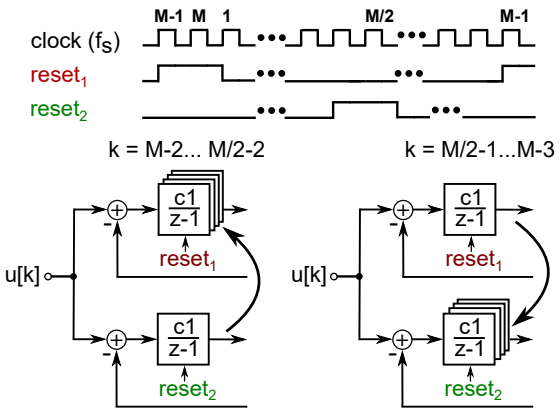

Fig. 6. Hardware-sharing timing for the presented I-ΔΣ ADCs.

the presented works, slices of the first integrator have been disabled during runtime to save power. On the other side, the input-referred noise is increased by this technique, since later samples (with higher circuit noise) contribute less to the Nyquist sample compared to early samples (with sufficiently low circuit noise). Thus, the saved power is beneficial over the slight increase in noise regarding the ADC's efficiency.

The proposed approach to make use of this technique for TI I-ΔΣ is shown in Fig. 6. The underlying idea is explained in the following. As the reset between the modulators is shifted by $M/2$ cycles, the weighting of the interleaved cycles is shifted by the same number of cycles. This means during the time, when the first modulator operates on the first $M/2$ samples, all available slices are used by this modulator because these samples are the ones with the highest weight in the reconstruction filter. During this time, the second modulator processes the last half of its M samples. With respect to Fig. 2, these samples are barely weighted in the CoI filter assuming an order of three or higher. As soon as the second modulator starts with a new conversion and the highly weighted first M/2 samples of it, all available slices are switched over.

In the following it is assumed that a total of 5 slices is used of which 1 is permanently assigned to each modulator. This leaves 3 slices that can be dynamically switched between one or the other side in ping-pong fashion. The maximum power consumed by the first integrator of each side using all available slices is

$$P_{\max} = 4 \cdot P_{Slice} \tag{4}$$

where P_{Slice} is the power consumed by every individual slice. If it is further assumed that the first integrator is permanently using 4 slices for its operation, the contributed noise power is

$$P_{N,ref} = \frac{\sigma_{n,rms}^2}{c_{norm}} \sum_{i=1}^{M} w_L[k]^2 = \sigma_{n,rms}^2, \tag{5}$$

where c_{norm} is a constant normalization factor that is the sum over all filter weights $w_L[k]^2$. $\sigma_{n,rms}$ is the rms noise voltage of the I-ΔΣ modulator with 4 active slices in the first integrator. In this example it is assumed that the first integrator is entirely dominating the noise performance of the ADC. By reducing the number of slices to one after $M/2$ cycles leads to the following increase in noise power $P_{N,*}$

$$P_{N,*} = \frac{\sigma_{n,rms}^2}{c_{norm}} \left(\sum_{k=1}^{M/2} w_L[k]^2 + \sum_{k=M/2+1}^{M} 4 \cdot w_L[k]^2 \right). \tag{6}$$

So the noise is less than linear increased by a factor F_N of

$$F_N = \frac{P_{N,*}}{P_{N,ref}} = \frac{\sum_{k=1}^{M/2} w_L[k]^2 + \sum_{k=M/2+1}^{M} 4 \cdot w_L[k]^2}{\sum_{i=1}^{M} w_L[k]^2}. \tag{7}$$

Assuming an exemplary OSR of 150 for a third-order modulator, the effective input-referred noise will be increased by less than 10% by this technique in case of a third-order CoI whereas the saved power in the dominating first integrator per ADC can be calculated as follows:

$$\mathrm{P}_* = 1 - \left(0.5 \cdot \frac{4\mathrm{P}_{\mathrm{Slice}}}{4\mathrm{P}_{\mathrm{Slice}}} + 0.5 \cdot \frac{1\mathrm{P}_{\mathrm{Slice}}}{4\mathrm{P}_{\mathrm{Slice}}} \right) = 0.375. \tag{8}$$

It can be seen that making use of this technique is resulting in a power reduction of 37.5% while only slightly increasing the input-referred noise. Effectively, the Schreier FoM of a TI ADC using hardware sharing in ping-pong fashion should ideally improve by

$$\Delta\mathrm{FoM_S} \approx \underbrace{-0.4\,dB}_{+10\%\ \mathrm{Noise}} \underbrace{+3\,dB}_{2\cdot BW} \underbrace{-1\,dB}_{1.25\cdot Power} \approx +1.6\,dB \tag{9}$$

compared to a non-TI, non-sliced I-ΔΣ modulator. Using a fourth-order filter instead would yield $\Delta\mathrm{FoM_S} \approx 1.9$ dB. But as the noise penalty that comes with the third-order filter is roughly 1 dB lower than that of a fourth-order filter, it makes sense to choose a third-order CoI reconstruction filter to achieve the best possible noise performance. So far, the TI mode of operation and hardware sharing have been introduced. The following subsection will now present three different operation modes that are possible with an I-ΔΣ ADC as shown in Fig. 5. Each mode allows for using hardware sharing.

D. Operation Modes

Slight modifications on the architecture shown in Fig. 5 potentially allow for different application scenarios the ADC can be reconfigured for. As already discussed, the ADC can be used time interleaved to be able to convert fast signals up to twice the bandwidth of every individual ADC.

Often it is desirable to mutliplex between multiple channels as in biomedical applications like neural recorders [17]. In such a scenario there is no benefit in using the ADC in a TI mode. Thus, a multiplexer must be added upfront like shown in Fig. 7. To separate the digital sequences after conversion, a demultiplexer must be used. Still it is possible to use the hardware sharing in ping-pong fashion as the reset signals can be used as in the TI mode. Such, the efficiency of such two multiplexed ADCs is increased as compared to two ADCs that are operated separately.

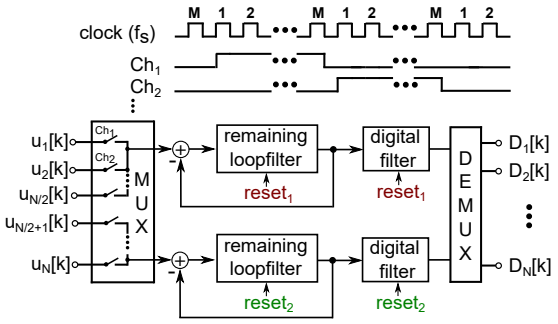

Fig. 7. Block diagram of the I-$\Delta\Sigma$ ADCs configured such that multiplexed operation is possible.

III. System-Level Implementation of the ADC

This section gives an overview of the decisions on system level that have been made to satisfy all requirements for the TI ADC using hardware sharing resulting in a manufactured prototype IC.

A. Calibration for Time-Interleaved ADCs

So far, the principle of time interleaving for I-$\Delta\Sigma$ ADCs has been introduced. In the following, possible shortcomings are highlighted. Therefore, Fig. 5 shall again be observed. For time-interleaved operation, the digital outputs of both sides are upsampled, delayed and added. Ideally, there is no mismatch between both channels. In this case, one does not expect any degradation in resolution by combining both outputs. However, in reality both modulators are analog circuits that are subject to component mismatch. Consequently, any mismatch between both channels may lead to a degradation of the resulting digital output.

According to [18] and [19], the main contributors to a degraded SNDR is channel mismatch with respect to gain and offset. Different offsets in both ADC channels may cause a periodic pattern in the output spectrum as they are modulated with a frequency of $2f_N$, thus fold back at f_N. As the mismatch in offset can be quite large, the offset has to be removed to avoid any degradation in SQNR. This can either be done on circuit level or can be removed in the digital domain before adding both channels.

The same modulation occurs due to gain mismatches between both channels. Here, amplitude modulation of both input signals (differently scaled by $\Delta\Sigma$ coefficients) at $2f_N$ can be seen. This leads to tones centered at $f_N \pm f_{sig}$. For high-resolution TI ADCs, this must be calibrated. A one-time foreground calibration, however, is sufficient. Furthermore, a timing error Δt between both channels may lead to a severe degradation in performance. As this is the most difficult part to calibrate, it shall be investigated in more detail.

To be able to analyze Fig. 5, it is replaced by an adequate mathematical model as shown in Fig. 8. Here, the delay is put upfront and modeled as a delay of the input signal in Fourier domain as $exp(j2\pi f(T + \Delta t))$. The static but undesired timing error due to mismatch is Δt. The desired time shift $T = 1/(2f_N)$. The grayed-out filter H[z] is assumed to be unity for the moment. With the help of this model , the output

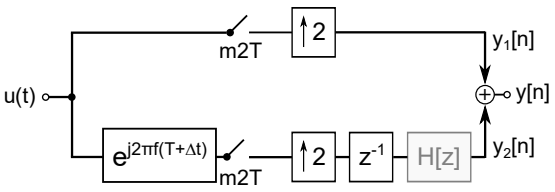

Fig. 8. Mathematical model of the TI I-$\Delta\Sigma$ ADCs including timing error Δt.

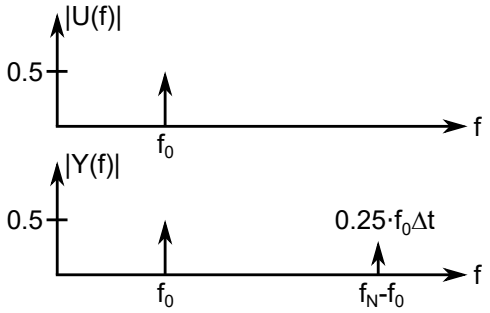

Fig. 9. Fourier transform of the input signal u(t) and the time-interleaved output including fold-over component due to timing errors, respectively.

y[n] can now be calculated. In the following it is assumed, without the loss of generality, that $u(t) = cos(2\pi f_0 t + \theta)$. The derivation is lengthy and can be reviewed in detail in [18]. However, the outcome of the derivation and its influence on the TI I-$\Delta\Sigma$ are of interest. The output of the TI I-$\Delta\Sigma$ in presence of timing error is obtained as

$$\begin{aligned} y[n] = &\cos\left[\pi f_o \Delta t\right] \cos\left[2\pi(f_o nT + \frac{f_o}{2}\Delta t) + \theta\right] \\ &+ \sin\left[\pi f_o \Delta t\right] \sin\left[\pi\left(2\left(f_o - f_N\right)nT + f_o \Delta t\right) + \theta\right]. \end{aligned} \tag{10}$$

Assuming a small sampling time error Δt, the equation can be approximated with:

$$\begin{aligned} y[n] \approx &\cos\left[2\pi f_o nT + 2\pi f_o \frac{\Delta t}{2} + \theta\right] \\ &\underbrace{-\pi f_o \Delta t \sin\left[\pi\left(2\left(f_N - f_o\right)nT + f_o \Delta t\right) + \theta\right]}_{\text{image}}. \end{aligned} \tag{11}$$

The frequency-domain spectrum of x[n] and y[n] are illustrated in Fig. 9, respectively. It can clearly be seen that an image of the input signal appears at $f_N - f_0$ due to the timing mismatch Δt . To correct for this error, a compensation filter H[z] as shown in gray in Fig. 8 can be used. As presented in [18], this filter can be derived as:

$$H(z) \xrightarrow{z=e^{j2\pi f}} H(f) = e^{-j2\pi f \Delta t} e^{j\frac{\pi \Delta t}{T}\operatorname{sign}(f)}, |f| \leq f_N \tag{12}$$

As the presented ADC is highly oversampled, it can be assumed that $\Delta t < 1/(M \cdot f_N)$ thus $\Delta t \ll f_N$. This leads to:

$$H(f) \approx 1 \tag{13}$$

Equation (13) already suggests that for large oversampling ratios it may be possible to omit the calibration filter H(z) that compensates for timing errors without loss of performance.

TABLE II
THERMAL NOISE PENALTY FACTOR AS A FUNCTION OF COI ORDER L AND OSR M TAKEN FROM [7]

L \ M	25	50	75	100	150	200
1	1.0	1.0	1.0	1.0	1.0	1.0
2	1.3	1.3	1.3	1.3	1.3	1.3
3	1.7	1.8	1.8	1.8	1.8	1.8
4	2.2	2.2	2.2	2.3	2.3	2.3

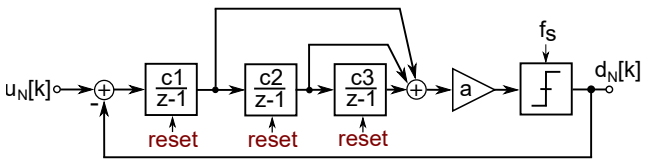

Fig. 10. Architecture of the implemented third-order CIFF architecture. The CoI filter is not shown here.

TABLE III
SCALING COEFFICIENTS OF THE ANALOG LOOPFILTER AS SHOWN IN FIG. 10.

c1	c2	c3	a
0.2403	0.3956	0.1067	0.3333

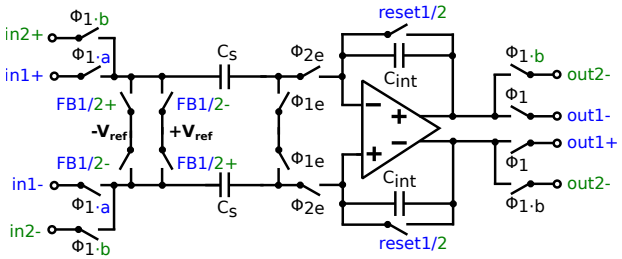

Fig. 11. Block diagram of a slice of the first integrator. All switches except for the reset switch are realized as bootstrapped switches.

B. Modulator Architecture

The target of this work is to design a discrete-time, high-resolution I-$\Delta\Sigma$ ADC with a TI bandwidth of 100 kHz. This shall be achieved through time-interleaving two I-$\Delta\Sigma$ ADCs. In the following the choice of architectures for the modulator as well as the reconstruction filter are discussed.

With regard to Fig. 3 and the fact that time interleaving by a factor of two is targeted, it seems practical to choose a modulator order that is as high as possible such that the attenuation at $2f_{BW}$ is as low as possible (c.f. Tab.I). However, in [2] a thermal noise penalty factor has been introduced that accounts for the reduced suppression of thermal noise due to the flattened response for higher-order modulators as compared to a first-order modulator. Tab. II shows the noise penalty factors as a function of order and OSR. Taking into account the signal attenuation at the band edge as shown in Tab.I, first and second order designs are not viable as the attenuation at high frequencies is too large. Another argument that supports this decision is the demand for high resolution at fast conversion speed. Lower-order designs require multi-bit quantization, to keep the OSR reasonably low. This causes non-linear distortion which in turn requires linearization techniques that are more efficient at larger OSRs [20] or require complicated compensation schemes to work properly in the incremental mode [21]. To achieve high resolution for single-bit, low-order modulators large OSRs are required. This is counteracting the fast conversion speed target. As a reasonable accuracy can be achieved with a single-bit third-order modulator, this is preferred as it offers a good tradeoff between aggressiveness of noise shaping and decrease in maximum stable amplitude [7].

As high resolution together with a power-efficient implementation is targeted, a feedforward architecture, as shown in Fig. 10, is chosen. The feedforward paths reduce the signal power that is processed by the integrators and therefore greatly relax their requirements. The web tool from www.Sigma-Delta.de [22] has been used to optimize the coefficients for the I-$\Delta\Sigma$ modulator. The obtained coefficients are shown in Tab. III. An OSR of 150 is required to achieve an SQNR ≈ 100 dB. For the sake of simplicity and good reconstruction quality, a third-order CoI filter has been chosen as reconstruction filter. It was stated in [11] and [23] that the filter can be chosen an order higher as the modulator. This will cause an increase of quantization error but flattens the transfer function close to the band edge and thus reduces signal attenuation. Furthermore, the weights towards later cycles are reduced what decreases the noise contribution of the used hardware-sharing technique. In general it would be possible to choose a fourth-order CoI filter, but this would come at the cost of an increased quantization noise floor and a larger noise penalty factor shown in Tab. II. The effect of reduced noise contribution by using smaller weights during the last M/2 cycles would be entirely dominated by the increased noise contribution.

IV. CIRCUIT-LEVEL IMPLEMENTATION

The most important part of the discrete-time modulator is the switched-capacitor (SC) integrator located at the input of the modulator as its performance dominates the accuracy and power consumption of the whole ADC. Any error caused here will not see any noise shaping. Consequently, it is very important to make sure that this part does closely match the system requirements in terms of linearity and noise. The block diagram of a single implemented slice of the first integrator can be seen in Fig. 11. The size of the sampling capacitor C_s is chosen such that the sum of C_s of all slices gives a total of 300 fF to meet the thermal noise requirements at this node. In this design, a total SNDR of 90 dB was targeted. The control signals a and b control the switches that assign the integrator to the first or the second channel. The switching from one channel to the other channel happens during the reset phase, when the OTA is reset to common mode. The sampling switches on the input side of the OTA are a possible source of harmonic distortion. To reduce the signal-dependent charge injection, which is one of the causes of harmonic distortion, bottom-plate sampling is used. Furthermore, the signal-dependent variation of the on resistance of the sampling switches could lead to imperfect settling of the sampling capacitor C_s with respect to the input voltage of the respective channel. To reduce this

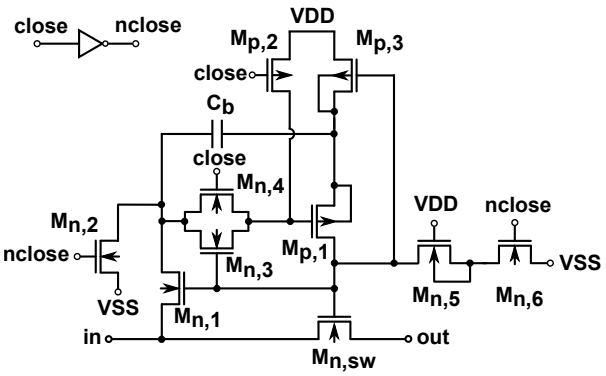

Fig. 12. Schematic of the bootstrapped switch that is used in the sampling network of the integrator.

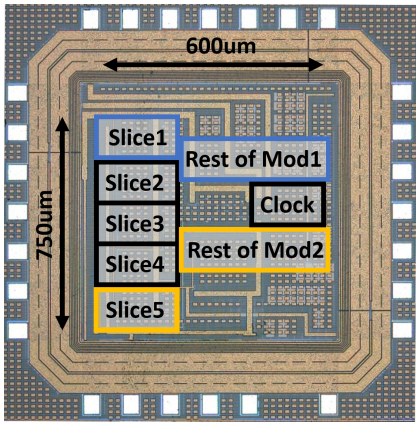

Fig. 13. Chip photograph of the prototype IC.

variation to an acceptable level, bootstrapping, as presented in [24], has been used for the sampling switches at the input as well as for the feedback switches. This technique also helps to mitigate charge injection that strongly depends on the channel area of the switch. With bootstrapping the size of the pass device can be reduced to a minimum while the on resistance remains low due to the large gate-source voltage, which again reduces the amount of charge injected to both sides while turning the switch off. This guarantees a very good linearity. The schematic of the implemented switches can be seen in Fig. 12. However, as it can be seen from the schematic, the implementation of this switch is more costly than simply using a transmission gate and comes with an increased area penalty. This is mainly due to the battery capacitor C_b that is in the range of 100 fF and the switch $M_{p,3}$ that must be put in a separate well as its bulk is connected to its source to prevent the transistor from damage due to voltage stress.

The OTA of the first integrator has to provide enough DC gain, bandwidth as well as slew-rate to make sure that the amplifier can settle to the required accuracy at the end of every integration phase. However, as it can be concluded from [25], these properties can be traded in partly for each other. A folded cascode with slew-rate enhancement as presented in [7] has been used for every slice of the first integrator stage. Additionally, transistor sizes have been adjusted to reduce the 1/f-noise contribution. The sliced OTA achieves a dc gain of 70 dB. The simulated GBW is 200 MHz with a phase margin of above 70°. As I-$\Delta\Sigma$ modulators provide noise shaping to a certain degree [22], later stages are relaxed in terms of required accuracy. Especially the feed-forward topology relaxes the requirements of the second and third stage to a minimum. Thus, only transmission gates are used as sampling switches and the OTAs of the second and third stage are realized as simple telescopic amplifiers as swing is low and the load capacitors are fairly small. The addition of the individual signals is passively performed by an SC network. The size of the used capacitors is negligibly small to reduce the loading of the preceding OTAs. The quantization is done by means of a simple strong-arm latch.

V. Simulation and Measurement Results

A. Measurement Setup

A high-precision, audio-band signal generator has been used to generate a differential signal. To further limit the noise contributed by the generator, a passive RLC filter has been used. The on-board resistors, capacitors and inductors have been selected carefully to avoid distortion. In order to avoid channel mismatch, 0.01% matching resistors have been selected for this. Readout and filtering of the data are performed by an FPGA. After every conversion, this data is accessed by Matlab, where the spectral analysis is performed.

B. Measurement Results

A chip photograph of the implemented design can be seen in Fig. 13. The presented IC was fabricated in a 180 nm CMOS technology and occupies an active area of approximately 0.45 mm^2. The five integrator slices located at the input of the ADC consume a major part of the area. This is mainly due to the large bootstrapped switches. The rest of both modulators are placed close to their fixed slice. A bias network distributes the reference current across the chip. A clocking network is necessary to create the non-overlapping clocks required for bottom-plate sampling. This clocking network contains clock drivers to make sure that parasitic capacitance doesn't lead to an overlap of clock phases.

The first measurement is performed to make sure that the hardware-sharing approach is working as expected. To improve visibility of differences, all measured curves have been averaged across 100 measurements. The differential input of the ADC is tied to the internal common mode to avoid disturbers and noise possibly introduced by the signal generator. The results are shown in Fig. 14. It is worth mentioning that both channels are indistinguishable in terms of noise performance. So it is enough to show the spectra of only one of the ADCs here. The green curve shows the measurement of a single channel without hardware sharing. This means that only a single slice is assigned to this channel. The blue curve shows the measurement results for using four slices not permanently but in the described hardware-sharing mode.

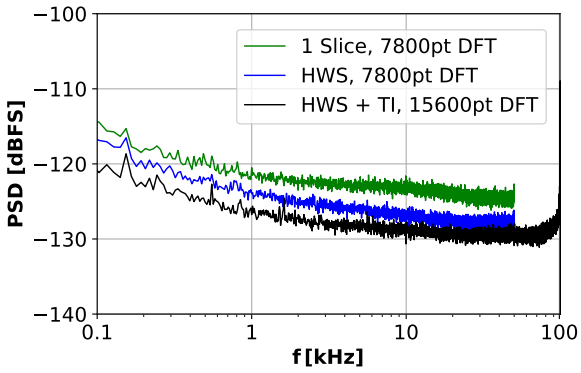

Fig. 14. Noise performance of one ADC using only one slice and four slices with hardware sharing, respectively, as shown in green and blue. The measured performance of the ADC using HWS and TI is shown in black.

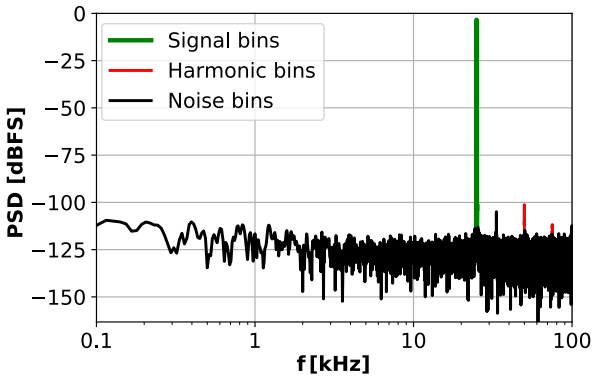

Fig. 15. Exemplary measured 15600-point DFT of the ADC in TI mode with enabled hardware sharing and in-advance calibration for gain for an input signal of -3.5 dBFS at a frequency of 25 kHz.

Last, the black curve shows the measured noise floor in the presented TI mode including hardware sharing. The black curve lies approximately 5.6 dB below the green curve and 3 dB below the blue curve. This can be explained as follows. If only a single channel was upsampled by a factor of two, the power spectral density would drop by 6 dB as the mean noise power is halved while the respective bandwidth is doubled. Now two channels add their uncorrelated noise, thus the mean noise power increases by 3 dB. Consequently, leaving aside the hardware sharing, the black curve should ideally be 6 dB below the green curve and 3 dB below the blue curve. However, as the hardware sharing introduces a slight noise penalty together with the power benefit, the difference between the black and the blue curve to the green curve is slightly diminished. It can be seen that 1/f noise is modulated up to 100 kHz as described previously. An exemplary spectrum for the TI mode including an input signal is shown in Fig. 15. An input signal of -3.5 dBFS at 25 kHz has been applied to the ADC. Due to mismatch in offset and gain between both channels, a simple calibration was performed in advance. A one-time calibration for the gain is sufficient to reduce the foldover components such that they don't contribute anymore. Before adding the signals, their mean is subtracted. The costly calibration for timing errors in the clock is not needed as the oversampling ratio is much larger than the Nyquist rate and thus the assumption that the timing error is low enough that no calibration is needed holds true here. Also both modulators run from the same clock which helps to further reduce this mismatch.

It is clearly visible that the measurement shows nonlinear behavior which leads to a second and third harmonic. However, the measured SFDR is 101.5 dB and the total harmonic distortion (THD) is as low as -95.6 dB. The measured peak SNR and SNDR are 85.2 dB and 85.1 dB, respectively. The total noise is dominated by thermal noise. However, the 1/f part of the noise could be reduced by making use of auto-zeroing in the first integrator. For the sake of a rapid tapeout, this feature has not been added to the presented prototype. It can be seen that there is a spur that is not related to the signal. The origin could not be fully clarified but is related to

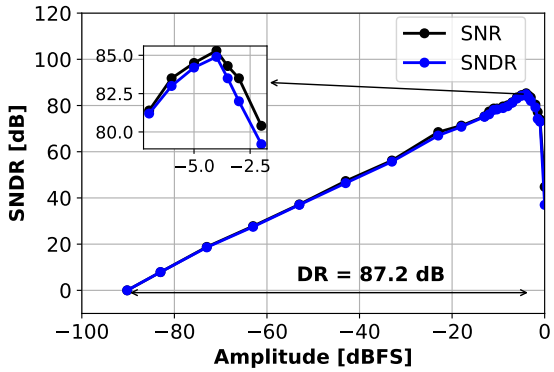

Fig. 16. MSA of the TI I-$\Delta\Sigma$ ADC for an input signal of 1 kHz.

the digital pad-driver as lowering its supply voltage reduces the spur and lowers circuit noise as well. Unfortunately, this voltage can not be lowered arbitrarily as digital data is lost at a certain point resulting in a strong loss of performance. This in conjunction with the noise contribution of the signal generator and the PCB lead to approximately 3 dB drop in SNDR as compared to simulation results. A separate measurement has been performed to determine the maximum stable amplitude (MSA) as well as the dynamic range (DR) of the TI ADC. The result is shown in Fig. 16. The MSA is located at -3.5 dBFS. For the MSA, the ADC is achieving an SNR and SNDR of 85.2 and 85.1 dB, respectively. At an input amplitude of -90.2 dBFS, the SNR/SNDR reaches 0 dB leading to a dynamic range of 87.2 dB. In total, the IC draws 449 μA from a 3 V supply. The power breakdown of the ADC that has been extracted from simulation results is depicted in Fig. 17. As the digital logic cells as well as the circuit for clock generation are driven from the 3 V supply, their share of the total power consumption is quite large. It is expected that going for smaller technology nodes in conjunction with lower supply voltages would lead to great savings in the digital part therefore making the presented design more efficient.

The table shown in Tab. IV summarizes this work and compares it to similar designs taken from the state of the art.

TABLE IV
COMPARISON TO THE STATE OF THE ART OF I-$\Delta\Sigma$ ADCS

	Katayama [26] SSCL 2018	Wang [5] JSSC 2019	Zhang [6] VLSI 2016	Vogelmann [9] JSSC 18	Mokhtar [27] SSCL 2019	**This work**
Technology [nm]	180	65	180	180	180	**180**
Area [mm^2]	0.72	0.134	0.5	0.363	0.175	**0.45**
Supply [V]	3	1.2	1.5	3	3	**3**
Power [μW]	27700	550	34.6	1098	1270	**1347**
$f_{s,nyq}$ [kS/s]	1250	40	2	200	200	**200**
SNDR [dB]	96.6	100.8	96.8	86.6	83.0	**85.1**
SFDR [dB]	110	120.3	-	101.3	94.3	**101.5**
FOM_s [dB]	173.6	176.4	174.6	166.2	161.9	**163.8/165.9***

(*FOM_s based on the SNDR and the DR, respectively.)

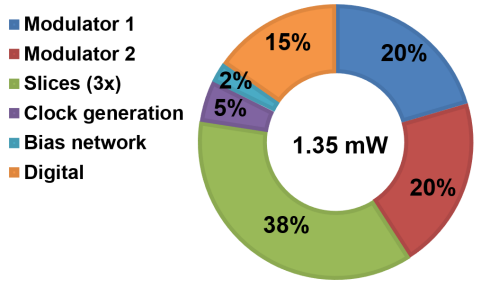

Fig. 17. Power breakdown of the individual components of the TI I-$\Delta\Sigma$ ADC.

VI. CONCLUSION

To the best of the author's knowledge, this paper reports the first fabricated TI I-$\Delta\Sigma$ ADC. For increased efficiency, this proof-of-concept ADC makes use of a hardware-sharing technique. Furthermore, the ADC is fully re-configurable and is especially suitable for variable scenarios ranging from high resolution over high-channel count to fast conversion speed. A two-channel prototype IC was manufactured in 180 nm CMOS achieving a bandwidth of 100 kHz. The ADC is capable of achieving a peak SNDR of 85.1 dB and a DR of 87.2 dB. Including the presented hardware-sharing technique, this ADC consumes approximately 1347μW resulting in a FoM based on SNDR and DR of 163.8 dB and 165.9 dB, respectively.

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