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PLL Based Fully-Integrated LO Generation for Wideband RF Front-Ends

DISSERTATION

zur Erlangung des akademischen Grades eines

DOKTOR-INGENIEURS (DR.-ING.)

der Fakultät für Ingenieurwissenschaften
und Informatik der Universität Ulm

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Ulm, 19.04.2018

Abstract

This dissertation describes Phase Locked Loop (PLL) based Local Oscillator (LO) designs for RF front-end modules targeting wideband wireless communications systems from microwave to millimeter-wave ranges. With the increase of the operating frequencies in wireless transceivers, it becomes more challenging to deliver fully integrated LO signals with high performance. In conventional single loop PLLs, the comparison frequency is restricted by the speed and noise of the phase frequency detector, which increases the in-band phase noise and the phase lock time. In this thesis, a novel dual loop PLL topology with a higher comparison frequency and a wider loop bandwidth is investigated: a frequency acquisition loop speeds up the lock time; a phase locked hold loop improves the phase noise and spurious levels. The trade-offs between the loop bandwidth, phase noise and lock time are much more relaxed than in conventional PLLs. The LO generator is fully integrated in a 0.25μm SiGe BiCMOS technology. The designs benefit from the high speed, low noise HBTs and the small sized, low power consumption CMOS transistors. The key sub circuit block designs and optimization are in detail discussed, which include phase/frequency detectors, frequency dividers and prescalers, voltage controlled oscillators, loop filter designs and so on. The loop behavior, frequency response and transient performance are studied at a system level. Three demonstrators are presented: a 35 GHz ultra-low phase noise PLL for Ka-Band radar communications which achieves state-of-the-art phase noise performance; a wideband frequency synthesizer for multi-band satellite communications with a frequency range from 16 to 24 GHz; a 3 to 5 GHz reconfigurable receiver integrated with an agile frequency synthesizer for small cell base station applications.

Acknowledgements

First of all, I would like to express my deepest gratitude and appreciation to my supervisor, Prof. Dr.-Ing. Hermann Schumacher, for giving me this great opportunity to work in his group, providing me guidance, support and encouragement through the research work and in all other aspects during the time that I studied and worked in Ulm.

Secondly, I would like to thank the colleagues who I worked with in the Institute of Electron Devices and Circuits: Andreas Trasser, Bernd Schleicher, Giuseppe Oliveri, Gang Liu, Dayang Lin, Ferdinand Sigloch, Tatyana Purtova, Peter Lohmiller, Sébastien Chartier, Ursula Winter, Václav Vanlenta and Ursula Spitzberg who were always supportive and friendly.

I would also like to thank the industry partners: Atmel, IHP, EADS (now Airbus Group) and EU research commission for their technology and financial support. Additionally, I would like to give my thanks to the colleagues who worked for the Flexwin Project for great collaboration: Prof. Wolfgang Menzel, Volker Ziegler, Mehmet Kaynak, Mohamed Elkhouly, Ulf Holmberg, Giandomenico Amendola and Luigi Boccia.

Last but not least, I would like to thank my parents and family who are always there for me.

To my father

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Introduction

1.1 Motivation

A Local Oscillator (LO) is one of the most essential blocks in the RF transceiver frond-end in wireless communication systems. Through a frequency mixer, the LO signal up- or down-converts signals of interest to targeted frequencies. The quality of the LO signal plays an important role in determining the performance of an RF transmitter/receiver [1].

An off-the-shelf crystal oscillator is ideal as an LO with fixed frequency below the hundred-MHz range due to its superior signal purity and low cost; a Surface Acoustic Wave (SAW) based oscillator operates up to GHz frequencies with excellent phase noise performance. It is challenging for a single quartz crystal oscillator to operate beyond the GHz range. The frequency range can be expanded by adding frequency multipliers after an oscillator, mixing of different oscillators or using Phase Locked Loops (PLLs). One of the drawbacks of the direct frequency multiplication is that it also multiplies the phase noise over the complete spectrum. The mixing of different oscillators has drawbacks in terms of spectral purity. A PLL uses a crystal oscillator signal as a reference and stabilizes a Voltage Controlled Oscillator (VCO) through a negative feedback loop. The frequency multiplying factor of the VCO over the reference signal is determined by the frequency dividers in the loop, either in integer or fractional forms.

For applications where tunable LO signal frequencies are needed, for example targeting various operating bands or communication channels, frequency synthesizing is usually required. There are typically two types of frequency synthesizers: one type is the traditional PLL based synthesizer and the other type is more modern, the so-called Direct Digital Synthesizer (DDS). The DDS emerged with the

development of CMOS technology and became popular in the last decade. The basic architecture of a DDS system includes a clock frequency, a frequency counter, a look-up table, a register, a digital-to-analog converter and a low pass filter. Comparing with PLLs, one of the main advantages of the DDS is its flexibility in terms of its output frequency, amplitude and waveform types [2]. It becomes very challenging to generate signals from GHz frequencies onward with high spectrum purity using DDS, and PLLs based frequency synthesizing is still the most commonly used technique for LO generation.

For a fixed reference signal, the frequency synthesis is realized by manipulating the frequency divider ratios. There are cases when more complicated frequency sweeping algorithms are required, such as in Frequency-Modulated Continuous-Wave (FMCW) radar applications. A DDS can then be used to replace the crystal oscillator [3]. The combination of the DDS and the PLL can achieve a fine frequency tuning step down to sub Hertz for applications up to millimeter wave ranges.

Among the most popular semiconductor technologies, CMOS processes dominate the IC market driven by their lower cost and higher integration levels, and compound semiconductors still dominate circuit blocks where high performance is required in terms of power capability, noise, linearity and so on. While the III-V semiconductor technology keeps exploiting its market toward low noise and high power applications, SiGe HBT and BiCMOS technologies have been catching up with compatible performance but with much lower cost, and definitely play a significant role as a compromise solution between GaAs and CMOS technologies.

In mobile terminal devices nowadays, the LO generator can be integrated on the same die with the RF transceiver in a CMOS technology. However, for applications such as satellite communication, cellular base stations and so on, the LO signals usually require higher power, better noise performance, and faster settling time; the LO generator is usually implemented separately from the RF front end in different technologies, chips or even with discrete components.

The aim of this research is to investigate a fully integrated solution of high performance PLL based frequency synthesizers in a SiGe BiCMOS process and the potential to integrate the synthesizer into the complete RF transceiver front end module. Additionally, the trade-offs between the key parameters will also be studied based on the process technologies and the various PLL topologies. The PLL sub blocks such as phase/frequency detector, frequency dividers, VCOs, low pass filters will be analyzed down to transistor levels and optimized from the per-

spective of the complete performance of the PLLs, such as frequency band, power consumption, phase noise, lock time and so on.

1.2 Dissertation Outline

The dissertation is organized into the following chapters:

Chapter 2 introduces the performance requirement and specifications for PLL based frequency synthesis, in terms of frequency range and resolution, phase noise, spurious tones and lock time.

Chapter 3 describes the most widely used two types of PLL types. After a performance comparison, an innovative dual-loop PLL topology with superior phase noise performance and fast lock behavior is also introduced in this chapter.

Chapter 4 discusses in detail the sub circuit blocks design for the frequency synthesizer. It includes the design of 3 types of phase frequency detectors, frequency dividers used both as prescaler of the PLL and multi-band frequency synthesis, VCOs at various frequency bands with wide frequency tuning range, loop filters and a phase locked indicator. In the end of the chapter, the performance of each PLL block is summarized.

Chapter 5 describes the PLL simulation and optimization on a system level in terms of frequency response. Methods to achieve the best phase noise performance are discussed with reconfigurable loop parameters. To achieve a fast lock time, transient behavior is also discussed for two types of PLLs and the novel dual-loop PLL.

Chapter 6 discusses the PLL system integration together with the characterization results in 3 demonstrators targeting various applications, which include a 31.9-38.8 GHz dual-loop PLL, a 16-24 GHz frequency synthesizer and 3-5 GHz LO generation in a reconfigurable receiver front-end.

Chapter 7 summarizes the dissertation and concludes the work.

2

PLL Basic Parameters

The key performance indicators of a PLL based frequency synthesizer include operating frequency range, frequency resolution, phase noise, spurious levels and lock time. Based on targeted applications, trade-offs are required between the power consumption, cost and the key performance.

2.1 Frequency Range and Resolution

Frequency range is defined by the requirements of the targeted application. For a single loop PLL, when no further post frequency synthesis is applied, the tuning range of the VCO must cover the frequency band of the application. However, often additional function blocks must be introduced to match the targeted frequency band: if the VCO cannot oscillate up to the desired frequency, for example due to the limit of the process technology, a frequency up-conversion or multiplication is required; in another case, frequency dividers or multi-ratio frequency prescalers are essential when the LO signals shall cover a much wider frequency range than the VCO itself.

In modern communication systems, multi-band multi-standards single chip modules are common; multi-loop PLLs or post frequency synthesizing blocks are required for the LO generation to cover all the targeted frequency bands. Theoretically, for a PLL with 40% frequency tuning range, a continuous frequency sweep can be achieved using multi-ratio frequency dividers with divider ratios $1.5 \cdot 2^N$ and $2 \cdot 2^N$ $(N = 0, 1, 2...)$ as shown in Fig. 2.1.

In a PLL, the controlled swing voltage which is usually generated by a charge pump or an active loop filter shall cover as much as possible the valuable tuning voltage of the VCO. Additionally, for VCOs incorporating varactors, the frequency

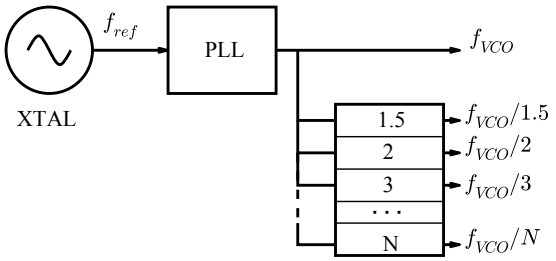


Figure 2.1: Block diagram of a typical direct frequency synthesizer

tuning gain K_{VCO} is typically non-constant. Since K_{VCO} is one of the key parameters which determine the loop behavior of the PLL, the variation of K_{VCO} may degrade the loop performance and cause instability problems. More details about the VCO designs will be described in Chapter 4.4.

The frequency resolution of a PLL is the minimum frequency step it can achieve at the synthesizer output, usually specified by the channel step size in modern communication systems. Tab. 2.1 lists the frequency bands and step size specifications for some of the most popular communication standards in Germany nowadays [4][5][6]. As one can see, the channel step size varies from 200 kHz to tens of MHz. In some applications such as satellite communications, private mobile radios or instrumentation, the frequency resolution requirement is even higher. For example, the Iridium satellite system has a channel step of 31.5 kHz in L band (1616 - 1626.5 MHz) for communication with the users; a digital Private Mobile Radio (dPMR) requires a channel step of 6.25 kHz for the dPMR446 standard.

Table 2.1: Frequency band (UL-uplink, DL-downlink) and step size specifications of some modern communication standards

Standard	**Frequency Band**	**Step size**
GSM 900	UL: 880-915 MHz, DL: 925-960 MHz	200 kHz
DCS 1800	UL: 1710-1785 MHz, DL: 1805-1880 MHz	200 kHz
LTE E-UTRA Band 7	UL: 2520-2570 MHz, DL: 2620-2690 MHz	5-20 MHz
WLAN 802.11b	2412-2484 MHz	5 MHz

Fig. 2.2 shows the block diagram of a typical PLL based frequency synthesizer. In steady state, the output frequency of the PLL can be expressed as:

$$f_{VCO} = \frac{f_{ref} \cdot N}{R} \tag{2.1}$$

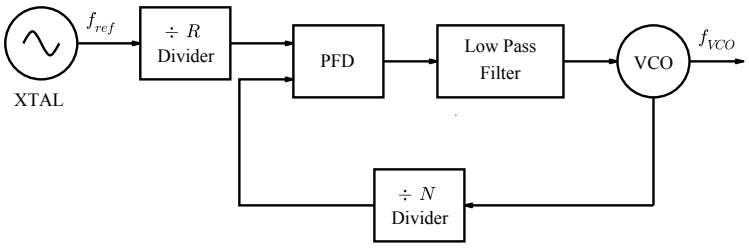


Figure 2.2: Integer-N frequency synthesizer

where f_{ref} is the reference frequency, R and N are frequency divider ratios of the reference and VCO divider.

In integer-N frequency synthesizers, the reference frequency f_{ref} is a fixed value which is typically generated from a crystal oscillator. The frequency step can be expressed by $\frac{f_{ref}}{R}$, where the divider ratio N can be swept in integer. The concept of an integer-N synthesizer is very straight forward and was adopted widely in early wireless telephony transmitter/receiver modules [7].

However, there are certain limitations for the integer-N concept. As shown in Fig. 2.2, the frequency step $\frac{f_{ref}}{R}$ is also defined as the comparison frequency of the PLL. To achieve a fine frequency resolution, the comparison frequency must be reduced accordingly. For a given output frequency band, see (2.1), a finer frequency resolution requires higher frequency divider ratio N. Taking GSM-900 applications as an example, the 200 kHz step size requires the divider ratio N to vary from 4400 to 4575 to achieve the output frequency from 880 MHz to 915 MHz. The divider ratio degrades the in-band phase noise behavior by a factor of $20 \log N$, which is more than 70 dB in this case. Meanwhile, for a stable loop behavior, the comparison frequency limits the loop bandwidth down to tens of kHz, and the loop bandwidth limits the lock time to the sub-millisecond range [8].

The fractional-N frequency synthesizer relaxes the relation between the resolution and the comparison frequency of the loop and allows the resolution to be a fractional portion of the comparison frequency [9]. Fig. 2.3 shows the basic block diagram of a Σ-Δ fractional frequency synthesizer. The frequency resolution can be described as:

$$f_{VCO} = \frac{f_{ref}}{R} \cdot (N + \frac{Q}{F}) \tag{2.2}$$

where integer F is the fractional resolution and integer Q is the fractional ratio which varies from 0 to F. Again, taking GSM-900 as an example, to achieve a

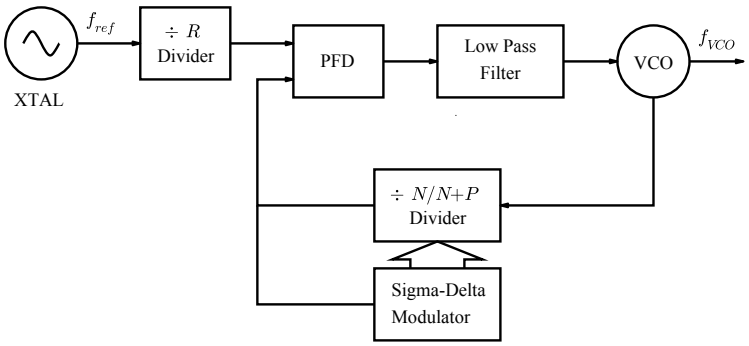


Figure 2.3: Fractional-N frequency synthesizer

frequency resolution of 200 kHz, the fractional resolution can be set to 32. The divider ratio N now can be reduced to 137, and the comparison frequency is 1.6 MHz. In comparison with the integer-N topology, the in-band phase noise contribution is now improved by 30 dB and the lock speed is in the range of microseconds.

However, the fractional-N topology will bring in fractional spurs or dithered phase noise to the PLL output. In the early 1990s, Tom A.D. Riley and his team presented a new method. Using the knowledge of the over-sampled analog to digital converters, a high order Σ-Δ modulator was introduced into the fractional-N frequency synthesizer design for noise shaping purposes [10]. It has been proved that at least a third order Multi-stAge noise SHaping (MASH) Σ-Δ modulator is required to generate an uncorrelated quantizer error sequence and thus provides sufficient noise shaping [11]. Another method to reduce the fractional spurious tones was also reported: instead of the Σ-Δ modulator, it used a new type of digital quantizer, with an additional charge pump offset and a sampled loop filter [12].

2.2 Phase Noise

Phase noise represents the rapid, short-term, random phase fluctuations of a signal in the frequency domain, while jitter represents such fluctuations in the time domain. The phase noise suppression ratio (usually also referred as "phase noise" in the literature) is defined as the ratio of the power in 1Hz bandwidth at a specific offset of the carrier frequency f_c to the carrier power, as shown in Fig. 2.4. As seen from the definition, phase noise is a parameter which describes the spectrum purity of a signal, which is one of the most critical performance parameters in frequency synthesizer designs.

For example, in a wireless receiver, the phase noise together with the spurious tones of the LO signal degrade the system performance as illustrated in Fig. 2.5.

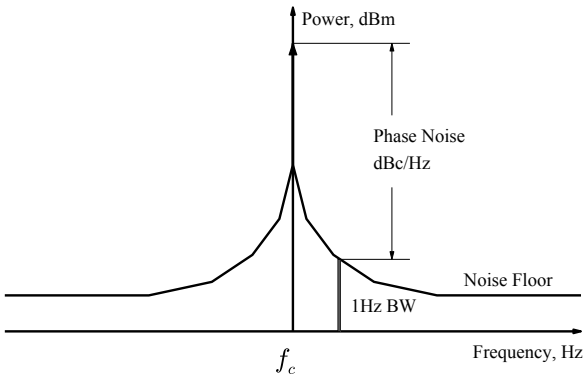


Figure 2.4: Phase noise definition on a certain carrier frequency

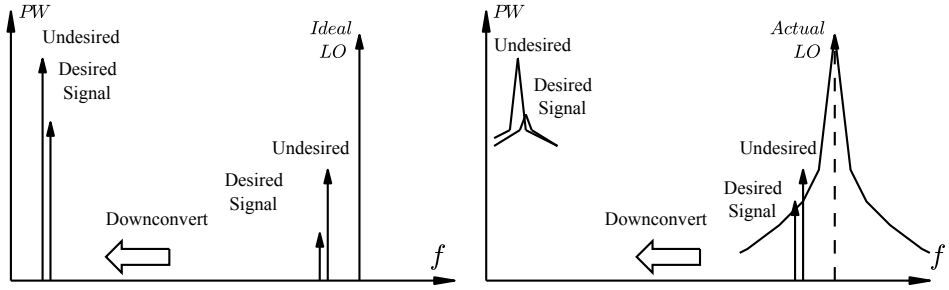


Figure 2.5: Phase noise effects on a receiver system

With an ideal LO signal, the desired signal can be demodulated to IF with no interference from the undesired signal. In practical systems, with phase noise added to the LO signal, both the desired and undesired signals will be down converted to IF with phase noise. The phase noise of the signal itself degrades the signal to noise ratio of the receiver in general. Additionally, if a strong undesired signal is close enough to the desired channel, the desired signal will be no more detectable.

Table 2.2 lists the typical phase noise specifications for wireless communication systems with some of the most common standards [13].

Table 2.2: Phase noise specifications of some popular wireless communication standards

Standards	**Phase Noise, dBc/Hz @ Hz**
WCDMA	-90 @ 10k, -113 @ 100k
GSM	-111 @ 100k, -143 @ 3M
DECT	-85 @ 100k
Bluetooth	-119 @ 3M
WLAN	-116 @ 3M

All the components in the PLL contribute to the overall phase noise of the output signals. The phase transfer mechanism is shown in Fig. 2.6, where ϕ_{in} is the phase of the reference signal; ϕ_{out} is the phase of the VCO output; $\phi_{out,d}$ is the phase of the signal at the output of the divider N; K_ϕ is the gain of the phase detector as in V; K_{VCO} is the gain of the VCO as in rad·s^{-1}V^{-1}; and $Z(s)$ is the transfer function of the loop filter.

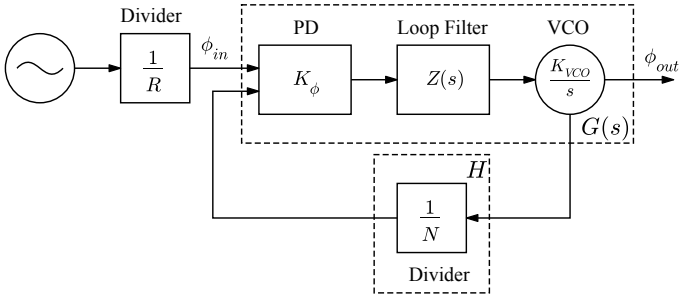


Figure 2.6: Phase transfer mechanisms in PLLs

In the frequency domain, the phase transfer functions can be expressed using the Laplace transform as follows:

$$V_d(s) = K_\phi(\phi_{in} - \phi_{out}) \tag{2.3}$$

$$V_c(s) = Z(s)V_d(s) \tag{2.4}$$

$$\phi_{out} = \frac{K_{VCO}V_c(s)}{s} \tag{2.5}$$

$$\phi_{out,d} = H\phi_{out} \tag{2.6}$$

And the closed loop phase transfer function can be expressed as:

$$\frac{\phi_{out}}{\phi_{in}} = \frac{G(s)}{1 + G(s)H} \tag{2.7}$$

where:

$$G(s) = K_\phi Z(s)\frac{K_{VCO}}{s} \tag{2.8}$$

$$H = \frac{1}{N} \tag{2.9}$$

The closed loop bandwidth ω_c is defined as the corner frequency where $GH = 1$. The phase transfer function can be approximated as:

$$\frac{G(s)}{1+G(s)H} = \begin{cases} N & f \ll \omega_c \\ G(s) & f \gg \omega_c \end{cases} \tag{2.10}$$

Tab. 2.3 lists the phase transfer functions of the PLL sub-blocks. The phase transfer functions also apply to the phase noise analysis. For the phase noise frequency which is inside the loop bandwidth, which means $GH \gg 1$, the reference oscillator, phase detector, frequency divider and loop filter dominate the overall phase noise of the PLL; for the phase noise frequency outside the loop bandwidth, which means $GH \ll 1$, the VCO dominates the phase noise of the PLL [14]. The following chapters will focus on the optimization of the intrinsic phase noise of each circuit blocks based on their transfer functions.

Table 2.3: Phase transfer functions of the PLL sub-blocks

Noise Source	**Transfer Function**	**Low Frequency**	**High Frequency**
Reference	$\frac{1}{R}\frac{G}{1+GH}$	$\frac{1}{R}N$	$\frac{1}{R}G$
Divider R	$\frac{G}{1+GH}$	N	G
Divider N	$\frac{G}{1+GH}$	N	G
Phase detector	$\frac{1}{K_\phi}\frac{G}{1+GH}$	$\frac{1}{K_\phi}N$	$\frac{G}{K_\phi}$
Loop filter	$\frac{1}{K_\phi}\frac{G}{1+GH}$	$\frac{1}{K_\phi}N$	$\frac{G}{K_\phi}$
VCO	$\frac{1}{1+GH}$	$\frac{N}{G}$	1

2.3 Spurious Tones

Besides the phase noise, spurious tones are also observed in the output spectrum at certain frequency offsets. The causes of spurious tones include the leakage from the reference and its harmonics, the fractional components from the Σ-Δ modulator, the decoupling of the power supplies and cross talk between the circuit blocks and loops and so on [15]. Of all types of spurious tones, the reference spur is the most common one in integer-N PLL designs.

For a single loop analog type PLL in the locked state, the phase error is indicated by the DC component of the phase/frequency detector output. However, the fundamental or harmonics of the comparison signals will also be presented at the phase/frequency detector output due to the detector topologies, leakage and mismatches. Depending on the offset frequencies, the out-of-band spurs can be attenuated by a well designed low pass loop filter. The non-filtered reference and

its harmonics after the loop filter will appear at the tuning port of the VCO and generate a frequency modulated signal at the output [16].

Assume that the reference signal from the phase/frequency detector output is:

$$v_{PD} = V_{PD}\cos(\omega_0 t + \phi_0) \tag{2.11}$$

where V_{PD} is the amplitude of the output of the phase detector at the reference frequency; and ω_0 is the reference frequency. After the loop filter, the signal which appears at the tuning voltage out the VCO can be expressed as:

$$v_{tune} = V_{Tune} + A \cdot V_{PD}\cos(\omega_0 t + \phi_0) \tag{2.12}$$

where V_{Tune} is the DC output of the loop filter in the locked state, A is the gain of the loop filter at ω_0. The VCO output now becomes:

$$v_{VCO} = V_{VCO}\cos\left[\omega_c t + \frac{K_{VCO}\cdot A\cdot V_{PD}}{\omega_0}\sin(\omega_0 t) + \phi_c\right] \tag{2.13}$$

where ω_c is the VCO frequency at V_{Tune}, and $K_{VCO}\cdot A\cdot V_{PD}/\omega_0$ is the modulation index m_f. In practical PLL designs, typically m_f is much smaller than one, hence the modulation is a narrow band FM. The locked PLL output now can be approximated based on the Bessel functions [17]:

$$v_{VCO} = V_{VCO}\cos(\omega_c t+\phi_c')+\frac{V_{VCO}\cdot m_f}{2}\left\{cos\left[(\omega_c-\omega_0)t+\phi_l\right]+cos\left[(\omega_c+\omega_0)t+\phi_r\right]\right\} \tag{2.14}$$

Now, the double side band spurs with an amplitude of $V_{VCO}\cdot\frac{m_f}{2}$ are observed at the offset frequency of ω_0 of the carrier. The spurious level can now be expressed as $20\log(\frac{m_f}{2})$ dB. Since ω_0 is much larger than the bandwidth of the low pass filter, a narrower loop bandwidth reduces A, thus the index m_f. Therefore, the reference spurious tones can be improved by reducing the loop bandwidth or the VCO gain.

The analysis of the reference spurs is also suitable for spurs which are caused by the harmonics of the comparison frequency and the out-of-band spurs in fractional-N PLLs. However, the fractional spur frequency can be much lower than the comparison frequency and can even be located inside the loop bandwidth, where the modulation is no more a narrow band FM. In this case, (2.14) is no more suitable for the spurious analysis. The analysis of the spurs which are inside or close to the loop bandwidth is more related with Σ-Δ fractional-N synthesizer designs [18] and is beyond the scope of this work.

2.4 Lock Time

The lock time of the PLL is one of the key parameters which influence the reaction time of a communication system. For example, to avoid interference or protect data security, a frequency hopping mechanism is required and the LO signals need to settle to the new frequency as fast as possible [19]. When the PLL locking process is not fast enough, several PLLs are commonly used to speed up the frequency hopping under the penalty of higher power consumption and costs. In early GSM & EDGE base station designs, two PLLs were applied as a "ping-pong" architecture for the LO generation, which worked alternately on the allocated channels [20].

The lock time is defined as the time it takes for a PLL to switch from an arbitrary state to a phase locked state with a specified frequency. The start state can be either an initial state after the power-on or wake-up of the system, or a previous locked state. The PLL starts with a pull-in process as shown in Fig. 2.7. The pull-in time depends on the type of the PLL, the initial frequency error, the damping factor, and the natural frequency of the PLL. In the lock-in process, the loop locks within one beat note between the comparison signals. Therefore, the lock-in time can be approximated as the reciprocal of the PLL natural frequency. More detail will be discussed in Chapter 3.

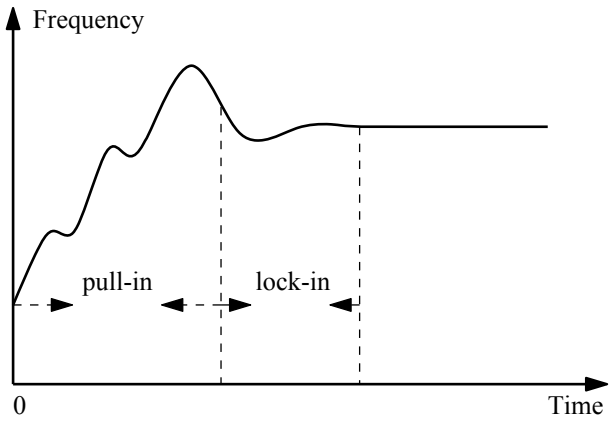


Figure 2.7: Typical transient behavior of the PLL output frequency

3

Introduction of PLL Types

PLLs can be classified according to their use of phase/frequency detectors, frequency dividers or the loop filters. PLLs using mixer type phase detectors are called analog PLLs or linear PLLs; those using digital phase/frequency detectors such as EXOR gates and 3-state Phase Frequency Detectors (PFDs) are called digital PLLs (DPLLs). Even though the term "digital" is used, the loop filter and the VCO in DPLLs are still implemented with analog circuits. All-DPLLs use digital blocks only, including the loop filter and the VCO [21]. Based on the divider used, PLLs can be distinguished as either integer-N or fractional-N; more details see Section 4.4. With respect to the order of the loop filter, PLLs can be defined as second order (type II), third order (type III) and high order PLLs [22]. PLLs can also be discriminated by the type of loop filter - passive or active.

The following sections will mainly focus on the PLL types based on the variation of the phase/frequency detectors. In the final section, we will introduce an innovative dual-loop PLL which combines both an analog phase detector and a digital PFD, both an active loop filter and a passive loop filter into the PLLs. The dual-loop PLLs have several advantages over single loop types of PLLs.

3.1 Analog PLLs

An analog PLL (APLL) has four essential blocks: a reference oscillator, a mixer type phase detector, a low pass filter and a voltage controlled oscillator. Frequency dividers are also needed when the VCO frequency is higher than the reference oscillator frequency or frequency synthesizing is required. The block diagram of an analog PLL is shown in Fig. 3.1.

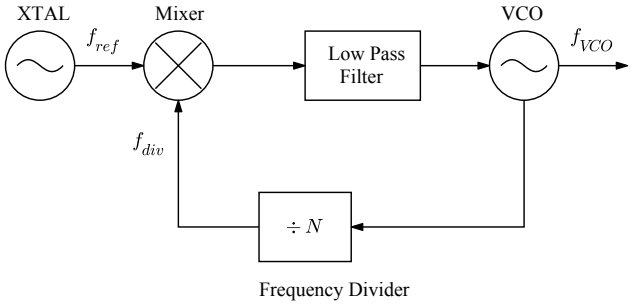


Figure 3.1: Block diagram of an analog PLL (APLL)

The mixer compares the two input signals from the reference and the VCO (or divider) output. Assuming the inputs are sinusoidal and the mixer operates in the multiplier mode, the output of the mixer contains two spectral components as shown in (3.4):

$$\begin{aligned} v_{Ref} &= V_{Ref} \cdot \cos(\omega_{Ref} t + \phi_{Ref}) && (3.1)\\ v_{VCO} &= V_{VCO} \cdot \cos(\omega_{VCO} t + \phi_{VCO}) && (3.2)\\ v_{out} &= K \cdot V_{Ref} \cdot V_{VCO}[\cos((\omega_{Ref} - \omega_{VCO})t + \phi_{Ref} - \phi_{VCO}) && (3.3)\\ &\quad + \cos((\omega_{Ref} + \omega_{VCO})t + \phi_{Ref} + \phi_{VCO})] && (3.4) \end{aligned}$$

where v_{Ref} and v_{VCO} are the reference and the VCO signals with frequency ω_{Ref} and ω_{VCO} ; V_{Ref} and V_{VCO} are the amplitudes of the input signals; ϕ_{Ref} and ϕ_{VCO} are the initial phases; K is the gain of the mixer. The component corresponding to the sum of the input frequencies ω_{sum} (here $\omega_{Ref} + \omega_{VCO}$) is suppressed in the low pass filter, while the difference frequency component $\Delta\omega$ (here $\omega_{Ref} - \omega_{VCO}$) represents the frequency error signal. When the initial comparison signals have the same frequency but differ in phase, the difference signal is then a DC signal $K \cdot V_{Ref} \cdot V_{VCO} \cdot \cos\Delta\phi$, which indicates only the phase error of the input signals. The negative feedback loop controls the phase via the VCO such that the difference signal becomes minimum. When the difference signal of v_{out} is zero, the phase error magnitude $|\Delta\phi|$ is $\frac{\pi}{2}$.

The loop filter can be designed using a passive lag, an active lag, a passive low pass filter or an active Proportional Integral (PI) low pass filter. The VCO in the loop generates an additional pole in the transfer function of the PLL; the PLL order is always the loop filter order plus one. APLLs with active PI filters (as shown in Fig. 3.2) have a wider hold range than the ones using passive types. From (2.8), the transfer function of an open loop is rewritten now as in (3.5).

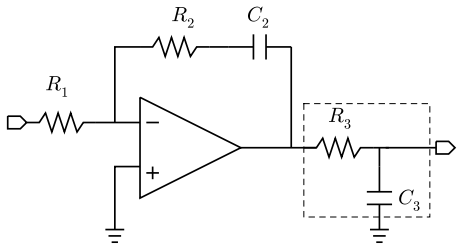


Figure 3.2: Active PI filter with an additional RC stage

$$\frac{\phi_{div}}{\phi_{Ref}} = \frac{sR_2C_2+1}{sR_1C_2(sR_3C_3+1)}K_\phi\frac{K_{VCO}}{sN} \tag{3.5}$$

where K_ϕ and K_{VCO} are the gain of the phase detector and the VCO, respectively. The new transfer function has a frequency response of a 3^{rd} order low pass filter formed by two poles from the loop filter and an additional pole from the VCO. The pole generated by R_3 and C_3 creates a higher frequency roll-off to suppress the spur levels [23]. The pole is usually located between the natural frequency ω_n and the frequency of the first order reference spur, which creates an additional spurious attenuation of 20 dB/dec typically. The amplitude Bode plot of the open loop transfer function of the 3^{rd} order PLL is shown in Fig. 3.3, where $\tau_1 = R_2C_2$ and $\tau_2 = R_3C_3$.

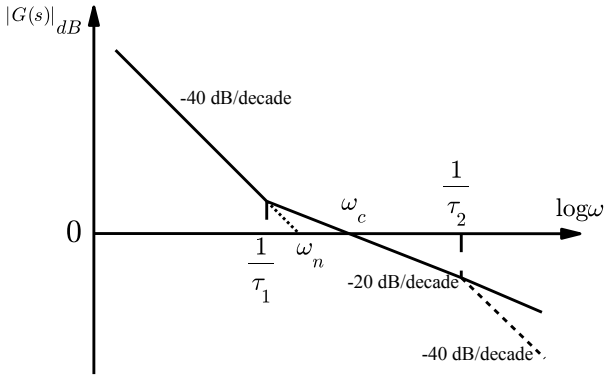


Figure 3.3: Bode plot of the open loop transfer function of the 3^{rd} order APLL

Based on (2.7), the closed loop transfer function is now re-written as:

$$H(s) = \frac{sR_2C_2+1}{s^2\frac{R_1C_2}{K_\phi K_{VCO}}(sR_3C_3+1)+s\frac{R_2C_2}{N}+\frac{1}{N}} \tag{3.6}$$

To simplify the analysis of the frequency response of the 3^{rd} order PLL, the influence of the additional pole on the frequency close to the loop bandwidth can

be neglected, however it will be considered for the analysis of the spurious level attenuation. The loop transfer function as shown in (3.6) can now be simplified as:

$$H(s) = \frac{sR_2C_2 + 1}{s^2\frac{R_1C_2}{K_\phi K_{VCO}} + s\frac{R_2C_2}{N} + \frac{1}{N}} \tag{3.7}$$

The denominator of $H(s)$ is written in a normalized form: $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ω_n is the natural frequency of the loop, and ζ is the damping factor:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{R_1C_2N}} \tag{3.8}$$

$$\zeta = \frac{R_2C_2}{2}\sqrt{\frac{K_\phi K_{VCO}}{R_1C_2N}} \tag{3.9}$$

The pull-in range $\Delta\omega_P$ of a PLL is defined as the initial frequency error of the reference frequency and the output frequency, within which the phase can be locked. The lock-in range $\Delta\omega_L$ of a PLL is defined as the initial frequency error, within which the phase can be locked with no cycle slip. Typically, if the initial frequency error is distinctly smaller than the pull-in range, the pull-in time T_P and the lock-in time T_L can be approximated as: [24]

$$T_P = \frac{\pi^2}{16}\frac{{\Delta\omega_0}^2}{\zeta{\omega_n}^3} \tag{3.10}$$

$$T_L = \frac{2\pi}{\omega_n} \tag{3.11}$$

where ω_n is the natural frequency of the feedback loop, and ζ is the damping factor. The damping factor ζ is usually between 0.7 and 1. The pull-in time and the lock-in time are significantly dependent on the natural frequency ω_n. However, for a given comparison frequency of the PLL, a higher loop bandwidth ω_n will reduce the out-of-band spurious tones attenuation. To maintain the same attenuation level, a higher comparison frequency or a higher order loop filter is required.

3.2 Digital PLLs

In DPLLs, the mixer is replaced by phase detection blocks such as EXOR or JK flip-flops. A 3-state PFD (see 4.2.3) is one of the most popular PFD types in modern PLL designs. The signals to be compared are converted to digital logic signals. Instead of detecting the phase error in real-time even inside one signal

period, the digital phase detectors detect only the signal edges. The phase error of the comparison signals are presented as pulses with varying widths at the phase detector output. It has an unlimited phase detection range and can also detect the polarity of the frequency error. This is very important especially in systems where frequency hopping is required.

The 3-state PFD is usually followed by a charge pump in a DPLL. After the charge pump, the phase error voltage is converted to a phase error current. The phase error current gain $K_{\phi,I}$ [1] is the maximum source/sink current of the charge pump I_{cp}.

With the low pass loop filter, the pulses are smoothed and used as the control signal to the VCO. The block diagram of a DPLL is shown in Fig. 3.4.

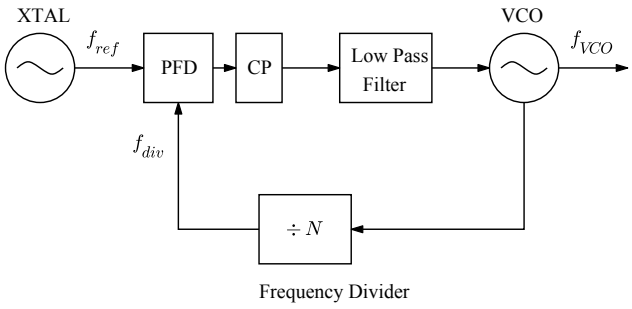


Figure 3.4: Block diagram of a DPLL

A typical passive loop filter for DPLLs is shown in Fig. 3.5. When the output voltage of the charge pump is not sufficient to cover the effective tuning voltage of the VCO, an active loop filter is required.

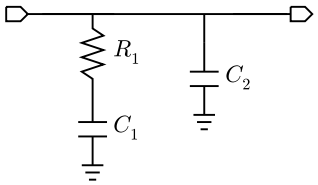


Figure 3.5: Passive low pass filter with an additional RC stage

From (2.8), the transfer function of an open loop is rewritten now as:

$$\frac{\phi_{VCO}}{\phi_{Ref}} = \frac{sR_1C_1 + 1}{s^2R_1C_1C_2 + s(C_1 + C_2)} \cdot I_{cp} \cdot \frac{K_{VCO}}{sN} \tag{3.12}$$

[1] The physical unit of the phase error current gain is A. However in some literatures, unit A·rad^{-1} is used .

where K_{VCO} is the gain of the VCO.

The amplitude Bode plot of the open loop transfer function of the 3^{rd} order DPLL is shown in Fig. 3.6. where $\tau_1 = R_1 C_1$ and $\tau_2' = R_1 \frac{C_1 C_2}{C_1 + C_2}$.

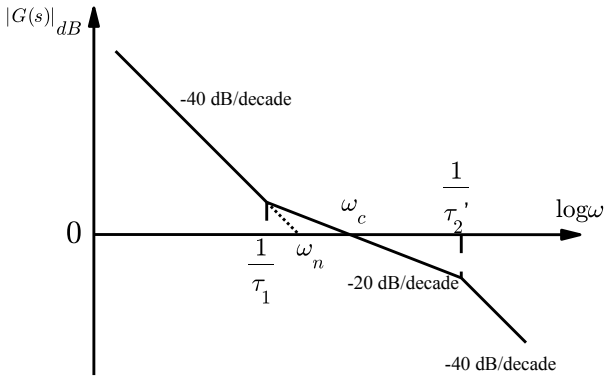


Figure 3.6: Bode plot of the open loop transfer function of the 3^{rd} order DPLL

Based on (2.7), the closed loop transfer function is now re-written as:

$$H(s) = \frac{sR_1C_1 + 1}{s^2 \frac{C_1+C_2}{I_{cp}K_{VCO}}(sR_1\frac{C_1C_2}{C_1+C_2} + 1) + s\frac{R_1C_1}{N} + \frac{1}{N}} \tag{3.13}$$

As a rule of thumb, since the capacitance C_1 is around 10 times larger than C_2, the closed loop function of the DPLL can be simplified as:

$$H(s) = \frac{sR_1C_1 + 1}{s^2 \frac{C_1}{I_{cp}K_{VCO}} + s\frac{R_1C_1}{N} + \frac{1}{N}} \tag{3.14}$$

The denominator of $H(s)$ is written in a normalized form: $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ω_n is the natural frequency of the loop, and ζ is the damping factor:

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{C_1 N}} \tag{3.15}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_{cp}K_{VCO}C_1}{N}} \tag{3.16}$$

The pull-in time and the lock-in time can be expressed as:

$$T_P = \frac{\Delta\omega_0}{\pi\omega_n^2} \tag{3.17}$$

$$T_L = \frac{2\pi}{\omega_n} \tag{3.18}$$

The pull-in time is proportional to the initial frequency error $\Delta\omega_0$. Differing from the APLL, (3.17) is valid for any initial frequency errors.

3.3 A proposed novel dual-loop PLL

As discussed in Chapter 2, for a single loop PLL, trade-offs must be made between the phase noise, spurious level and lock time. Many techniques have be developed to optimize the PLL performance, in order to achieve lower noise, lower spurious level and faster lock time simultaneously. An adaptive loop bandwidth control technique was presented in [25] for a single loop DPLL, which used a higher loop bandwidth in the frequency acquisition process and switched to a lower loop bandwidth in the phase tracking process adaptively. Adjusting the loop bandwidth by the charge pump current resulted a faster lock time and a lower spurious level simultaneously. In [26], the bandwidth was controlled by switching the resistance of the RC loop filter. A dual-loop topology was presented in [27], which used a phase frequency detector and a Phase Error Detector (PED) to drive the charge pump; a coarse tuning was controlled by the PFD with a higher phase error gain while the PED realized a fine tuning with a lower phase error gain and narrower bandwidth.

In this work, a novel dual-loop topology is designed, which uses two types of phase detectors to optimize the PLL performance. Typically, the mixer type PD has a much lower flicker noise level and faster operating speed than a 3-state PFD [28]. The reason that the mixer type PD gets less popular in modern PLL designs is its limited frequency acquisition range. In the proposed dual-loop topology, the mixer type PD is used as the phase locked hold loop in the steady state; the 3-state PFD is designed for the frequency acquisition process, since it has a much wider frequency acquisition range (infinite theoretically) than the mixer. To avoid the noise interference from the frequency acquisition loop to the phase locked hold loop, the 3-state PFD is isolated from the PLL by a lock detection block when the PLL achieves the steady state. The block diagram of the dual-loop PLL is shown in Fig. 3.7.

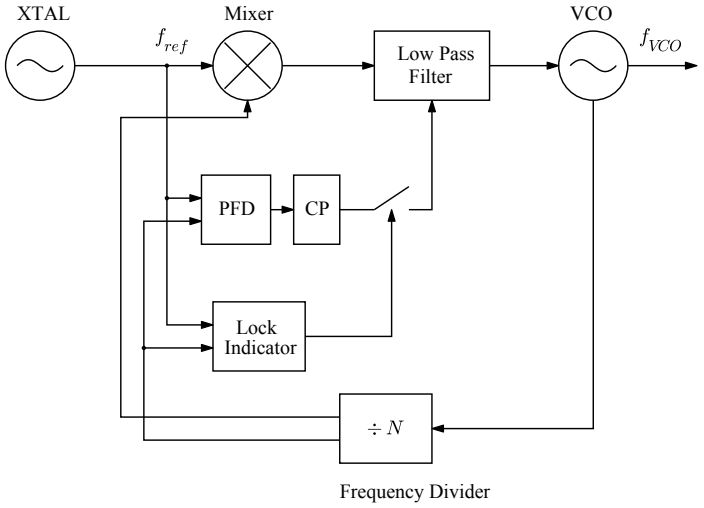


Figure 3.7: Block diagram of the dual-loop PLL with two types of phase detectors

This topology shows more advantages especially when the PLL operates in a high frequency range (above X band). Traditional 3-state PFDs have a limited operating frequency range below 200 MHz. For an integer-N PLL design, a lower comparison frequency requires a higher divider ratio N. As discussed in Section 2.2, the phase noise of the PLL inside the loop bandwidth degrades by a factor of $20 \cdot \log N$. Since the mixer type PD has much higher operating frequency range with ultra-low noise level when compared to a 3-state PFD, using the mixer type PD, the divider ratio N is reduced to improve the noise performance. A wider loop bandwidth now can be designed to achieve a faster phase lock time. Additionally, a higher comparison frequency shifts the reference spurious tones to a higher offset frequency, the spurious level will not be increased by increasing the loop bandwidth.

4

Sub-Circuit Designs

In this chapter, the key blocks of the PLLs will be discussed in detail including topology designs, simulation and performance optimization. The chapter is distributed into the following sections: an overview of the technology used in this work; design of phase frequency detectors, frequency dividers/prescalers, loop filters, voltage controlled oscillators, a charge pump, a phase-locked indicator and summaries of the key performance of the sub blocks.

4.1 Technology

The 0.25 µm SiGe BiCMOS technology SG25H3 from IHP Electronics is used in this work. It provides an npn-HBT module with a SiGe:C base with up to 120 GHz transit frequency and 180 GHz maximum oscillation frequency. Additionally, 3 different breakdown voltages (BV_{CEO}) for the npn-HBTs are offered. The technology also provides NMOS, PMOS, isolated NMOS and passive components such as poly resistors and MIM capacitors. [29]

Tab. 4.1 lists the key parameters of the three types of npn HBTs.

The high performance type HBT is most widely used in this work because of its superior frequency behavior. Fig. 4.1 shows the transit frequencies of the high performance type HBT over various collector currents I_C and collector-emitter voltages V_{CE}; the transit frequencies peak at $I_C \approx 2$ mA with $A_E = 0.22 \times 0.84$ µm^2. The maximum f_T increases with V_{CE} increasing from 0.5 to 2 V.

The minimum noise figure NF_{min} of the high performance HBT is simulated at different operating frequencies as shown in Fig. 4.2. In most cases, the minimum noise figure and the maximum transit frequency cannot be achieved simultaneously at the same bias condition; trade-offs are necessary among the performance parameters such as gain, noise figure and power consumption [30].

Table 4.1: Comparison of the key parameters of the HBTs from SG25H3 technology. A_E is the minimum allowed emitter area

Parameter	**High Performance**	**Medium Voltage**	**High Voltage**
A_E, µm^2	0.22 × 0.84 (shp1)	0.22 × 2.24	0.22 × 2.2
f_T, GHz	120	45	25
f_{max}, GHz	180	140	80
BV_{CEO}, V	2.3	5	7
BV_{CBO}, V	6	15.5	21
β	150	150	150

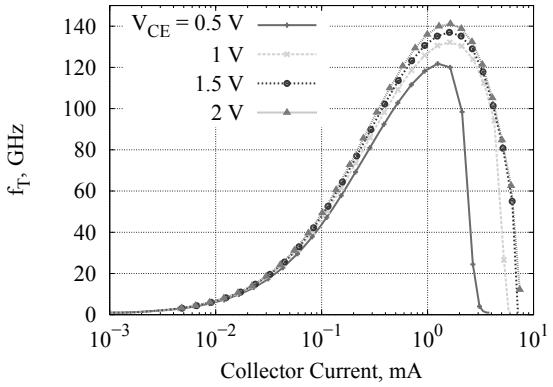


Figure 4.1: Transit frequency f_T of the high performance type versus bias points, $A_E = 0.22 \times 0.84$ µm^2

In a bipolar transistor, the flicker noise current at the base is expressed as a function of the base current I_B, and the emitter junction area A_E as in (4.1) [31]:

$$S_{I_B} = \frac{K}{A_E} I_B^{\alpha} \frac{1}{f} \tag{4.1}$$

where K is a constant based on technologies. In modern transistors, the typical value of α is 2.

For a single device, the analysis of I_B is more useful, since it provides the information of number fluctuation of the carrier in the junction. However, from the circuit design point of view, the analysis of the I_C is more valuable since most of the RF figures of merit fundamentally depend on I_C instead of I_B. The flicker noise at the collector is expressed as:

$$S_{I_C} = \frac{K'}{A_E} \frac{I_C}{\beta^{\alpha}}^{\alpha} \frac{1}{f} \tag{4.2}$$

where β is the current gain of the HBT in a given bias point.

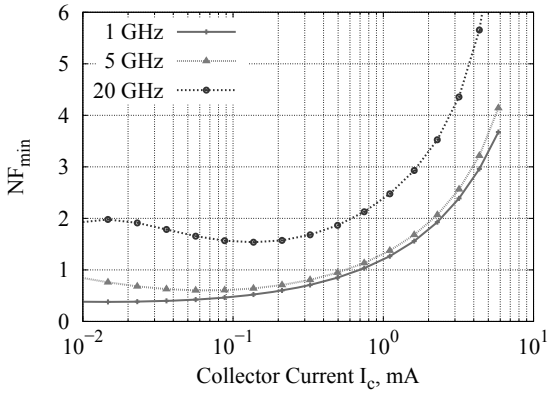


Figure 4.2: Minimum noise figure NF_{min} of the high performance HBT versus collector current and operating frequency, $A_E = 0.22 \times 0.84$ μm^2, $V_{ce} = 1.5$ V

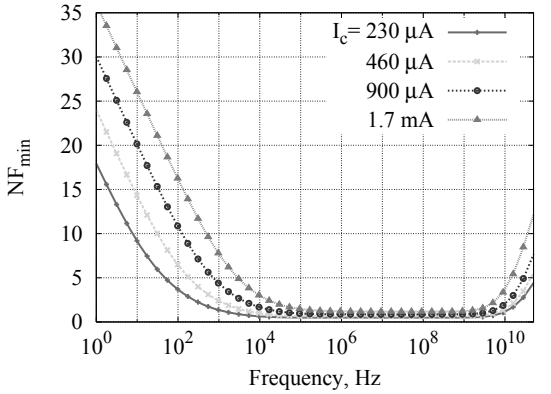


Figure 4.3: Minimum noise figure NF_{min} of the medium voltage type HBT versus operating frequency and collect current, $A_E = 0.22 \times 2.24$ μm^2, $V_{ce} = 2$ V

Fig. 4.3 shows the noise behavior of the medium voltage type HBTs at various bias points versus frequency sweeping from 1 Hz to 50 GHz. The 1/f noise (flicker noise) is strongly dependent on the collect current I_C; the noise corner frequency varies from 100 Hz to 3 kHz with I_C increasing from 230 μA to 1.7 mA.

The technology offers 5 metal layers, with thicknesses of 0.58, 0.73, 0.73, 2 and 3 μm from bottom to top, The 5 layers are named as "Metal1", "Metal2", "Metal3", "TopMet1" and "TopMet2". The substrate has a resistivity of 50 Ω·cm.

Four types of resistors are offered with characteristic parameters listed in Tab. 4.2. Among the four resistor types, type "Rppd", which utilizes unsalicided, p-doped gate polysilicon as the resistor material, has the lowest temperature coefficient of its resistance. The resistor type "Rhigh" has the highest sheet resistance and can be used as compensation for the "Rppd" type where higher resistive values are required and the chip area becomes critical.

Table 4.2: Four types of resistors offered by SG25H3 technology from IHP

Parameter	**Rsil**	**Rpnd**	**Rppd**	**Rhigh**
Sheet Resistance, $\Omega/\square$	6.9	210	280	1600
Maximum Current Density, mA/µm	2.0	0.5	0.3	0.23
Temperature Coefficients, ppm/K	2980	-536	-30	-2500
ppm/K^2	0.2	0.98	0.75	5

4.2 Phase/Frequency Detectors

In phase/frequency detector designs, the key performance parameters include phase detector gain K_ϕ, maximum error detecting range $\phi_{d,max}$, maximum operating frequency $f_{d,max}$, and phase noise PN_d.

A mixer type phase detector, an EXOR and a 3-state PFD will be discussed respectively in this section.

4.2.1 A Mixer Type Phase Detector

As discussed in chapter 2.3, the leakage of the comparison signals and their harmonics create reference spurs at the PLL output. Mixer type phase detectors are usually designed using double balanced topologies such as a passive ring mixer or a Gilbert mixer, which have better port-to-port isolation and lower DC offsets than the single balanced ones. A double-balanced ring mixer has a conversion loss of 6 to 8dB, therefore requires input signals with higher power level to achieve the same output power as the Gilbert mixer. The operating frequency of a phase detector is usually below 1 GHz; a ring mixer in this range needs bulky transformers and a Gilbert mixer is much more compact.

A Gilbert cell, as shown in Fig. 4.4, includes a transconductance stage (Q_1,Q_2) and a switching quad ($Q_3 \sim Q_6$).

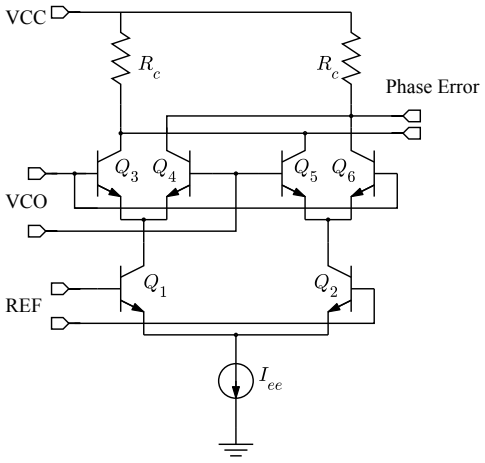


Figure 4.4: Gilbert mixer core using HBT technologies

The output of the Gilbert mixer can be expressed as:

$$v_{out} = I_{ee} R_c \tanh \frac{v_{Ref}}{2V_T} \tanh \frac{v_{VCO}}{2V_T} \tag{4.3}$$

where I_{ee} is the bias current for the emitter coupled pair; R_c is the load resistance; and V_T is the thermal voltage, which is around 26 mV at room temperature. When the mixer is used for phase detecting, the amplitudes of the two input signals are much higher than 26 mV. The maximum output voltage can be approximated as:

$$V_{max} \approx I_{ee} R_c \tag{4.4}$$

The error voltage is a function of the phase differences of the two comparison signals [32]:

$$V_{error} = I_{ee} R_c (\frac{2|\phi_{error}|}{\pi} - 1) \tag{4.5}$$

The phase detector gain K_ϕ can be expressed as:

$$K_\phi = \frac{2 I_{ee} R_c}{\pi} \tag{4.6}$$

As discussed in Chapter 2, the in-band phase noise of the PLL is partly contributed by the low frequency noise of the phase detector, where flicker noise dominates.

The flicker noise increases with the increase of the collector current. However, from (4.6), to achieve the same phase detector gain, lower collector current requires larger load resistance, which increases also the thermal noise voltage at the mixer output. The collector current and transistor size shall be optimized based on the tradeoffs between the flicker noise, thermal noise floor, gain and input matching.

In a Gilbert cell, the flicker noise in the switch quad appears directly at the mixer output. The flicker noise in the transconductance stage is up-converted to the phase noise of the LO leakage and its odd order harmonics at the output. Therefore, the transconductance stage does not contribute flicker noise directly to the output, provided that the transistors in the quad core are switched on and off ideally [33]. In practical designs, with the mismatches among the quad core transistors, the flicker noise from the transconductance stage leaks slightly through the mixer quad to the output. Fig. 4.5 shows the flicker noise contribution from the two stages. To have a fair comparison, the transistor sizes of the two stages were properly selected according to (4.2), such that they have similar intrinsic flicker noise.

The complete schematic of the analog phase detector is shown in Fig. 4.6. Emitter followers worked as level shifters. Resistive emitter degeneration was used to improve the dynamic range of the reference input ports. RC low pass filters with

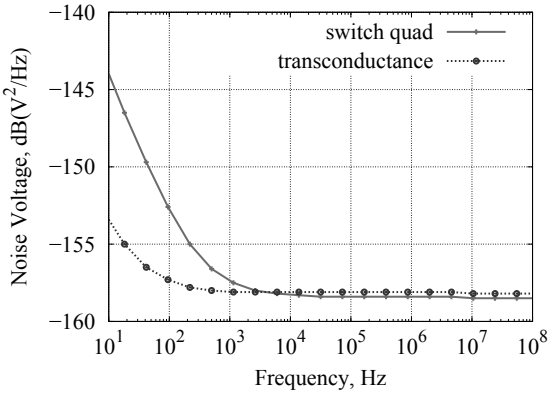


Figure 4.5: Flicker noise contribution from the transconductance stage and the switch quad of the Gilbert mixer core.

a corner frequency of around 80 MHz were also added for pre-filtering of the phase error voltage. The tail current of the emitter coupled pair was biased at 1.3 mA.

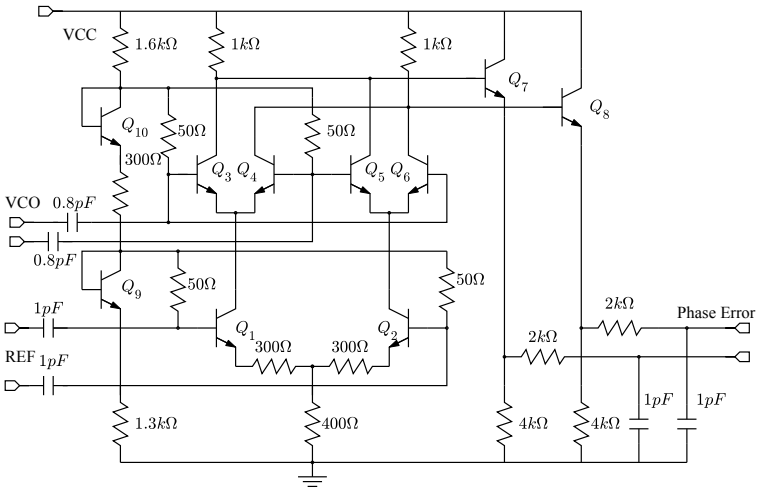


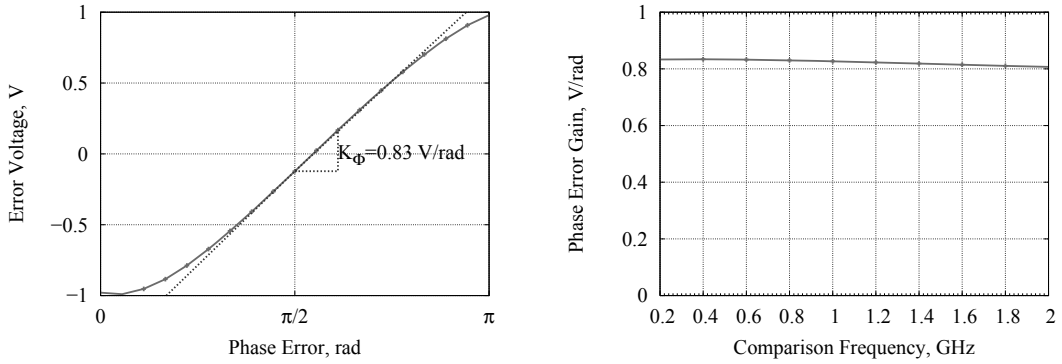
Figure 4.6: Schematic of the Gilbert mixer as phase detector. $Q_{1,2}$ = MV4×2, $Q_{3,4,5,6}$ = MV1×2, $Q_{7,8}$ = MV1×2, $Q_{9,10}$ = shp1 (see Tab. 4.1)

In an APLL, when the two comparison signals are in the locked state, the tuning voltage for the VCO is:

$$V_{tune} = V_{error} \cdot G_{filter} + V_{offset} \tag{4.7}$$

where G_{filter} is the DC gain of the low pass filter, which is above 20 dB for active loop filters (see Section 4.5); V_{offset} is the DC offset of the filter output. The effective tuning voltage for the VCO in this work is from 0 to 5 V (see Section 4.3). Fig. 4.7(a) shows the output phase error voltage versus the input phase error. At the offset voltage set to 2.5 V, the phase error voltage in the locked state is limited

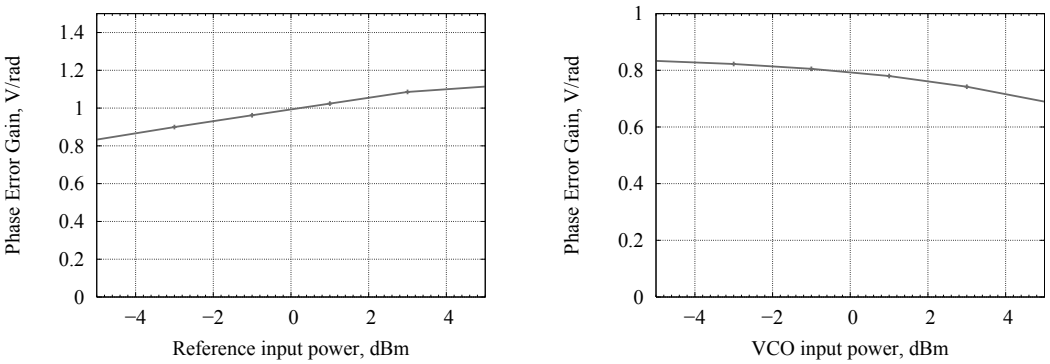
within ±0.25 V. The phase error gain is around 0.83 V and quasi constant within the effective phase error voltage region.



(a) (b)

Figure 4.7: (a)Phase error voltage at 1 GHz comparison frequency, P_{Ref} = -5 dBm, P_{VCO} = -5 dBm (b)Phase error gain varies with comparison frequency, P_{Ref} = -5 dBm, P_{VCO} = -5 dBm

Fig. 4.7(b) shows the frequency response of the analog PD. The phase error gain varies from 0.855 V to 0.8 V in the frequency range of 200 MHz to 2 GHz.



(a) (b)

Figure 4.8: (a)Phase error gain versus reference power at P_{VCO} = -5 dBm, (b) Phase error gain versus VCO power at P_{ref} = -5 dBm. Comparison frequency = 500 MHz

Fig. 4.8 shows the phase error gain with various the input power levels of the two comparison signals. At 500 MHz, the gain varies from 0.8 to 1.1 V for the input power at the reference port varying from -5 to 5 dBm, and from 0.82 to 0.7 V for the input power at the VCO port varying from -5 to 5 dBm.

The noise performance of the phase detector is shown in Fig. 4.9. The corner frequency is around 3 kHz, and the noise floor is around -158 dBV^2/Hz. The

noise performance is independent of the comparison frequency, which is one of the advantages compared with the digital phase frequency detectors.

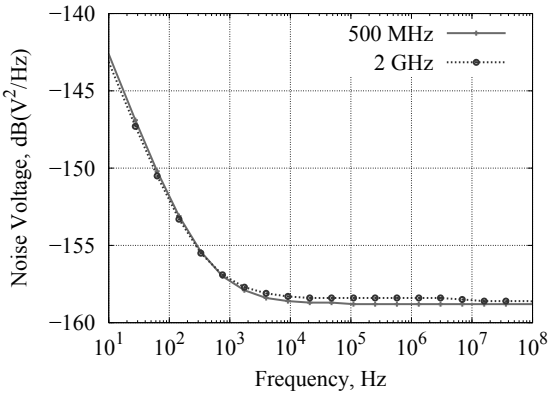


Figure 4.9: Simulated low frequency noise power at a comparison frequency of 500 MHz and 2 GHz, P_{Ref}=-5 dBm, P_{VCO}= -5 dBm

The complete power consumption of the phase detector is 2.7 mA at 3.3 V supply.

4.2.2 An EXOR Phase Detector

An exclusive OR is able to detect the phase difference between two square wave signals. When the two comparison signals are in phase, the output of the EXOR indicates logic low; when the two comparison signals are 180° out of phase, the output indicates logic high.

The EXOR in this work was implemented using CMOS transistors in the IHP SiGe BiCMOS technology with a minimum gate length of 240 nm. The phase error voltage response is shown in Fig. 4.10. The phase detecting range is π and the phase error gain is around 1 V, which is quasi constant over the complete phase detecting range.

The power consumption of the EXOR is around 140 µA at 3.3 V supply. The EXOR circuit was chosen as a phase detector for the phase locked indicator block in this work, which be discussed in Section 4.6.

4.2.3 A 3-State Phase Frequency Detector

The 3-state PFD is one of the most popular phase frequency detectors in modern PLL designs, mainly because it can detect both the phase and frequency errors of two signals. The schematic of the PFD is shown in Fig. 4.11: it combines 5 NAND

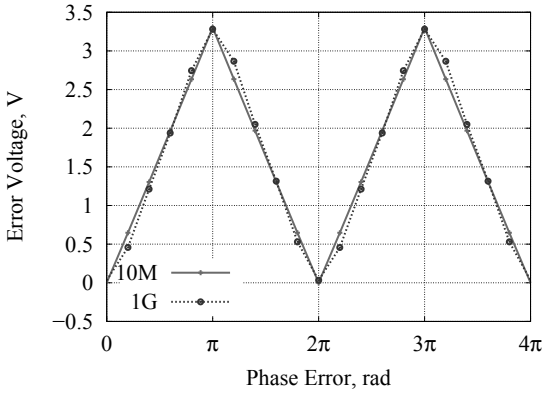


Figure 4.10: Simulated phase error voltage of the EXOR at 10 MHz and 1 GHz frequency, both inputs are square wave signals with $V_H = 3.3$ V, $V_L = 0$ V

gates and 2 RS-Flip-Flops. The outputs of the PFD are labeled as "U" and "D" representing the up and down state, respectively.

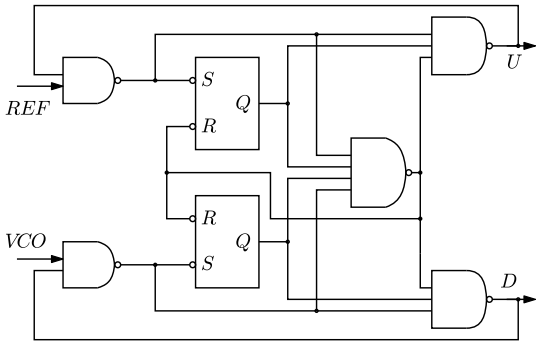
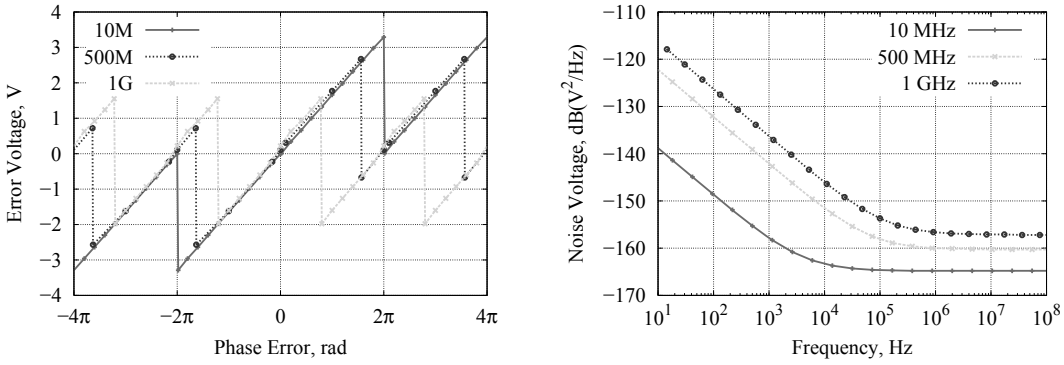


Figure 4.11: Schematics of the 3-state Phase frequency detector

The PFD in this design was implemented using CMOS transistors with a minimum gate length of 240 nm. Fig. 4.12(a) shows the error behavior at various comparison frequencies. At 10 MHz, the phase detecting range is 4π. The phase error gain at 3.3 V supply is 0.52 V over the complete phase detecting range. The phase/frequency detecting range degrades with the increased comparison frequency. At 1 GHz, the PFD cannot distinguish frequency errors, and the phase detecting range is reduced to 2π.

The noise behavior of the PFD is shown in Fig. 4.12(b). At 10 MHz comparison frequency, the flicker noise of the 3-state PFD is comparable with the mixer type PD, while the noise floor of the 3-state PFD is even lower. With frequency increased from f_1 to f_2, the flicker noise of the PFD degrades by $10 \cdot \log(f_2/f_1)$ dB. This is mainly because, after the comparator converts the input signals to the digital levels, the PFD only senses the edges of the input signals, and the jitter contributes more

phase noise to the output at higher comparison frequencies. At 1 GHz comparison frequency, the flicker noise is increased to -126 dBV^2/Hz at 100 Hz offset frequency. The complete power consumption of the PFD is 1 mA at 3.3 V supply.



(a) (b)

Figure 4.12: (a) Simulated phase error voltage for different comparison frequencies 10 MHz, 500 MHz and 1 GHz (b) Simulated low frequency noise of the PFD at comparison frequency 10 MHz, 500 MHz and 1 GHz

4.2.4 Charge Pump

A charge pump is usually used together with the 3-state phase frequency detector in PLL designs. Cooperating with the loop filter, it converts the logic states at the PFD output ports into a stabilized analog voltage signal to control the VCO frequency [34].

Same as the 3-state PFD, the charge pump in this work is implemented in CMOS. Fig. 4.13 shows the simplified schematic of the charge pump with an additional enable state which comes from the phase locked indicator. In the frequency acquisition and phase locking process, the charge pump is enabled. The inputs of the charge pump are fed directly from the phase error of the PFD outputs, which means only three states are available for the charge pump inputs. In state (1,0), P_1 is switched off and N_1 is switched on; the charge pump output indicates a low voltage and sinks the current back. In state (0,1), P_1 is switched on and N_1 is off, the charge pump outputs a high voltage and charges the load capacitance. In state (1,1), both P_1 and N_1 are switched off and the charge pump is in high impedance mode and therefore is isolated from the load. In the phase locked state, the charge pump is disabled, P_2, N_2 are switched on, and the output indicates only a DC offset voltage which is decided by R_1 and R_2. The sizes of the transistors are listed in Tab. 4.3

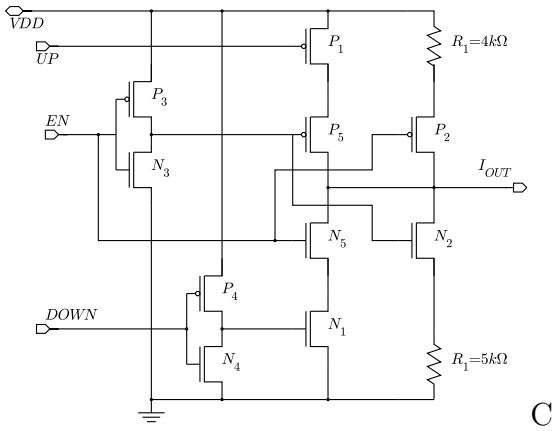


Figure 4.13: Simplified schematic of the charge pump for frequency acquisition loop

Table 4.3: Values of the key components of the charge pump, w and l are the channel width and length of the CMOS transistors

N_1	w= 4 μm, l = 270 nm	$P_{1,2}$	w= 7 μm, l = 270 nm
N_{2-4}	w= 2 μm, l = 270 nm	$P_{3,4}$	w= 2 μm, l = 270 nm
N_5	w= 10 μm, l = 270 nm	P_5	w= 10 μm, l = 270 nm

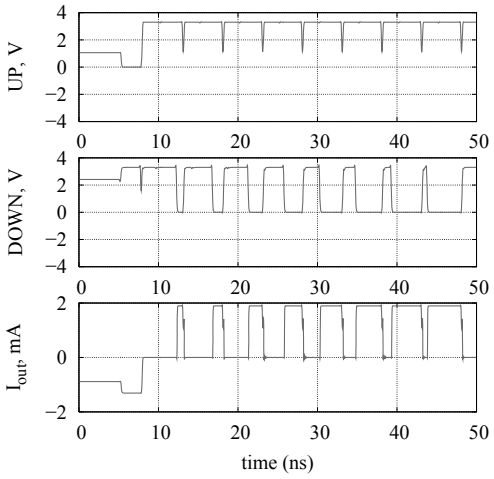


Figure 4.14: Transient behavior of the charge pump with 3-input states

Fig. 4.14 is the transient behavior of the charge pump with 3 input states from the PFD. The frequencies of the comparison input squared wave signals are 200 MHz and 222.2 MHz; the output error is now converted to the steering current with a peak current of 1.8 mA. In stand-by mode, the current consumption of the charge pump is around 370 μA at 3.3 V supply.

When the phases of the two input signals of the 3 state PFD are close enough,

the output pulse from the PFD is getting very narrow and the amplitude of the pulse starts to reduce due to the speed limitation and the capacitive load charging on the charge pump. When the amplitude of the pulse reduces below the gate threshold of the charge pump, only a sub-threshold current can pass through the load and a dead zone is presented in the output of the charge pump. Methods have been discussed in the literature to avoid the dead zone problem such as adding an additional delay in the PFD to avoid the narrow pulses appearing at the same time at the PFD output [35] or using a double edge checking technique to avoid the up and down signals rising at the same time [36] and so on. In this work, the charge pump works only during the frequency acquisition phase, and will be disabled in the phase locked state. Therefore, the dead zone problem is negligible here.

4.2.5 Summary

Three types of phase detectors were discussed in this section. The mixer type phase detector could work in a relative high frequency without degrading the phase noise. The 3-state phase frequency detector could detect both the phase and frequency errors. However, the speed of the PFD was limited to below 1 GHz, and tradeoffs were required between noise and operating frequency. The EXOR type phase detector was less complex than a 3-state PFD and had lower power consumption when comparing with the other two types. The performance of the three types of phase detectors is summarized in Tab. 4.4:

Table 4.4: Summarization of the key performance parameters of the three types of phase detectors

Parameter	**Mixer**	**EXOR**	**3-state PFD**
Technology	HBT	CMOS	CMOS
Operation frequency	2 GHz	1 GHz	500 MHz
Phase detection range, rad	$\sim \pi$	π	∞
Phase error gain, V	0.83	1	0.5
Noise at 100 Hz, dBV^2/Hz	-152	–	-132
Noise at 1 MHz, dBV^2/Hz	-157	–	-160
Power consumption, mW	8.9	0.46	3.3

4.3 Voltage Controlled Oscillators

The VCO is another crucial component in PLL designs: the output frequency range of the PLL is defined by the tuning range of the VCO; the tuning gain of the VCO K_{VCO} influences the PLL loop behavior; the phase noise of the free running VCO is the key parameter which determines the out-of-band phase noise of the PLL.

4.3.1 Resonators

The resonator determines the natural frequency of the oscillator. Fig. 4.15 shows a typical RLC resonator in a parallel topology. The resonant frequency is $\omega_0 = 1/\sqrt{LC}$. The unloaded quality factor Q_U can be expressed as (4.8). In practical oscillator designs, the loaded quality factor Q_L is considered, especially for phase noise optimization. Q_L is expressed as (4.9).

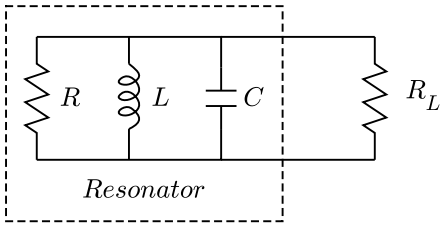


Figure 4.15: RLC resonator circuit in parallel topology

$$Q_U = R\sqrt{\frac{C}{L}} \tag{4.8}$$

$$Q_L = \frac{Q_U}{1 + \frac{R}{R_L}} \tag{4.9}$$

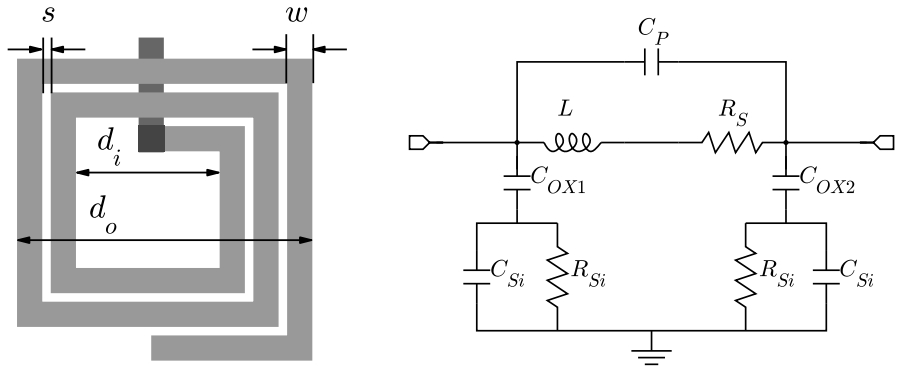
On-chip planar spiral inductors are widely used in monolithic VCO designs at microwave frequencies [37] and even in the millimeter wave range [38]. Fig. 4.16(a) shows the top view of a typical planar spiral inductor. The geometrical parameters of the inductors include the wire width w, the wire spacing s, the outer diameter d_o, the inner diameter d_i and the number of turns n. The inductance can be approximated through formula (4.10), which was described in [39].

$$L = K_1\mu_0\frac{n^2 d_{avg}}{1 + K_2\rho} \tag{4.10}$$

$$\rho = \frac{d_o - d_i}{d_o + d_i} \tag{4.11}$$

$$d_{avg} = \frac{d_o + d_i}{2} \tag{4.12}$$

where K_1 and K_2 are parameters which depend on the geometric shapes of the inductors.



(a) (b)

Figure 4.16: (a) Top view of a planar spiral inductor in square shape (b) Equivalent circuit of the spiral inductor

A conventional method to model the spiral inductors is the measurement-based approach. The model of the on chip planar spiral inductors can be described using an RLC equivalent circuit, as shown in Fig.4.16(b), where L is the inductance of the spiral wire, R_S is the series metal resistance, C_P is the coupling capacitance between the inductor turns, C_{OX1} and C_{OX2} are the capacitances between the metal and the substrate and C_{Si} and R_{Si} are the silicon substrate capacitance and resistance, respectively [40].

Any transmission line with length less than a quarter of λ is an inductor, provided that it is short-circuited at the other end. For millimeter wave applications, shunt inductors with sub-nH values can be implemented using transmission lines, since they are easier to adjust than spiral inductors and have comparable quality factors [41].

4.3.2 Colpitts Oscillator Designs

The most common LC oscillators are classified in the following types: Armstrong oscillator, Clapp oscillator, Hartley oscillator and Colpitts oscillator, among which Hartley and Colpitts topologies are the most commonly used types in integrated circuit designs [42]. The Hartley oscillator uses a tapped inductor together with a capacitor to form the resonator circuit, while a Colpitts type uses two capacitors and one inductor for the resonator. As for MMIC implementations, the Colpitts topology is more popular simply because it needs only one resonator inductor

instead of the complicated tapped inductor design as in Hartley oscillators [43]. The equivalent circuit of the Colpitts oscillator is shown in Fig. 4.17.

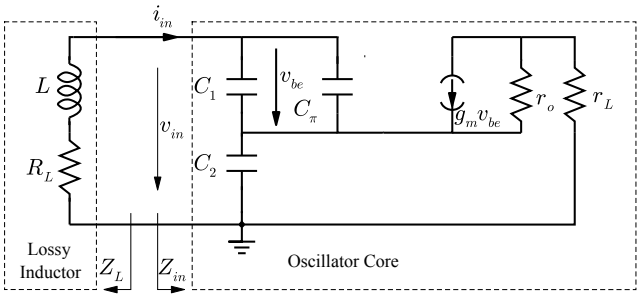


Figure 4.17: Equivalent circuit of the Colpitts oscillator

The input impedance of the oscillator core Z_{in} can be expressed as:

$$Z_{in} = -\frac{g_m}{\omega^2 C_2 C_1'} + \frac{1}{j\omega}\frac{C_1' + C_2}{C_1' C_2} \tag{4.13}$$

where C_1' is the equivalent capacitance of C_1 in parallel with C_π. When a large size transistor is used and C_π is comparable with C_1, C_1 can be omitted in oscillator designs.

An oscillation occurs, if and only if the following conditions are matched:

$$\Re\left(Z_L\right) + \Re\left(Z_{in}\right) < 0 \tag{4.14}$$

$$\Im\left(Z_L\right) + \Im\left(Z_{in}\right) = 0 \tag{4.15}$$

where $\Re\left(Z_L\right)$ and $\Re\left(Z_{in}\right)$ are the real parts of the load and input impendence; and $\Im\left(Z_L\right)$ and $\Im\left(Z_{in}\right)$ are the imaginary parts. As a rule of thumb, to have a fast start up of the oscillation, equation (4.14) can be modified as: [44]

$$1.2\Re\left(Z_L\right) + \Re\left(Z_{in}\right) < 0 \tag{4.16}$$

From (4.13),(4.15) and (4.16), the oscillation condition at startup can be written as:

$$g_m > \frac{1.2R_L(C_1' + C_2)}{L} \tag{4.17}$$

As the amplitude of the oscillation increases, the large signal transconductance G_m decreases till:

$$G_m = \frac{R_L(C_1' + C_2)}{L} \tag{4.18}$$

The oscillation frequency can be expressed as:

$$\omega_0 = \sqrt{\frac{C_1' + C_2}{LC_1'C_2}} \tag{4.19}$$

The simplified schematic of the differential Colpitts oscillator is shown in Fig. 4.18. L_B is the resonator inductor, C_1, C_2 and Q_1, Q_2 form the oscillator core. L_E at the emitters of Q_1, Q_2 implements DC feeding. Instead of using a resistive load, an inductive load L_C is used at the output stage to reduce power consumption. The frequency is tuned by varactor C_2. The oscillation frequency is now modified as:

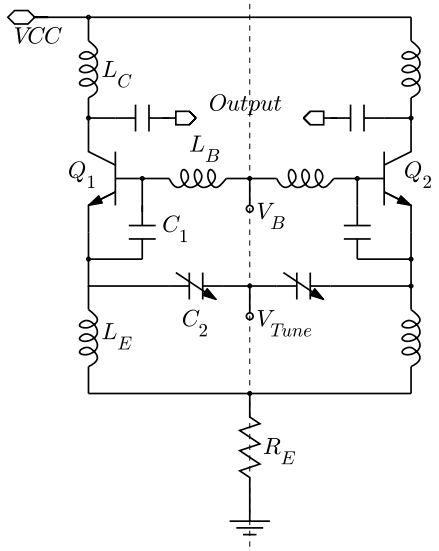
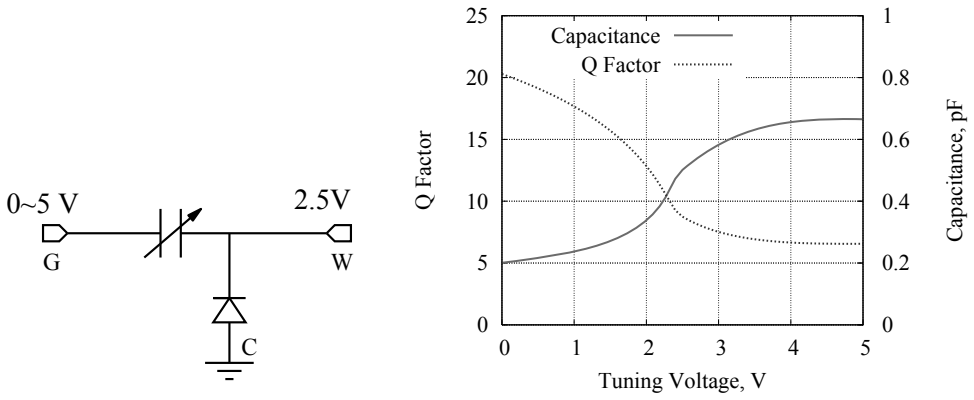


Figure 4.18: Simplified schematic of the differential Colpitts oscillator

$$\omega_0 \approx \sqrt{\frac{C_1' + C_2}{L_B C_1' C_2} + \frac{1}{2L_E C_2}} \tag{4.20}$$

Fig. 4.19(a) shows the bias conditions of the varicap: the charge extraction port "C" is connected to ground; the well contacts "W" have a constant voltage which is biased at 2.5 V in the schematic; and the tuning voltage is applied at the poly silicon gate "G". The tuning characteristics of the varactor is shown in Fig. 4.19(b). The maximum capacitance $C_{2,max}$ to minimum capacitance $C_{2,min}$ ratio is around 3.3; the quality factor is 20 at $V_G = 0$ V and reduces to 7 at $V_G = 5$ V.

The phase noise is probably the most critical parameter in oscillator designs, which describes directly the signal quality of an oscillator. One of the most popular formulas describing the phase noise in oscillators was introduced by D. B. Leeson [45]:



(a) (b)

Figure 4.19: (a) MOS varicap from IHP 0.25 µm SiGe SG25H3, size 3×10 (b) tuning characteristics at 20 GHz, V_C= 0 V and V_W = 2.5 V

$$L(\Delta\omega) = \frac{2FkTB}{P_S}\left[1+\left(\frac{\omega_0}{2\Delta\omega Q_L}\right)^2\right]\left(1+\frac{2\pi f_c}{|\Delta\omega|}\right) \tag{4.21}$$

where $\Delta\omega$ = offset frequency (Hz)

F = open loop noise factor of the active devices

k = Boltzmann constant

T = Temperature (K)

B = measurement bandwidth (Hz)

P_S = signal power (W)

ω_0 = oscillator center frequency (Hz)

Q_L = loaded resonator quality factor

f_c = corner frequency of the flicker noise in active devices (Hz)

At low frequency offset, which is below the corner frequency of the flicker noise caused by the active devices in the oscillator core (for example, Q_1 and Q_2 in Fig. 4.18), the phase noise can be simplified as:

$$L(\Delta\omega) = \frac{2FkTB}{P_S}\cdot\frac{\pi{\omega_0}^2 f_c}{|\Delta\omega|^3 Q_L^2} \tag{4.22}$$

At a frequency offset above the corner frequency of the flicker noise but below the corner frequency of the phase noise, the phase noise can be simplified as:

$$L(\Delta\omega) = \frac{FkTB}{2P_S}\left(\frac{\omega_0}{\Delta\omega Q_L}\right)^2 \tag{4.23}$$

The noise floor can be expressed as:

$$L(\Delta\omega) = \frac{2FkTB}{P_S} \tag{4.24}$$

which is determined by the signal power and the noise factor of the active devices.

The influence of the flicker noise from the HBTs of the oscillator core is shown in Fig. 4.20, inducing a -30 dB/decade slope below the 30 kHz corner frequency. The phase noise of the VCO at lower frequency offsets will be suppressed by the loop filter of the PLL. In this work, the PLL loop bandwidth is designed beyond 10 MHz, therefore the flicker noise of the HBTs is not critical for the VCO designs.

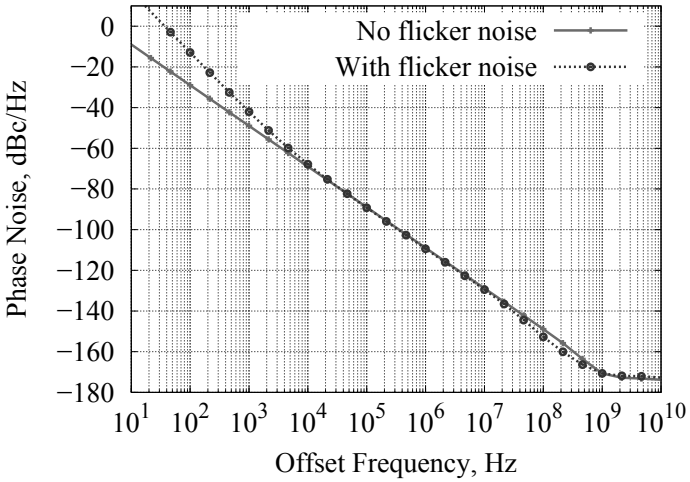


Figure 4.20: Simulated phase noise of the oscillator for HBT models without and with flicker noise at a center frequency $f_c = 17.5$ GHz

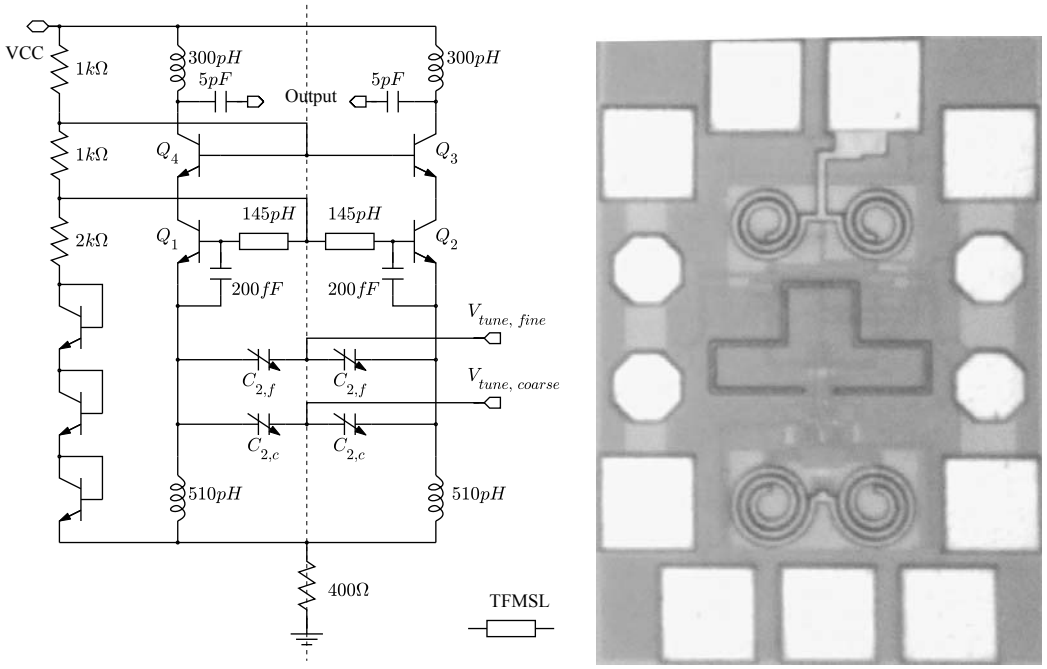
The unloaded Q factor of the resonator mainly depends on the Q factors of the resonator inductor L, capacitor C_2 and C_1' as shown in Fig. 4.17. The Q factor of the on-chip inductors is limited to below 15 in the frequency range from 15 to 40 GHz [46][47]. Besides the optimum combination of the dimension parameters of the inductors in 4.16(a), several other techniques were used to improve the Q factor of the on-chip inductors, such as metal layer shunting, spiral coils stacking, substrate shielding, inner coils tapering and so on [48][49]. Off chip inductors such as bond wires offer a much higher Q factor (typically around 50 at microwave frequencies) than the on chip inductors and are also used for VCO resonator designs [50]. However, small bond wire inductors at hundreds of pH are very sensitive to the production fluctuations.

One way to improve the Q factor of C_1' is to choose a larger capacitance of C_1 with a higher Q factor to compensate the poor Q factor of C_π. The Q factor

of C_2, which is in most cases a varactor in VCO designs, is limited as shown in Fig. 4.19(b). However, this can be compensated by applying a parallel MIM capacitor with a higher Q factor, under the penalty of a narrowed tuning range.

4.3.3 A 35 GHz VCO

Fig. 4.21(a) shows the schematic of a 35 GHz Colpitts VCO. The design is a modified version based on the VCO described in [51]. As was discussed in Chapter 2, the reference spurious level can be decreased by reducing the VCO gain. In this work, to reduce the VCO gain, only part of the varactors are tuned by the PLL through a fine tuning port; the rest are controlled externally through a coarse tuning port. The cascode transistors (Q_3, Q_4) work as an output buffer stage to boost the VCO output power.



(a) (b)

Figure 4.21: (a) Schematic and (b) Chip micrograph (300 μm × 180 μm exclusive pads) of the 35 GHz differential Colpitts VCO with thin-film microstrip line as the resonator inductor, $C_{2,f}$ = Varicap 1×4, $C_{2,c}$ = Varicap 2×6, Q_{1-4} = shp×4, (shp: high performance transistor, see Tab. 4.1)

The resonator inductors are realized using Thin Film Microstrip Lines (TFMSL). The characteristic of the inductors is shown in Fig. 4.22. The inductance is around 145 pH at 35 GHz. C_1 was set to 200 fF. The fine tuning varactor varies from 27 fF to 90 fF; the coarse tuning one varies from 81 fF to 270 fF. The load inductors

L_C and degeneration inductors L_E were realized using planar spiral inductors with inductance of 300 pH and 510 pH.

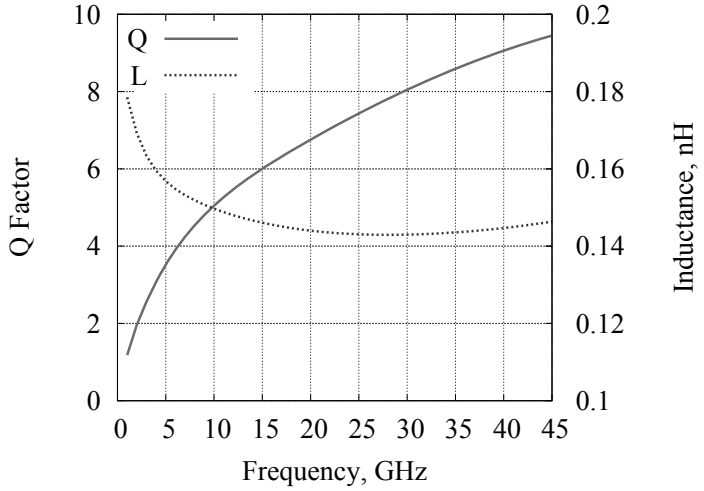
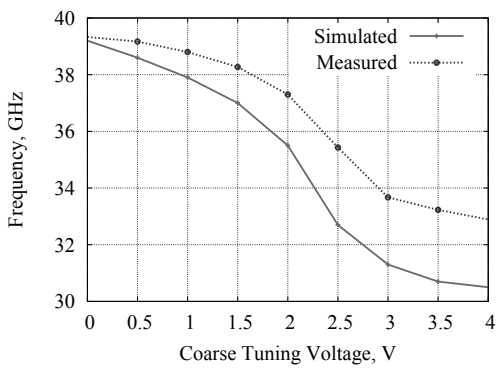
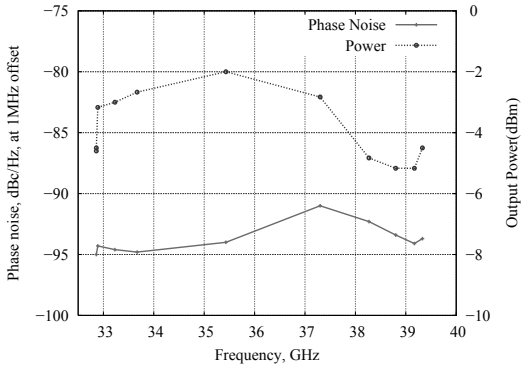


Figure 4.22: Characteristics of the TFMSL as resonator inductor using top mental layer 2, length= 260 µm, width = 3 µm

Fig. 4.23(a) shows the measured coarse tuning characteristics at a fine tuning voltage of 0 V. The tuning range is from 32.8 GHz to 39.33 GHz. The measured phase noise and output power is shown in Fig. 4.23(b). Comparing with the simulated results, the measured oscillator frequency at $V_{tune,coarse}$ = 2 V is around 2 GHz higher; the measured frequency tuning ranged is around 2 GHz lower. The phase noise is below -90 dBc/Hz at 1 MHz offset frequency over the complete frequency range. The single ended output power is around -3 dBm.



(a)



(b)

Figure 4.23: (a)Simulated and measured tuning characteristics of the 35 GHz VCO at 0 V fine tuning voltage (b) Measured output power and phase noise of the VCO at 1 MHz offset frequency

The VCO power consumption is 37 mW at 5 V supply. The chip micrograph is shown in Fig. 4.21(b) with a chip area of 300 μm × 180 μm exclusive pads.

4.3.4 A Dual-Core VCO

Conventional designs use multiple VCOs and switch between them to further increase the frequency tuning range, under the penalty of increased chip area [52]. The emerging RF-MEMS technologies make multi-band VCO design in millimeter wave range feasible by switching the resonator parameters, for example as discussed in [53]. However, even today, RF-MEMS do not have the maturity required for commercial products because of reliability issues and extremely large chip area consumption. Compared with RF-MEMS switches, the CMOS switches are more practical for reconfigurable circuit designs at microwave frequency range. In this work, a switchable dual-core VCO is designed using RF CMOS switches, which achieves a tuning range of 40% centered at 20 GHz.

The schematic of the dual-core VCO is shown in Fig. 4.24. The VCO is based on a modified differential Colpitts oscillator as discussed in 4.3.3. For example, the VCO $Core_1$ is formed by Q_1, Q_2, L_B, C_B, $C_{v,f}$ and $C_{v,c}$. The two VCO cores are controlled by RF CMOS switches S_1-S_4. The size of the CMOS switches is optimized to L = 240 nm and W = 120 μm after the trade-off between the on-resistance and the off-capacitances. The switches are placed outside of the resonator cores, so that the degradation of the resonator Q factor by the parasitics of the switches is negligible. The two resonator cores share the emitter degeneration inductors and the collector load inductors, which effectively reduces the chip area. When switches S_1 and S_2 are turned on and S_3, S_4 are turned off, DC current is supplied only to Q_1, Q_2 and stimulates the oscillation; meanwhile Q_3, Q_4 are switched off with a negligible DC leakage current of less than 1 μA flowing through. Cascode output buffers are used after Q_1-Q_4.

Table 4.5: Parameters of the key components of the dual-core VCO

Parameter	Value	Parameter	Value
L_B	270 pH	L'_B	230 pH
C_B	300 fF	C'_B	200 fF
$C^*_{v,f}$	276 fF	$C'^*_{v,f}$	184 fF
$C^*_{v,c}$	644 fF	$C'^*_{v,c}$	414 fF
L_E	540 pH	L_C	430 pH

*maximum capacitance at V_{GW} = 2.5 V

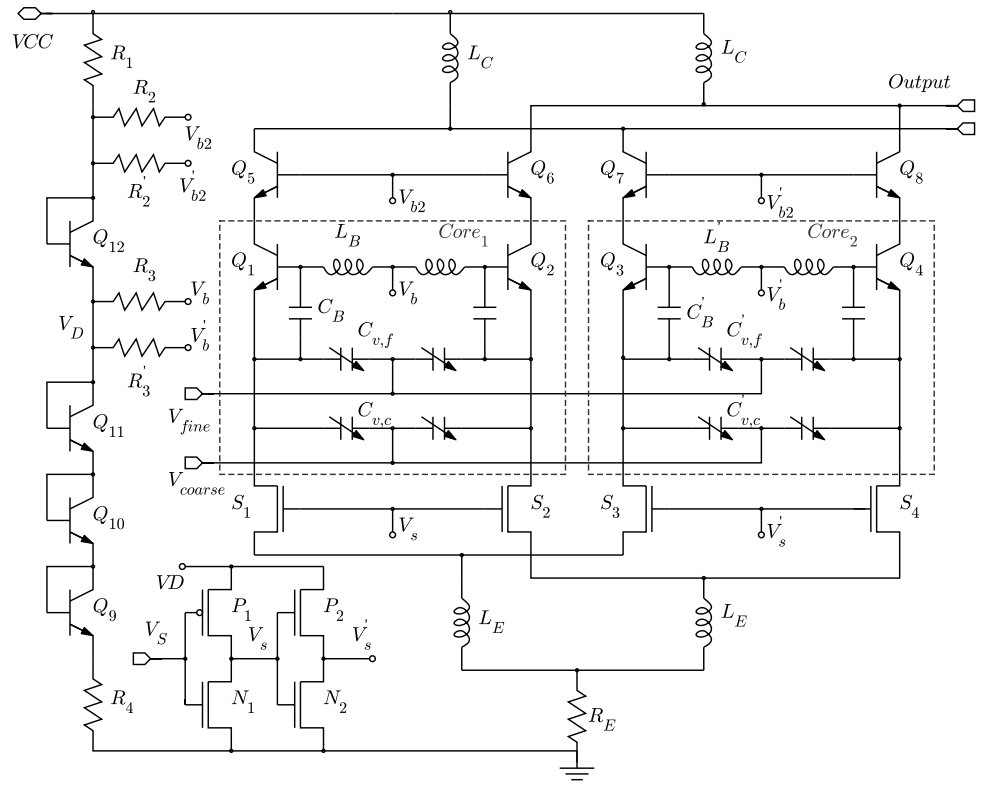


Figure 4.24: Schematic of the dual-core wide tuning range VCO

The inductors are realized using the topmost aluminum layer with a thickness of 3 μm. Spiral type inductors with tapered line width are designed as shown in Fig. 4.25. The substrate loss tends to increase with increased line width. Due to Eddy currents, the magnetically induced substrate loss is mainly in the center of the spiral inductors, narrowed line widths in the inner turns are preferred. The ohmic loss is predominantly in the outer turns, where wider line widths are preferred [54]. In this work, the inductor designs are assisted by the EM simulation tool ADS Momentum. Fig. 4.26 compares the inductor performance between the EM simulation using Momentum and the measurement results. The inductance is 270 pH and the Q factor is around 11 at 20 GHz. The EM simulation results match well with the measurement results.

The chip area is only 280 μm × 370 μm without pads. The voltage supply of the VCO is 5 V with a current consumption of 12 mA. Fig. 4.27 shows the measured frequency tuning characteristics of the dual-core VCO. The VCO can be tuned from 15.9 to 23.9 GHz with a coarse tuning voltage from 0 to 5 V and a fine tuning voltage from 0 to 3 V. The phase noise is measured using the Phase Noise Utility of the spectrum analyzer Agilent 8565E. Fig. 4.28 shows the measured phase noise of the dual-core VCO at 1 MHz offset frequency. At 15.9 GHz, the phase noise

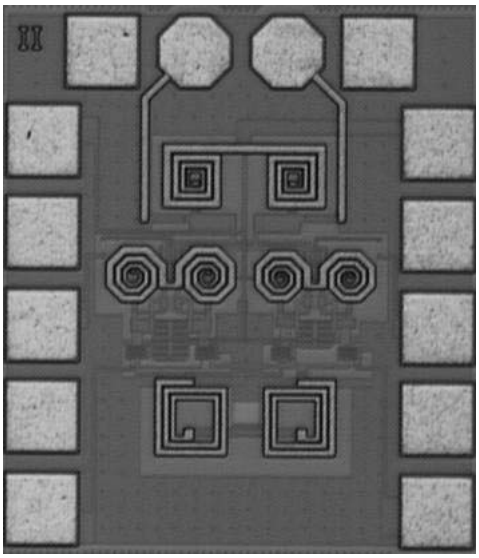
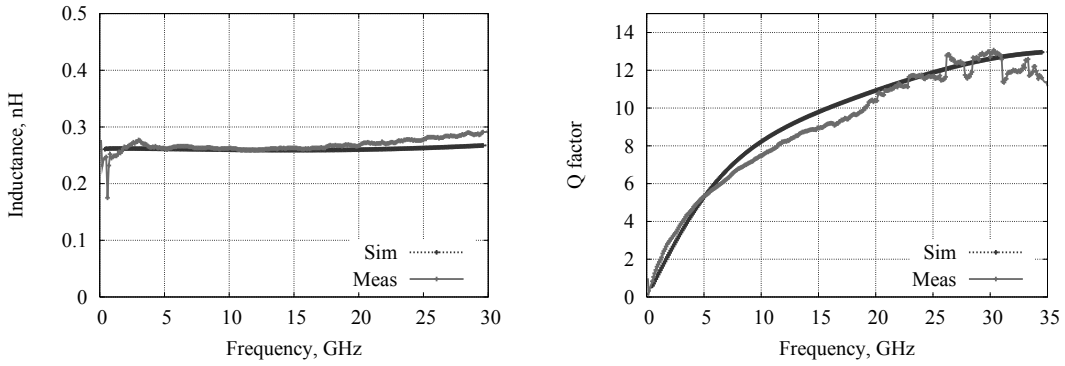


Figure 4.25: Chip micrograph of the dual-core wide tuning range VCO, 280 µm × 370 µm exclusive pads



(a) (b)

Figure 4.26: Comparisons of the EM simulated (ADS Momentum) inductor performance with the measurement results (a) Inductance (b) Q factor

at 1 MHz offset is around -108 dBc/Hz and at 23.9 GHz around -104 dBc/Hz. The output power is around 2 dBm at 15.9 GHz and decreases slightly to around -3 dBm at 23.9 GHz; the VCO output power over the complete tuning range is sufficient to drive the divider of the PLL and the de-/modulators. Table 4.6 lists the comparison of this work with previous publications.

4.3.5 Summary

In this section, the Colpitts type of oscillator was discussed, in terms of phase noise optimization, power consumption and chip area reduction. A 35 GHz VCO

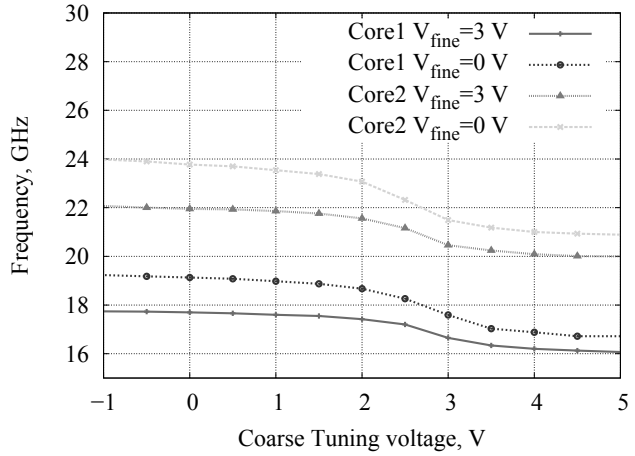


Figure 4.27: Frequency tuning characteristics of the dual-core VCO

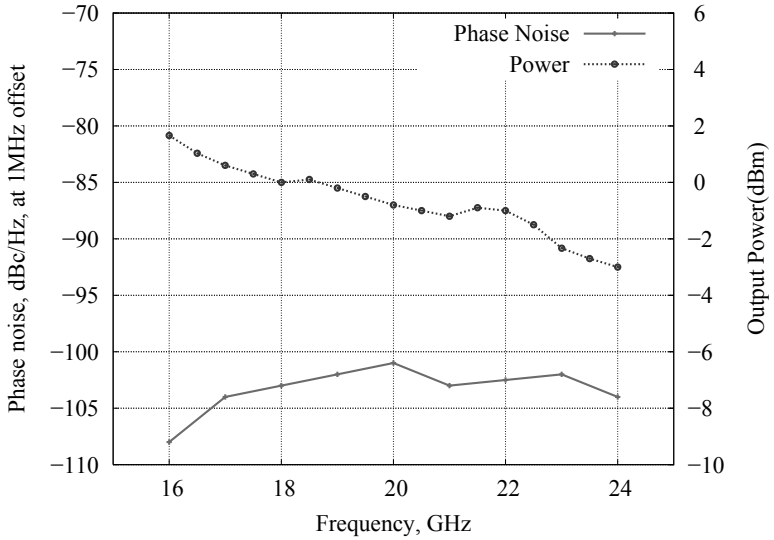


Figure 4.28: Measured phase noise and output power of the dual-core VCO

was designed with a tuning range of 18% and phase noise of below -90 dBc/Hz at 1 MHz offset frequency over the complete frequency range. A dual-core VCO achieved a tuning range of 40% with a decent phase noise of below -100 dBc/Hz at 1 MHz offset frequency; using switched resonator cores and shared DC feeding and output loading inductors, the chip area was minimized down to 0.1 mm^2.

Table 4.6: Measured VCO performance compared with prior published work

Parameter	[55]	[56]	[57]	This work
Technology	0.25 µm BiCMOS	0.13 µm CMOS	0.18 µm CMOS	0.25 µm BiCMOS
f_0(GHz)	20	26	23	20
Tuning range	2%	23.6%	16.5%	40%
Phase noise dBc/Hz@ 1MHz	-106	-92.6	-98	-104
Chip area (mm^2)	0.2*	0.12*	0.56**	0.1*/0.3**
Power (mW)	22.3	43	9	60

* Without pads ** With pads

4.4 Frequency Dividers

In a PLL, frequency dividers are used to adjust the frequencies of the VCO and sometimes the reference signal to the comparison frequency. In other words, the VCO frequency can be synthesized by multiplying the reference signal by the frequency divider ratios.

In RF and millimeter wave ranges, static frequency dividers and dynamic ones are probably the most popular types. Theoretically, the static divider can divide the signal down to arbitrarily low frequencies, since the latches are able to hold the signal levels for an arbitrarily long period [58]. The frequency range of the dynamic divider is determined by the frequency response of the open loop [59]. Typically, the dynamic types have higher operating frequency than static ones. Another type of frequency divider which is called injection locked frequency divider, has been reported since the last decade [60][61]. It works similar to an injection locked oscillator with an even higher operating frequency than the dynamic types. However, its frequency range is narrower than for static and dynamic dividers [62].

4.4.1 Static Frequency Dividers

The static frequency dividers can be realized using edge triggered D flip-flops where the Q-output is inversely fed back to the D-input as shown in Fig. 4.29. The maximum operating frequency is determined by the speed of the D-latches. The D-latch is implemented using the *high performance* HBT type from the SG25H3 technology (see Tab. 4.1) with a peak $f_T = 120$ GHz at a collector current density $J_C = 6$ mA/µm^2. The simplified schematic of the D-latch is shown in Fig. 4.30. The minimum transistor size is applied to reduce the current consumption.

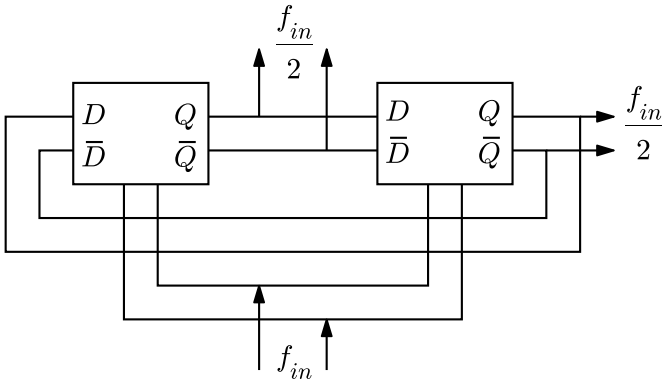


Figure 4.29: Block diagram of a static frequency divider

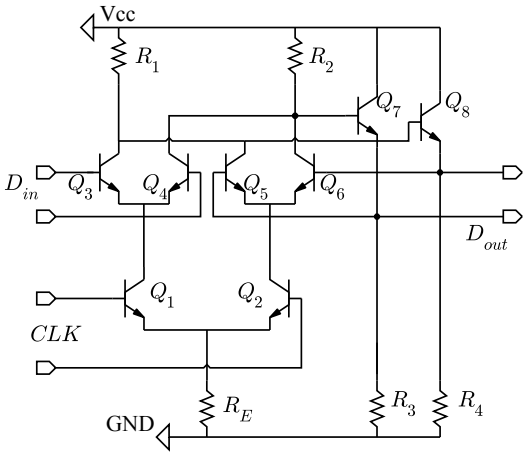


Figure 4.30: Simplified schematic of a D-latch using HBTs

Such a static frequency divider can self-oscillate, with the oscillation frequency indicating the operating speed of the divider. Fig. 4.31(a) shows the self oscillation frequency versus the biasing current. The maximum self oscillation frequency is achieved where the current consumption is 18 mA at V_{CC} = 3.3 V. The input sensitivity of a frequency divider is the required minimum input power. Fig. 4.31(b) shows the simulated divider input sensitivity with a self-oscillation frequency of 17.8 GHz; more input power is required when the output frequency shifts away from the self-oscillation frequency.

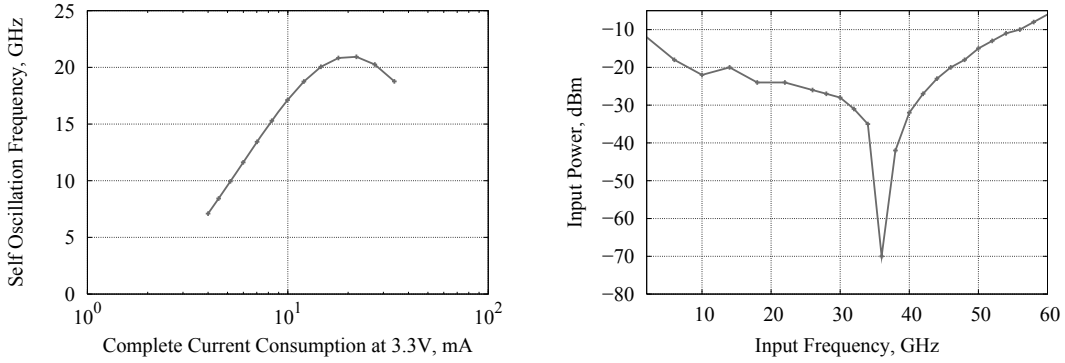


Figure 4.31: (a) Self oscillation frequency versus power supply (b) Input sensitivity of a static frequency divider versus input frequency

In most cases, the phase noise of the frequency divider is relatively low compared with other blocks in PLLs. The intrinsic phase noise at low frequency offset (below 10 MHz) of the static frequency divider is independent from the operating frequency, because the phase noise is mainly contributed by the flicker noise of the

transistors. A similar behavior was also observed from the low frequency noise of a mixer type phase detector, see Section 4.2.1. The phase noise of the frequency divider versus the input power level is shown in Fig. 4.32.

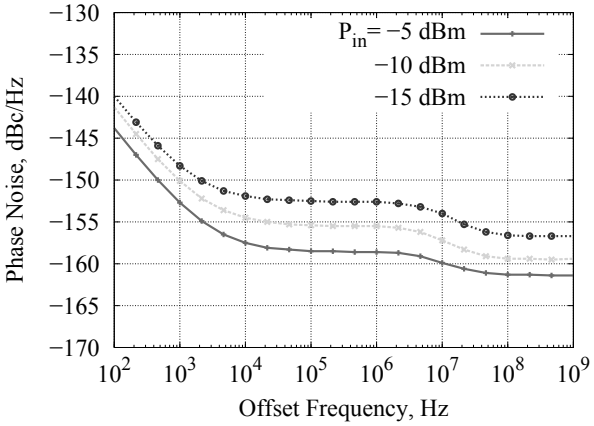


Figure 4.32: Simulated phase noise of the static frequency divider at 2 GHz input frequency, at input power P_{in} = -15 dBm, -10 dBm and -5 dBm

In the dual-loop PLL in this work, quadrature signals are required for the two different types of phase detectors. Quadrature signals can be generated from a ÷2 static divider as shown in Fig. 4.29 if the input periodic signal has a 50% duty cycle. Using 2 static ÷2 dividers as shown in Fig. 4.33, the quadrature signals can be generated independent from the duty cycle of the input signals.

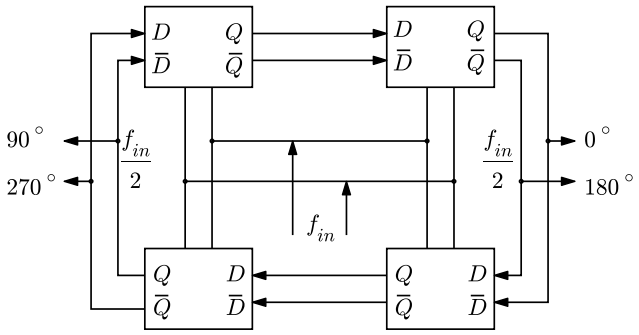


Figure 4.33: Block diagram of a static ÷4 frequency divider for quadrature signals generation

4.4.2 Dynamic Frequency Dividers

The dynamic frequency divider, which is also called Miller frequency divider, was introduced by R. L. Miller[63]. The block diagram is shown in Fig. 4.34, which combines a mixer, a low pass filter and an amplifier. The sum frequency $f_{in} + f_{out}$

in the output of the mixer is suppressed and the difference frequency $f_{in} - f_{out}$ in the output is then amplified and fed back to one of the mixer inputs. In this case, the difference frequency is exactly half of the excitation signal frequency.

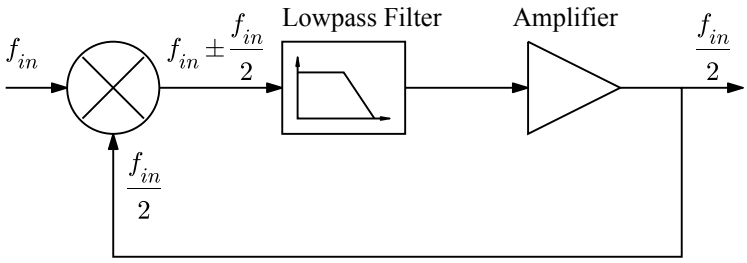


Figure 4.34: Block diagram of a dynamic ÷2 frequency divider

The simplified schematic of the dynamic frequency divider is shown in Fig. 4.35, where a Gilbert cell is used as the mixer. The smallest transistors were used in the Gilbert cell, so that the least current is required to achieve the fastest speed. The collector current of the emitter coupled pair is biased at 1 mA, which is half the current at which f_T peaks. The low pass filter is realized by the inherent low pass effect of the mixing core and the emitter followers. Three emitter follower stages work as level shifters and output buffers. The transistors in the first two emitter follower stages are biased at 500 μA. The current in the output stage is biased at 2.2 mA.

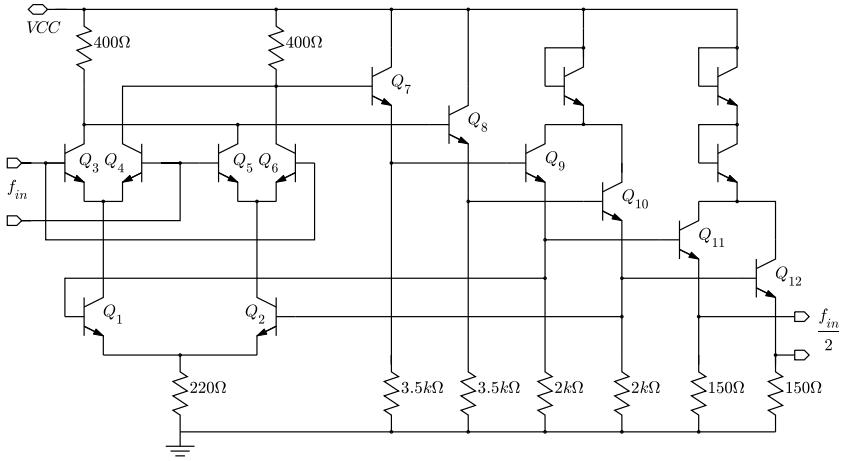
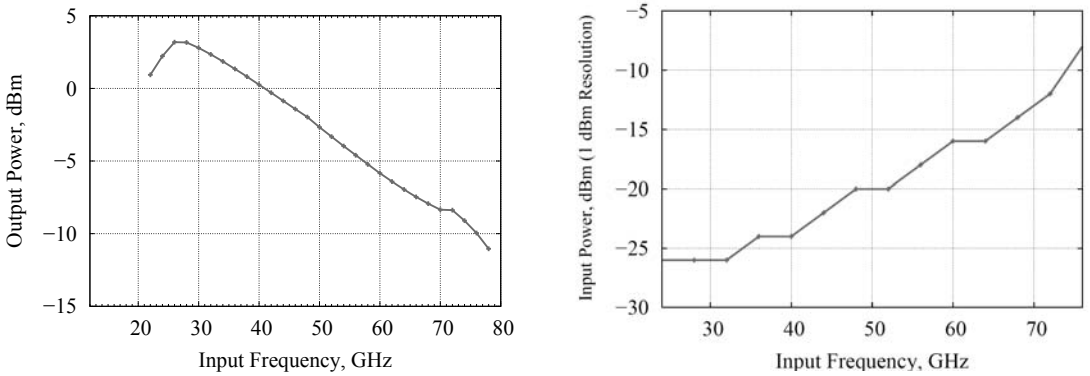


Figure 4.35: Simplified schematic of dynamic ÷2 frequency divider, Q_{1-12} = H3shp1 (high performance HBT, see Tab. 4.1).

The maximum operating frequency of the dynamic dividers is higher than the static ones [64][65]. The maximum operating frequency is reached when the open

loop gain goes below 0 dB at $f_{in}/2$; the lower frequency limit is reached when the open loop gain goes above 0 dB at $3f_{in}/2$.

Fig. 4.36(a) shows the simulated output power of the divider versus the input frequency at -3 dBm input power. The input operating frequency range is 22 to 78 GHz. Fig. 4.36(b) shows the input sensitivity of the dynamic divider. With increasing input frequency, it requires more power for the input signal.



(a) (b)

Figure 4.36: (a) Simulated output power versus the input frequency for P_{in} = -3 dBm; (b) Simulated input sensitivity of the dynamic ÷2 frequency divider

Fig. 4.37 shows the simulated output phase noise of the dynamic frequency divider at 30, 50 and 70 GHz input frequency with the same input power level of -3 dBm. At 32 GHz, the output phase noise has a corner frequency of around 200 kHz, with a noise floor of -157 dBc/Hz. In this design, the dynamic frequency dividers are used in the front of the multi-stage frequency dividers when the static frequency divider fails at operation due to the speed limit. When comparing the phase noise behavior with the static frequency divider as shown in Fig. 4.32, for a 32 GHz input signal, after the 4-stage frequency dividing, the phase noise of the dynamic divider will be much lower than the noise level of the static ones. Therefore, the phase noise of the dynamic frequency divider in this design can be neglected.

The DC bias point of the input port was set to 2.5 V. The complete power consumption of the dynamic divider is 8.7 mA at 3.3 V supply.

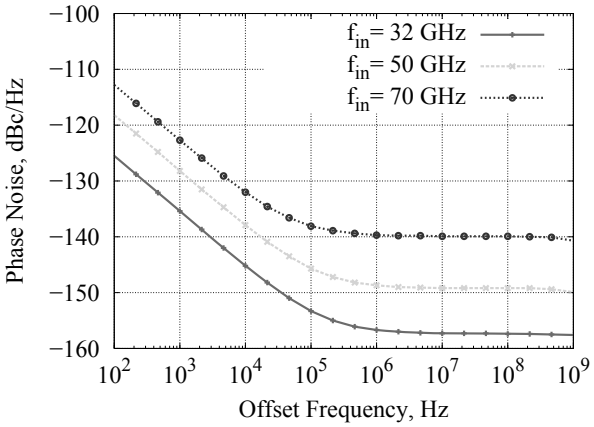


Figure 4.37: Simulated phase noise of the dynamic frequency divider at input power P_{in} = -3 dBm and different input frequencies: 32, 50 and 70 GHz.

4.4.3 Prescalers for PLL

4.4.3.1 Prescalers for a 35 GHz PLL

In this work, a 6-stage frequency divider was designed for a 35 GHz PLL similar to the one shown in [51]. The first stage is a dynamic frequency divider and the remaining stages are designed with static frequency dividers as shown in Fig. 4.38.

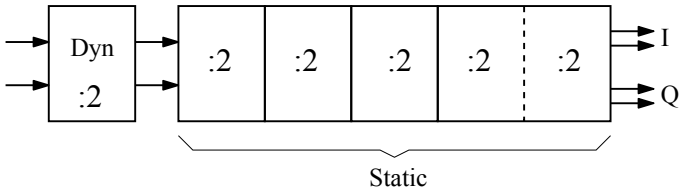


Figure 4.38: Block diagram of the divide-by-64 frequency divider

The dynamic divider is the one described in Section 4.4.2. Since the operating frequency reduces to half after each divider stage, the power consumption of each static stage is optimized according Fig. 4.31(a). To generate an IQ output for the dual-loop PLL, the last two static stages were designed as a ÷4 divider as discussed in Section 4.4.1. The power consumption of each divider stage is listed in Tab. 4.7.

Table 4.7: Power consumption of each divider stage with output buffers

Divider@3.3V	Dynamic	Static 1	Static 2	Static 3	Static 4,5
Current, mA	8.7	9.5	7	5.6	4.5

In the multi-stage frequency divider designs, the phase noise of the input signal

is improved by $20 \cdot \log 2$ dB after each divide-by-2 stage. Since the phase noise of the static frequency divider at low offset frequency is independent of the operating frequency, the last divider stage dominates the phase noise of the multi-stage frequency dividers.

4.4.3.2 Prescalers for a 16-24 GHz Frequency Synthesizer

The prescaler for a 16-24 GHz frequency synthesizer (see Section 6.2) combines a static ÷4 frequency divider and a multi-modulus programmable frequency divider as shown in Fig. 4.39. The multi-modulus divider includes 4 stages of 2/3 dual-modulus cells based on the one shown in [66]. The frequency divider ratio is set by the program ports "p" which vary from 2^4 to $2^{4+1} - 1$. In fractional-N frequency synthesizer designs, the programmable ports "p" can be controlled by a $\Sigma\Delta$ modulator to achieve even finer frequency resolutions [67][68].

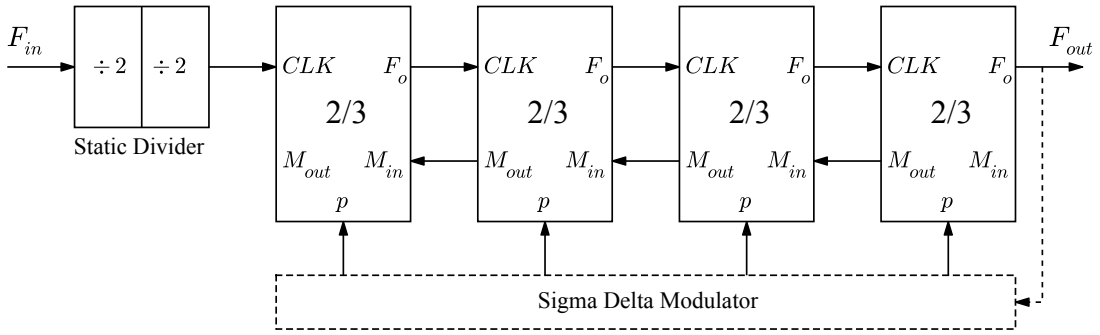


Figure 4.39: Block diagram of the prescaler for the 16 to 24 GHz frequency synthesizer

The simplified block diagram of the 2/3 unit is shown in Fig. 4.40. It combines three "D-Flip-Flop+NAND" units and one D-Flip-Flop similar to the one described in Fig. 4.29. The clock signals are driven by the input signals. The outputs of the D-Flip-Flops feed back to one of the "D" ports one after another. The divider ratio is switchable between 2 and 3 by port "p". The mode in port "M_{in}" catches the feed back from the other 2/3 units.

The schematic of the "D-Flip-Flop+NAND" cell is shown in Fig. 4.41. The NAND unit is implemented using an emitter coupled pair $Q_{7,8}$ at the collector port of Q_3. Transistor Q_9 is inserted at the collector port of Q_4 for level shifting. All the transistors were optimized to the minimum sizes to save power.

The bias point of the clock input is set to 1.5 V. The power consumption of the "D-Flip-Flop+NAND" is 3 mA at 3.3 V.

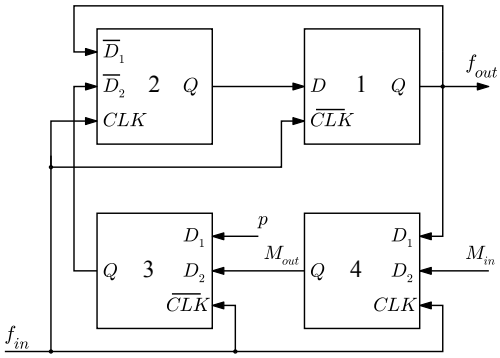


Figure 4.40: Block diagram of the ÷2/3 cell

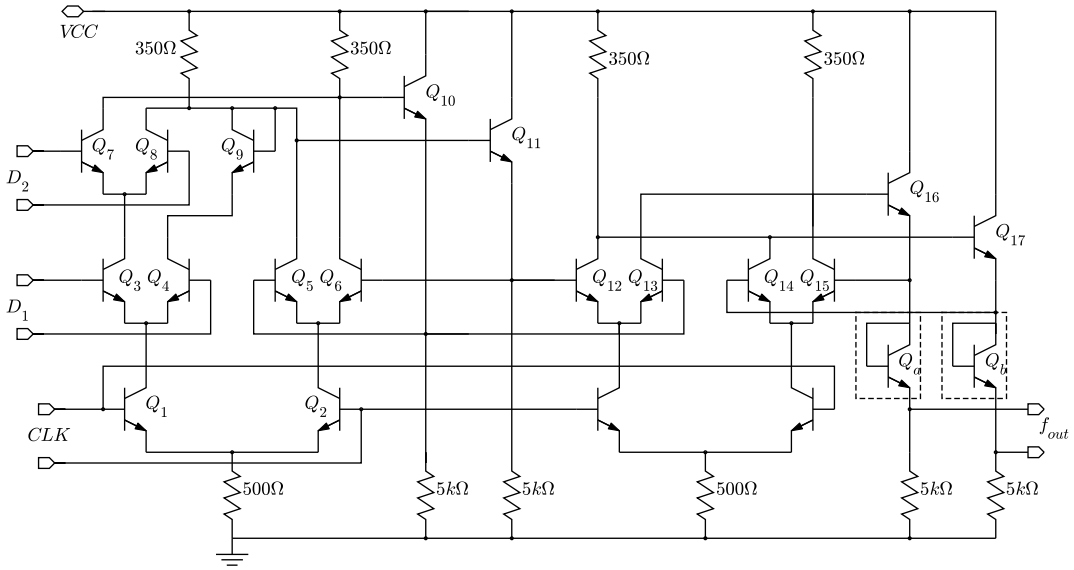


Figure 4.41: Schematic of the "D-Flip-Flop+NAND" cell, Q_{1-17} = H3shp1 (shp: high performance HBT, see Tab. 4.1)

The complete power consumption of the programmable divider is 50 mA at 3.3 V supply. The chip micrograph is shown in Fig. 4.42 with a chip area of 670×270 μm^2 exclusive pads.

The programmable frequency divider is fully characterized with a maximum operating frequency of 7 GHz. Fig. 4.43 shows the output waveforms at a divider ratio set from 16 to 31 at an input frequency of 5 GHz and input power of -5 dBm.

The divider ratio of the prescaler is tunable from 64 to 124 in steps of 4 after combining the static ÷4 divider. The maximum operating frequency is up to 28 GHz, which fits well for the 16-24 GHz frequency synthesizer design. The complete power consumption of the prescaler is 71 mA at 3.3 V supply. Table 4.8 lists the power consumption of each divider block.

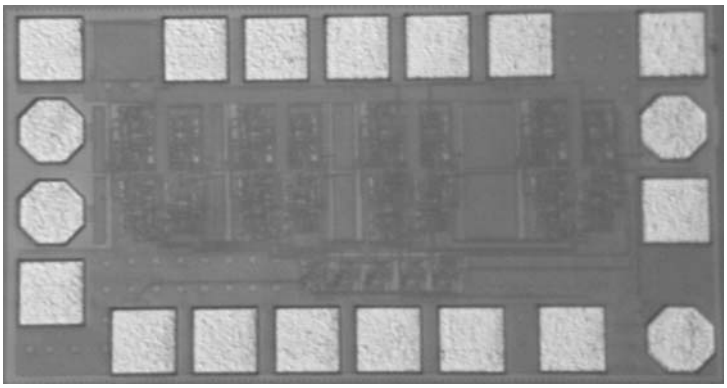


Figure 4.42: Chip micrograph of the programmable frequency divider by 16-31, 670×270 μm^2 exclusive pads

Table 4.8: Power consumption of each divider stage with output buffers

Prescaler@3.3V	1_{st} Static	2_{nd} Static 2	Programmable
Current, mA	13	8	50

4.4.4 Multi-Ratio Frequency Dividers

The multi-ratio frequency divider was used in a 3 to 5 GHz reconfigurable receiver (see Section 6.3). The dividers are used to expand the LO frequency range after generated by the 16 to 24 GHz frequency synthesizer. The circuit block diagram of the multi-ratio frequency dividers is shown in Fig. 4.47. The design includes a static ÷2 frequency divider, a semi-dynamic ÷1.5/3 frequency divider, a 2-bit multiplexer and a static ÷4 frequency divider at the output for the quadrature signal generation.

As shown in Fig. 4.44, the semi-dynamic frequency divider is based on the principle of a dynamic frequency divider [69]. Instead of feeding directly the difference frequency from the mixer output back to its input, a $\div 2^N$ divider is inserted in between. In this case, a frequency divide ratio of $2^N + 1$ and $(2^N + 1)/2^N$ can be achieved simultaneously. However, when the divider ratio 2^N gets higher, the sum and difference frequency at the mixer output becomes closer; a low pass filter with steeper roll-off is required to suppress the sum frequency. In this work, a divide-by-1.5/3 frequency divider was designed.

Fig. 4.45 shows the simplified schematic of the ÷1.5/3 frequency divider. It is similar to the one described in Fig. 4.35, which includes a Gilbert mixer and 2 emitter follower stages. The divide-by-2 block was realized using a static frequency divider, because of its wider operating frequency range than a dynamic one.

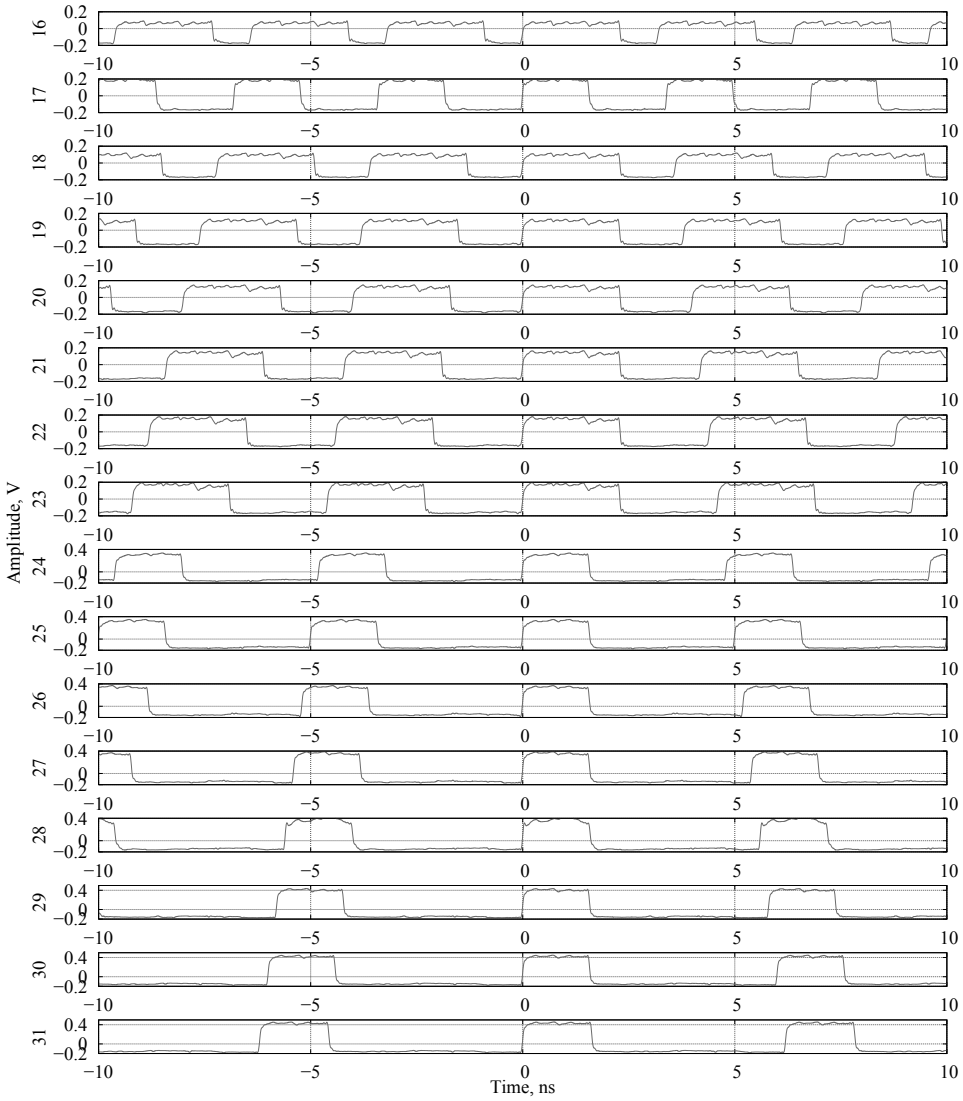


Figure 4.43: Measured output waveforms of the programmable frequency divider with divider ratio sweep from 16 to 31 by integer, f_{in} = 5 GHz, P_{in} = -5 dBm.

Fig. 4.46 shows the simulated input sensitivity of this frequency divider. The self oscillation frequency of the static divider is 15 GHz. The maximum operation frequency is 57 GHz, which is limited by the static frequency divider, while the minimum operation frequency is limited to 12 GHz by the dynamic frequency divider.

The multiplexer was realized using high speed differential ECL circuits [70]. The complete design generates multiple frequency divider ratios 4, 6, 8 and 12. The quadrature LO generation is essential for direct conversion transceivers [71]. The use of the ÷4 divider will generate accurate quadrature signals instead of using

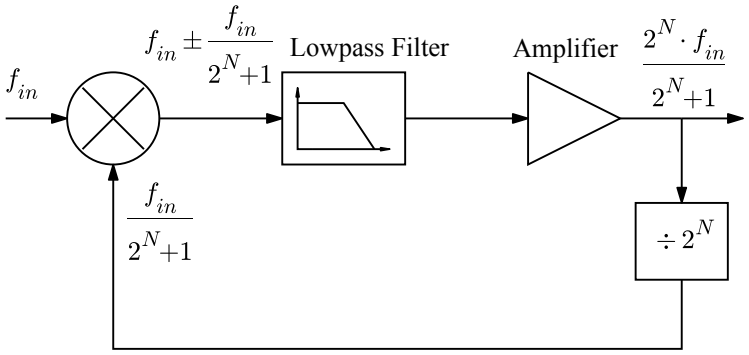


Figure 4.44: Block diagram of a semi-dynamic frequency divider

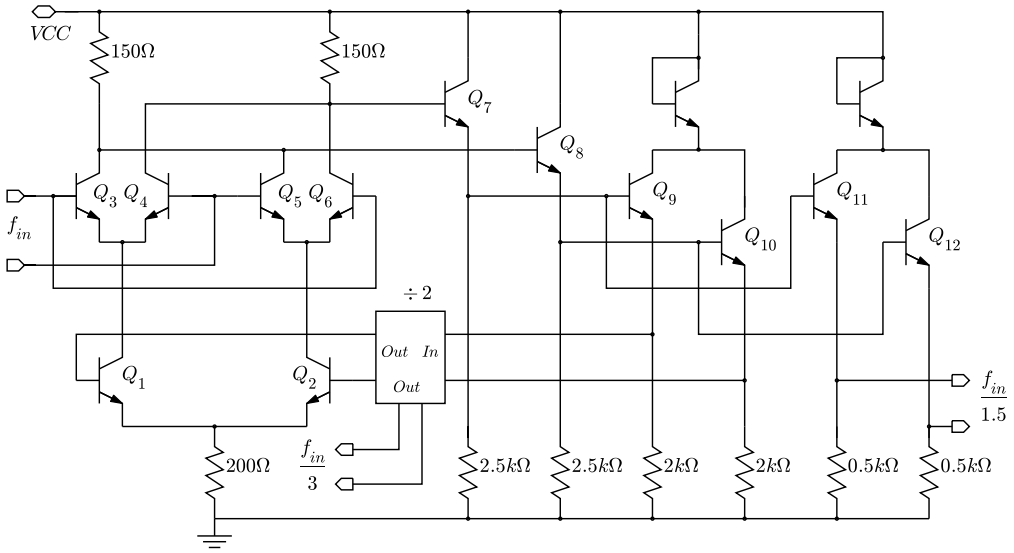


Figure 4.45: Simplified schematics of the ÷1.5/3 dynamic frequency divider, Q_{1-6} = H3shp2, Q_{7-10} = H3shp8, Q_{11-12} = H3shp4, (high performance HBT, see Tab. 4.1).

the bulky and lossy poly-phase shifters.

The chip micrograph is shown in Fig. 4.48, with a chip area of around 500×550 μm^2. Since this is a test chip for the complete receiver integration, only the single ended quadrature outputs $I+$ and $Q+$ are connected to the pads to save chip area. The divider ratio is switched using a 2-bit decoder.

The on-wafer measurement was done on a probe station; the output is measured using the spectrum analyzer Agilent 8565E. Fig. 4.49(a) shows the minimum required input power for the dividers operating in the frequency range from 10 to 32 GHz. The output power of the 16 to 24 GHz VCO is above -3 dBm (see Section 4.3.4), which is high enough to drive the multi-ratio frequency dividers.

Fig. 4.49(b) shows the output power of the multi-ratio divider in different out-

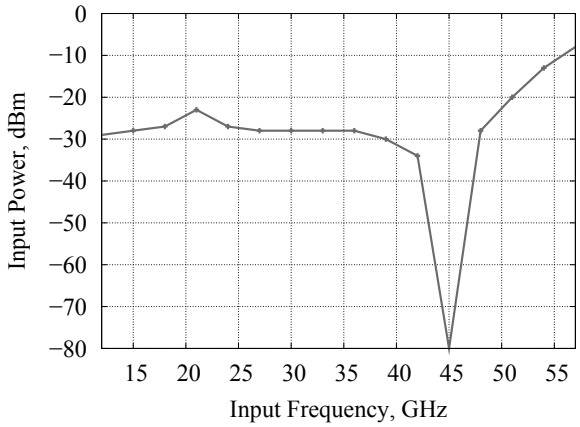


Figure 4.46: Sensitivity of the ÷1.5/3 dynamic frequency divider

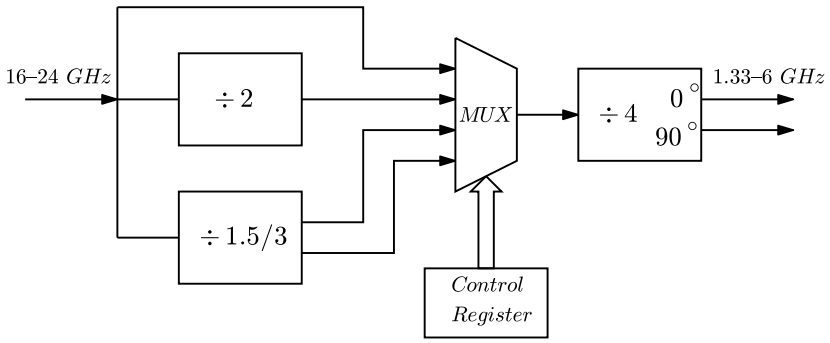


Figure 4.47: Block diagram of the multi-ratio frequency dividers

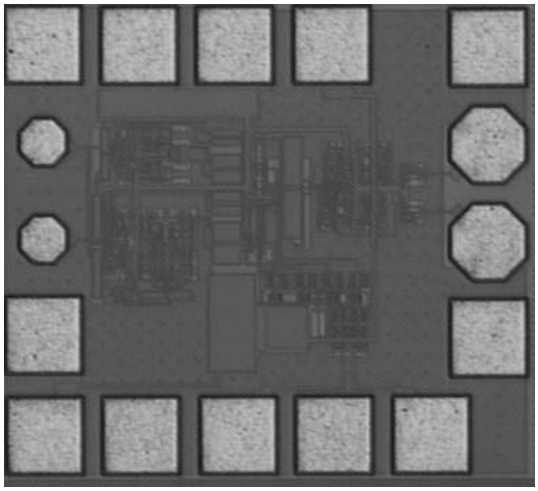
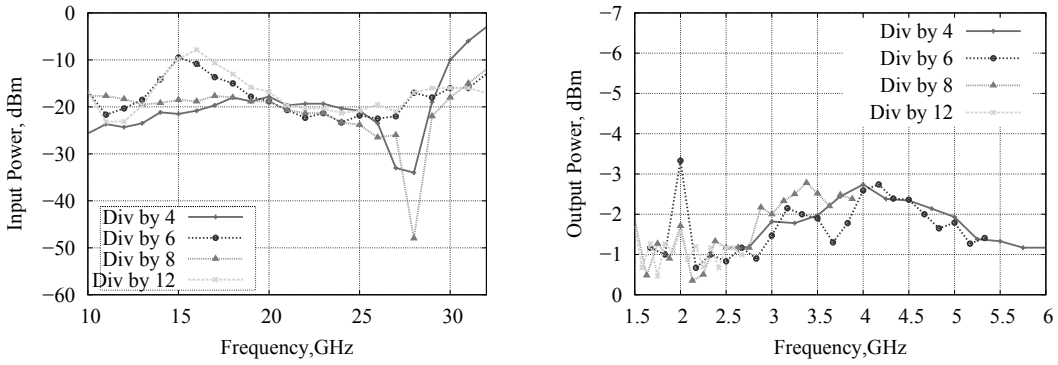


Figure 4.48: Chip micrograph of the multi-ratio frequency dividers, 500×550 μm^2

put frequency bands. The input frequency varies from 16 to 24 GHz, and the output frequency range from 1.33 to 6 GHz is achieved with an output power from -5.7 to -3.3 dBm. Since the output signals are in quadrature, they are suitable for

driving directly the LO ports at the IQ de-/modulators.



(a) (b)

Figure 4.49: (a) Input sensitivity of the multi-ratio frequency dividers (b) Output power of the multi-ratio frequency dividers versus output frequency bands

4.4.5 Summary

To select the type of dividers properly, tradeoffs need to be done between operating speed, frequency range power consumption and chip area. Static dividers are preferred for relatively low frequency applications, since they have a wider relative operating frequency range and need less chip area. Dynamic dividers are suitable for relatively high frequency applications, where static frequency dividers fail. Two prescalers were designed for the frequency synthesizers based on different applications. In the end, a high speed multi-ratio frequency divider was discussed; the input frequency range was reduced to 40% to achieve a continuous frequency sweep.

The performance of the frequency dividers discussed above is summarized in Tab. 4.9:

Table 4.9: Summarization of the key performance of the different types of frequency dividers

Dividers	Input frequency range, GHz	Power, mW
Dynamic ÷2	22-76	29
Static ÷2	0.2-60	60
Semi-dynamic ÷3	12-57	66
Prescaler ÷64	22-76	131
Prescaler ÷16-31	0-7	182
Multi ratio ÷4/6/8/12	10-32	220

4.5 Loop Filter

A typical active low pass filter includes an operational amplifier and R-C components. Since the output of the loop filter controls directly the tuning port of the VCO, it must be able to cover the effective VCO tuning voltage. In the IHP SG25H3 technology, HBTs with a higher breakdown voltage ($BV_{CEO} = 7$ V) were provided as shown in Tab. 4.1. The HV type of HBT was used for the active loop filter design, to achieve a higher output voltage swing. Due to the lack of PNP transistors in the available technology, a quasi operational amplifier using all NPN transistors was designed for the active loop filter based on the one discussed in [72]. Fig. 4.50 shows the schematic of the quasi operational amplifier. The input stage is a common emitter differential amplifier. The DC biasing voltage of the input is directly from the previous stage, which is the mixer type phase detector. The emitter coupled pair is biased at 1.8 mA. The emitter followers are used as buffers and level shifters. The output stage combines a common emitter and a common collector to achieve the differential to single-ended conversion. The transient behavior of the amplifier is shown in Fig. 4.51(a) at 1 MHz operating frequency. It indicates an output voltage swing of 5 V, which is sufficient to drive the tuning voltage of the VCO.

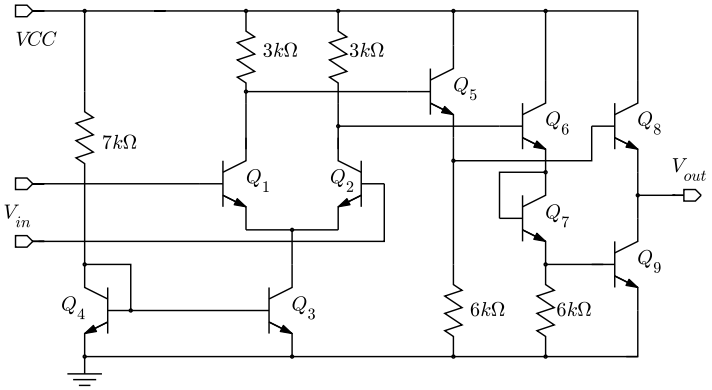
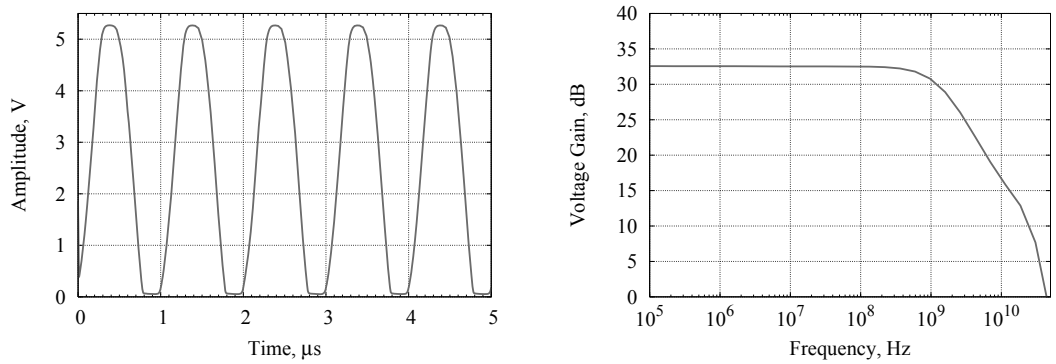


Figure 4.50: Simplified schematic of the differential to single-ended amplifier as a quasi operational amplifier, $Q_{1,2}$ = HV†4×2, Q_3 = MV* 4×1, Q_4 = MV* 2×1, Q_{5-9} = HV†2×1 (* Medium Voltage HBT, † High Voltage HBT, see Tab. 4.1)

The frequency response of the amplifier is shown in Fig. 4.51(b). The DC voltage gain is 32.6 dB, and the 3 dB bandwidth is 1.33 GHz. In this work, the PLL bandwidth is less than 20 MHz, which means the bandwidth for the amplifier is high enough for the loop filter design.

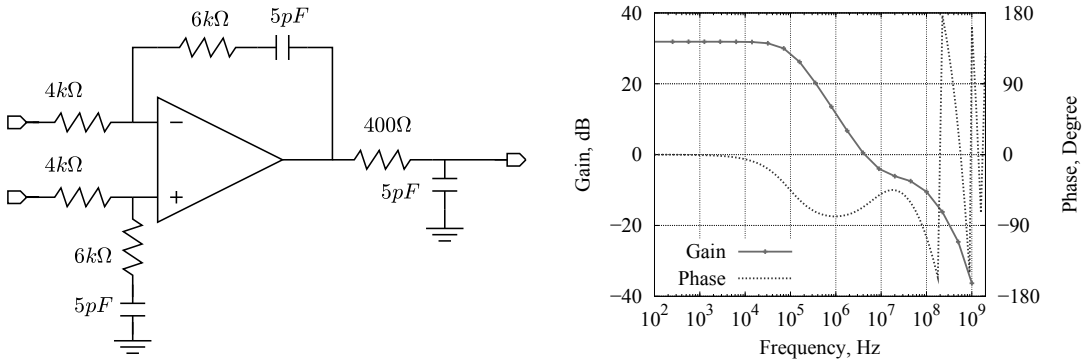
Fig. 4.52(a) shows the schematic of the second order loop filter, which is an active PI filter followed by an additional pole. The frequency response is shown in



(a) (b)

Figure 4.51: (a) Transient behavior of the amplifier with input frequency of 1 MHz and amplitude of 200 mV (b) Gain of the quasi operational amplifier

Fig. 4.52(b). The 3-dB bandwidth is at around 10 MHz and the phase margin is around 52°.



(a) (b)

Figure 4.52: (a) Schematic and (b) Frequency response of the second order low pass filter

4.6 Phase-Lock Indicator

In the dual-loop PLL design in this work, a phase-lock indicator is implemented to detect the locking state and switch between the two loops. The block diagram of the phase-lock indicator is shown in Fig. 4.53. The design is a modified version based on the lock indicator as described in [51]. It combines an EXOR phase detector, an RC low pass filter and a Schmitt trigger. The EXOR compares the phase difference of the signals, the phase error is smoothed by the low pass filter and then compared with a reference voltage level V_{ref}. When the phase error is below a certain threshold, the Schmitt trigger indicates the phase locked state.

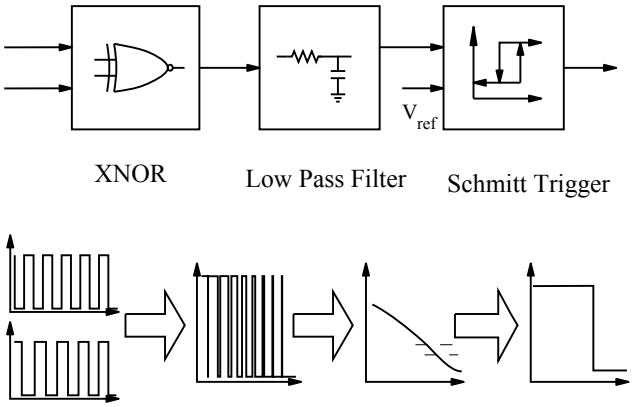


Figure 4.53: Block diagram of the phase-lock indicator

The schematic of the Schmitt trigger is shown in Fig. 4.54. It includes an operational amplifier and buffers in the output stage. The internal reference voltage with a hysteresis function is realized using a resistive voltage divider and an NMOS switch N_H. Assuming that initially V_{in} is higher than V_{ref}, the output V_{Id2} indicates logic low, the switch N_H is off and $V_{ref} = R_1 \cdot V_{DD}/(R_1 + R_2 + R_N)$. When V_{in} reduces below V_{ref}, the output V_{Id2} indicates logic high, the switch N_H is on and $V_{ref} = R_1 \cdot V_{DD}/(R_1 + R_2)$. The hysteresis function is realized due to the variation of V_{ref}. The transistor sizes are listed in Tab. 4.10.

Table 4.10: Values of the key component of the Schmitt trigger, w and l are the channel width and length of the CMOS transistors

N_{1-6}	$w = 3$ µm, $l = 270$ nm
N_H	$w = 16$ µm, $l = 270$ nm
P_{1-4}	$w = 3$ µm, $l = 270$ nm

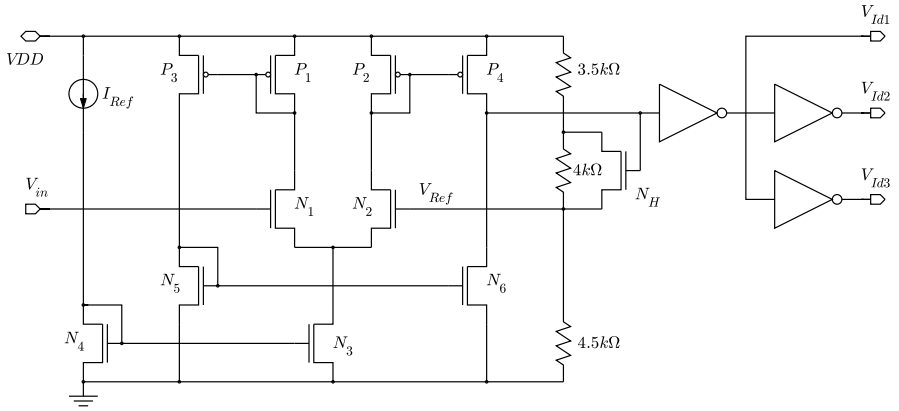


Figure 4.54: Simplified schematic of the Schmitt trigger

When the two signals are out of lock, an average phase error of $\pi/2$ will be presented at the input of the Schmitt trigger; while in the lock state, the phase error is zero. In practical designs, there are delay mismatches in the phase locked holding loop, the frequency acquisition loop and the phase-lock indicator. The phase error threshold is defined at $\pi/6$ for the quasi phase locking and $\pi/3$ for out of lock indication.

The simulated transient behavior of the Schmitt trigger is shown in Fig. 4.55. The input is a triangle signal with period of 400 ns. The hysteresis voltage is around 0.5 V.

The low pass filter is realized using an RC network to smooth the pulses at the output of the EXOR phase detector. In order to detect the locked state right after the phase error drops below the threshold, the bandwidth of the RC filter shall be comparable with the loop bandwidth of the PLL. In this work, the bandwidth is designed at 10 MHz with $R_I = 8$ kΩ, $C_I = 2$ pF.

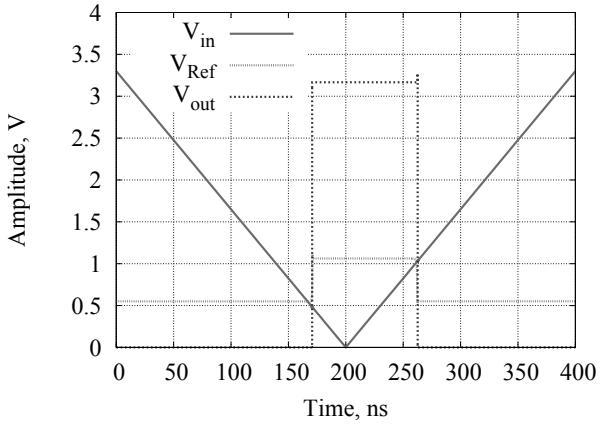


Figure 4.55: Simulated transient behavior of the Schmitt trigger

Fig. 4.56 shows the transient performance of the phase-lock indicator. The input comparison signals are two square waves with a period of 2 ns and a phase shift of 1/6 ns. The output of the EXOR is shown in the top figure, which is a pulse signal with around 16.7% duty cycle; after the RC low pass filter, the voltage level drops below the threshold voltage at 51 ns; and the indicator indicates a phase locked state.

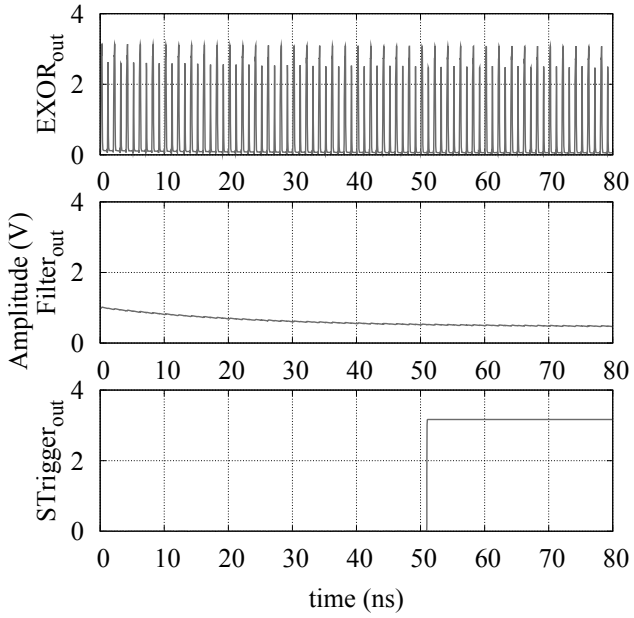


Figure 4.56: Simulated transient performance of the phase-lock indicator

5

System Simulation and Optimization

5.1 Frequency Response of the PLL

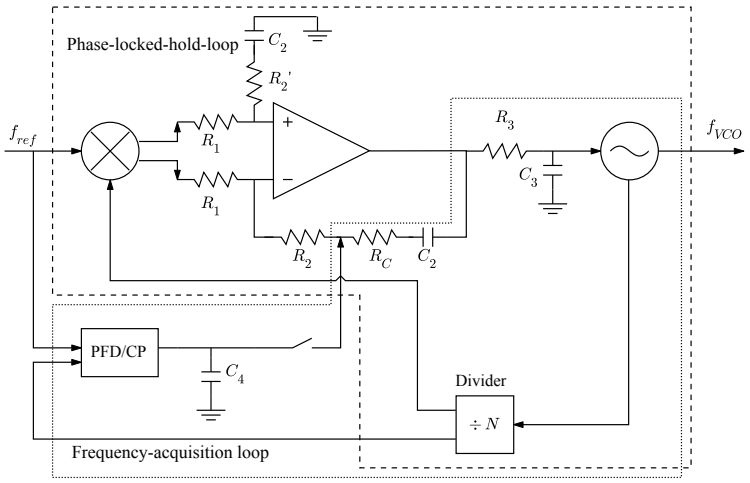


Figure 5.1: Schematic of the dual-loop PLL

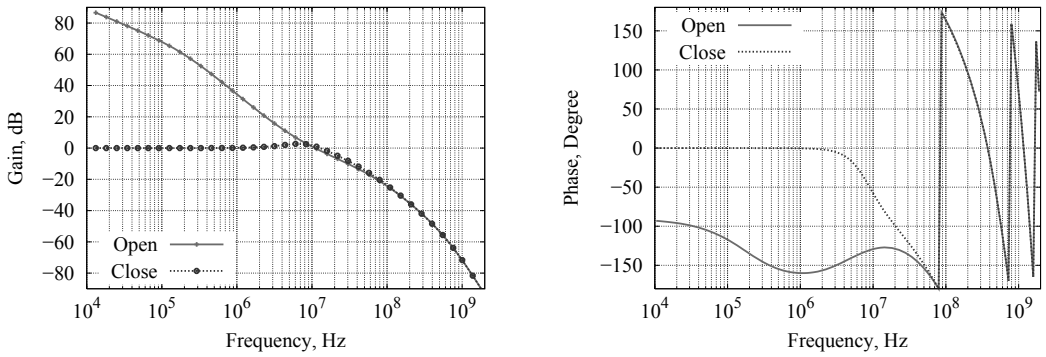
The schematic of the dual loop PLL is shown in Fig. 5.1, which combines a frequency acquisition loop and a phase locked hold loop. The phase locked hold loop is an APLL with an active PI loop filter as shown in Fig. 3.1. Assuming that the op-amp in the active filter is ideal, the frequency acquisition loop can be approximated as a DPLL as shown in Fig. 3.4. The filter transfer function of the frequency acquisition loop is similar to the one shown in Fig. 3.5, however with a reversed polarity. The phase error current from the charge pump is injected between R_2' and R_C. The loop bandwidth of the DPLL is set to around 3 times

the bandwidth of the APLL to achieve a fast frequency acquisition. The loop parameters are listed in Tab. 5.1

Table 5.1: Parameters of the frequency response simulation of the dual-loop PLL

Type	**APLL**	**DPLL**
Divider Ratio, N	32	
f_{comp}, MHz	1000	
ω_n, rad/s	47M	142M
Damp factor, ζ	0.71	0.71
Unity Gain Bandwidth, MHz	11	32
K_ϕ	0.8 V	1.8 mA
K_{VCO}, rad/(s·V)	1800M	
R_1, Ω	4k	
C_2, pF	5	
R_2, Ω	4k	
R_2', Ω	6k	
R_C, Ω	2k	
R_3, Ω	400	
C_3, pF	5	

Fig. 5.2 shows the simulated frequency response of the APLL at open loop and closed loop. The unity gain bandwidth is 11 MHz, and the phase margin is 52°.



(a) (b)

Figure 5.2: Simulated frequency response of the integer-N PLL with open loop (loop opened after the frequency divider) and closed loop in (a) amplitude and (b) phase.

As discussed in Chapter 4, the VCO gain K_{VCO} may vary by a factor of more

than 5 for PLLs with wide frequency tuning range. From the damping factor equation in (3.9), the variation of K_{VCO} may cause instabilities in the loop. Fig. 5.3(a) shows the frequency response of the PLL with different VCO gains varying from 500 M to 2500 M rad/(s·V). At the lowest K_{VCO}, the unity-gain bandwidth is reduced to 6.5 MHz and the phase margin is reduced to 36°. To compensate the variation of the VCO gain, loop parameters such as R_1, R_2 and C_2 can be designed as reconfigurable. Fig. 5.3(b) shows that a stable frequency response with variable K_{VCO} is achieved after the compensation by optimizing the other loop parameters. Tab. 5.2 lists the corresponded values of R_1, R_2 and C_2, which can be adjusted using CMOS switching networks or varactors in practical circuit designs.

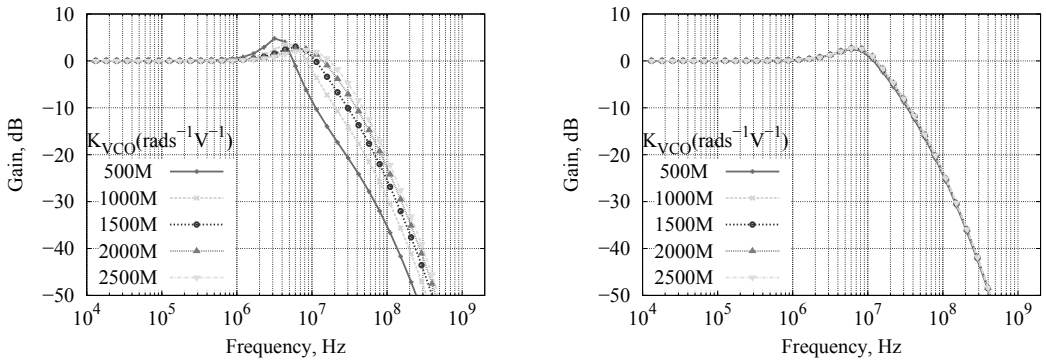


Figure 5.3: Frequency response of the PLL with variable VCO gain K_{VCO}, (a) original (b) after compensation by other loop parameters

Table 5.2: Loop parameters to compensate the variation of the VCO gain

K_{VCO}, rad/(s· V)	500M	1000M	1500M	2000M	2500M
R_1, Ω	1.1k	2.2k	3.3k	4k	4k
C_2, F	5p	5p	5p	5.5p	6.9p
R_2, Ω	6k	6k	6k	5.5k	4.3k

5.2 Phase Noise Modeling and Analysis

For the phase noise simulation and optimization of the dual-loop PLL, the sub-blocks from the phase locked hold loop are considered as the dominant noise sources; the noise behavior of the frequency acquisition loop is ignored since it

is isolated from the final locked state. The phase noise of each block (here for PD and loop filter is actual noise instead of phase noise) can be modeled using [73]:

$$\phi_{N,rms} = \sqrt{2 \cdot (10^{\frac{L_0}{10}} + 10^{\frac{L_{m1}}{10}} + 10^{\frac{L_{m2}}{10}} + 10^{\frac{L_{m3}}{10}} + ...)} \tag{5.1}$$

$$L_{m1} = L_1 + 10 \log \frac{f_1}{f} \tag{5.2}$$

$$L_{m2} = L_2 + 10 \log \frac{f_2}{f} \tag{5.3}$$

$$L_{m3} = L_3 + 10 \log \frac{f_3}{f} \tag{5.4}$$

where L_0 is the SSB noise floor, f_1, f_2, f_3 and L_1, L_2, L_3 represent the frequency and noise level at which the slopes are -10, -20 and -30 dB/decade as illustrated in Fig. 5.4.

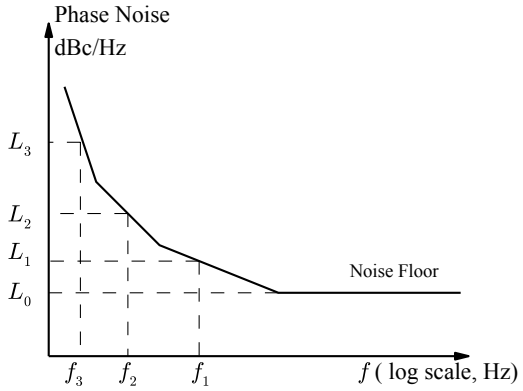


Figure 5.4: Phase noise modeling for the PLL components

Fig. 5.5 shows the modeled intrinsic phase noise of the VCO, phase detector, divider and loop filter based on the simulation results shown in Chapter 4. The VCO has a center frequency of 32 GHz; the low frequency noise of the phase detector is the one at 1 GHz comparison frequency; the frequency divider operates at 32 GHz input frequency.

The overall phase noise contribution function can be approximated as:

$$PN_{PLL} = \begin{cases} (\frac{PN_{PD}}{K_\phi} + \frac{PN_{Flt}}{K_\phi} + PN_{Div} + PN_{Ref}) \cdot N & \omega \ll \omega_c \\ PN_{VCO} & \omega \gg \omega_c \end{cases} \tag{5.5}$$

where PN_{PD} and PN_{Flt} are the intrinsic low frequency noise of the phase detector and the loop filter; PN_{Div}, PN_{VCO} and PN_{Ref} are the phase noise of the frequency divider, VCO and reference oscillator; ω is the offset frequency and ω_c is the loop bandwidth.

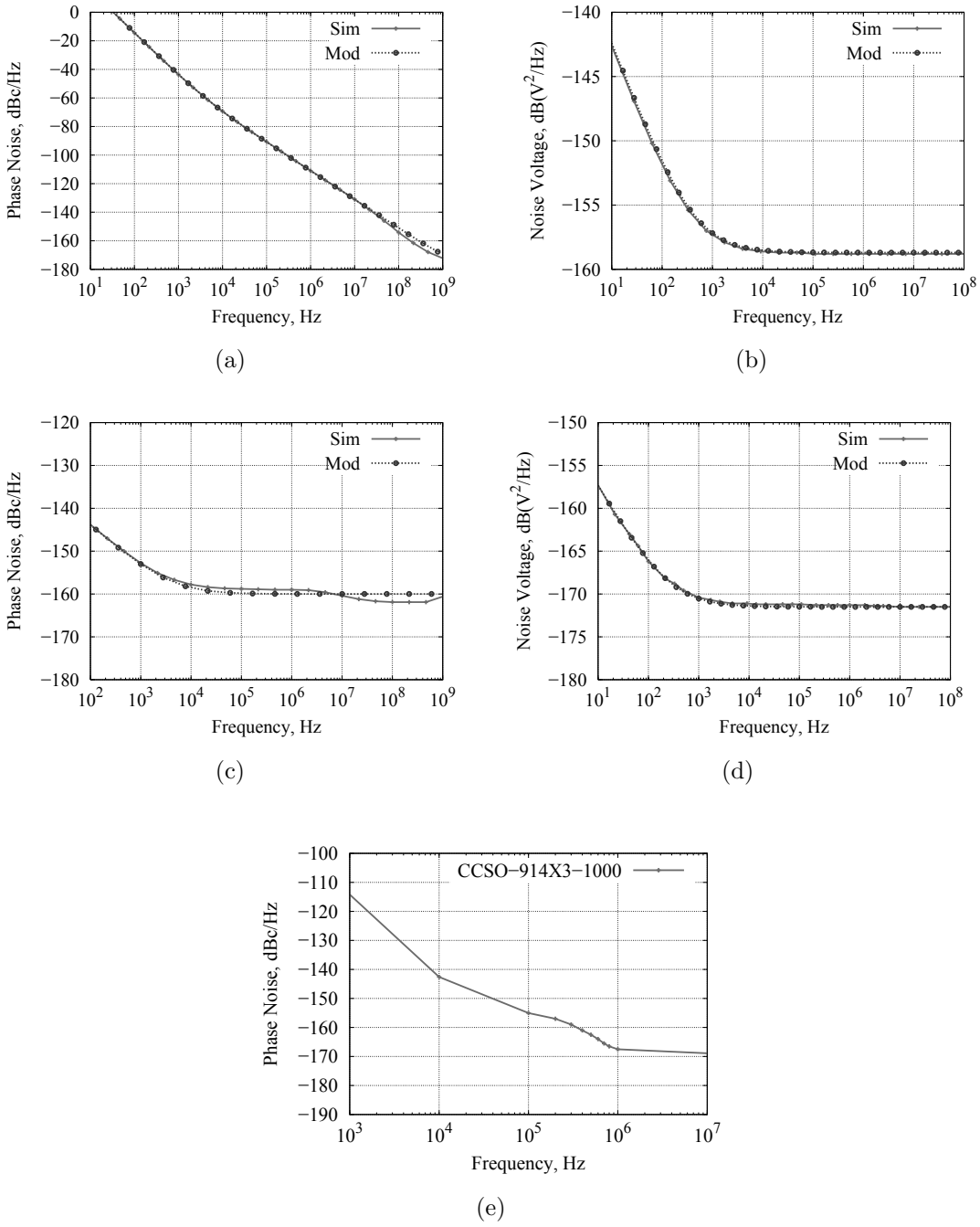


Figure 5.5: Phase Noise and low frequency noise modeling for (a) VCO, (b) Phase Detector, (c) Frequency divider and (d) Loop filter (e) Reference crystal oscillator from Crystek Cooperation

To obtain the optimum phase noise behavior, the loop bandwidth shall be designed at the point where the intrinsic phase noise of the free running VCO and the summation of noise contribution of the remaining PLL sub blocks cross [51]. As shown in Fig. 5.2, the summation of the noise contribution from the phase

detector, frequency divider and the loop filter has a noise floor of -125 dBc/Hz; and the phase noise of the free running VCO crosses the -125 dBc/Hz noise floor at 18 MHz, which is the optimum loop bandwidth.

Fig. 5.7(a) shows the comparison of the phase noise of different loop bandwidths. The frequency divider ratio is set to 32. By varying the loop filter parameters R_1, R_2 and C_2, the loop bandwidth varies from 8.5 MHz to 38 MHz, while the damping factor remains constant at 0.75. For the PLL with 8.5 MHz bandwidth, a ripple of 10 dB was created by the VCO phase noise. For the loop with 38 MHz, at frequency offsets from 18 to 38 MHz, the phase noise is no more dominated by the VCO but the other components, and degrades around 5 dB when comparing with the 18 MHz loop bandwidth. The loop with the 18 MHz bandwidth has better phase noise performance than the ones with 8.5 MHz and 38 MHz. Tab. 5.3 list the key parameters for the phase noise simulation of the PLL shown in Fig. 5.7(a)

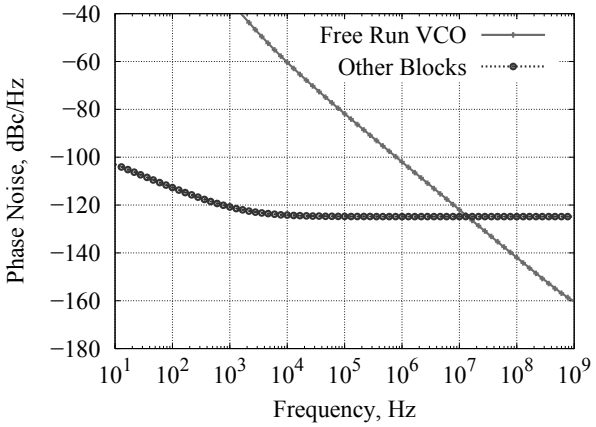


Figure 5.6: Phase noise of the simulated free running VCO at 32 GHz and the noise contribution from the other PLL blocks (reference noise neglected)

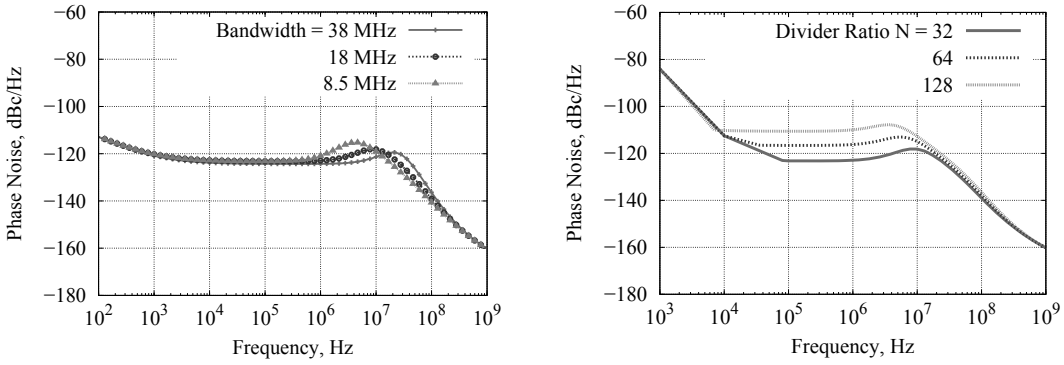
Equation (5.5) indicates that a low divider ratio N can improve the phase noise inside the loop bandwidth and consequently leads to a higher comparison frequency. In frequency synthesizer designs, trade-offs shall be made among the comparison frequency, the power consumption and operating speed of the multi-/dual- modules frequency dividers. In fractional-N PLL designs, the speed of the Σ-Δ modulator also limits the comparison frequency.

Fig. 5.7(b) shows the different phase noise of the integer-N PLL with frequency divider ratios 32, 64 and 128. To have a fair comparison, the gain factors of the VCO and the phase detector are kept constant for each state; the intrinsic phase noise of each PLL sub component is accessed from the models shown in Fig. 5.5. From (3.8), the loop bandwidth is automatically adjusted with the divider ratio

Table 5.3: Parameters of the phase noise simulation of the integer-N PLL with variable loop bandwidth

Unity-gain Bandwidth, MHz	**8.5**	**18**	**38**
Divider Ratio,	32		
f_{comp}, MHz	1000		
Damp factor, ζ	0.71		
K_ϕ, V	0.8		
K_{VCO}, rad/(s·V)	1800M		
R_1, Ω	4k	4k	1k
C_2, pF	20	5	5
R_2, Ω	3k	6k	3k
R_3, Ω	400		
C_3, pF	5		

by a factor of $\sqrt{2}$. As expressed in (3.9), the damping factor ζ is kept constant by varying the time constants τ_1 and τ_2.



(a) (b)

Figure 5.7: (a) Phase noise optimization of the PLL with variable loop bandwidth Bw = 8.5, 18, 38 MHz, reference noise neglected (b) Phase noise optimization of the PLL with variable frequency divider ratios N = 32, 64, 128, reference noise included

For frequency offsets inside the loop bandwidth, the phase noise at higher offset frequency degrades by 12 dB when the divider ratio increases from 32 to 128; the phase noise at very low offset frequency is independent from the divider ratio, since the phase noise of the reference signal is frequency dependent. For frequency offsets outside the loop bandwidth, the phase noise is independent from the frequency

divider ratio. Tab. 5.4 lists the key parameters in the phase noise simulation of the PLL shown in Fig. 5.7(b).

Table 5.4: Parameters of the phase noise simulation of the integer-N PLL with variable frequency divider ratios

Divider Ratio, N	**32**	**64**	**128**
f_{comp}, MHz	1000	250	62.5
ω_n, rad/s	47M	34M	24M
Damp factor, ζ	0.71		
Unity-gain Bandwidth, MHz	18	12	8
K_ϕ, V	0.8		
K_{VCO}, rad/(s· V)	1800M		
R_1, Ω	4k		
C_2, pF	5		
R_2, Ω	6k	8.5k	12k
R_3, Ω	400		
C_3, pF	5		

So far, the phase noise performance was analyzed without considering the thermal noise of R_1, R_2 and R_3 in the loop filter. The noise transfer function of the resistors are listed in Table 5.5: at low frequency offset, the transfer function of R_1 is approximated to N, similar to the transfer function of the loop filter; the transfer function of R_2 can be approximated to 0; the transfer function of R_3 is attenuated by a factor of the filter gain, and therefore also can be neglected. At high frequency offset, where the open loop gain is much smaller than N, the noise contribution from R_1, R_2 and R_3 can be neglected. As a conclusion, R_1 shall be low enough to avoid being the dominant noise source. However, as shown in (3.8), to achieve a specified natural frequency ω_n, a trade-off is required between R_1 and the area consumption of the on chip capacitor C_2.

5.3 Transient Behaviors of the PLL

As was described in (3.11), the lock-in time is directly related with the loop bandwidth ω_n. Fig. 5.8 shows the simulated transient behavior of the APLL with different unity-gain bandwidths varying from 4 MHz to 18 MHz. The initial frequency is set to 31.9 GHz, and the final locked frequency is 32 GHz. At the phase detector input, the initial frequency error is 3.125 MHz. From (3.10), the pull-in

Table 5.5: Phase transfer functions of the resistive components in the active loop filter of the PLLs, $\tau_1 = R_1C_2$, $\tau_2 = R_2C_2$

Noise Source	**Transfer Function**	**Low Frequency**	**High Frequency**
R_1	$\frac{G}{1+GH}\sqrt{\frac{s\tau_2+1}{s(\tau_1+\tau_2)+1}}$	N	$G\sqrt{\frac{R_2}{R_1+R_2}}$
R_2	$\frac{G}{1+GH}\sqrt{\frac{s\tau_1}{s(\tau_1+\tau_2)+1}}$	0	$G\sqrt{\frac{R_1}{R_1+R_2}}$
R_3	$\frac{G}{1+GH}\frac{\sqrt{s\tau_3+1}}{Z(s)}$	$\frac{N}{Z(s)}$	$\frac{G}{Z(s)}$

process can be neglected and the lock-in process starts immediately. At 4 MHz bandwidth, the lock-in time is around 0.5 µs. By increasing the bandwidth to 18 MHz, the lock-in time is reduced to 0.13 µs. The other loop parameters are listed in Tab. 5.6.

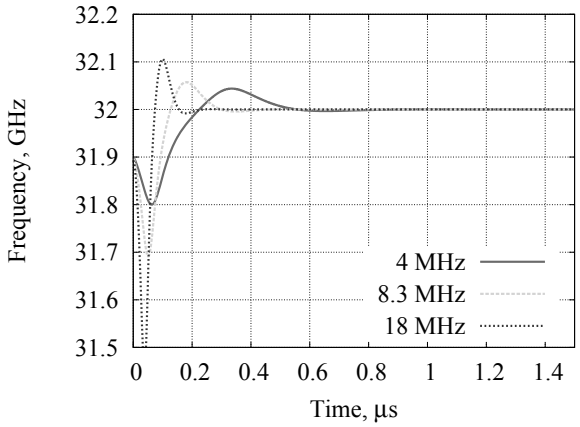


Figure 5.8: Transient simulation of the PLL with variable 3-dB bandwidth 4, 8.3, 18 MHz

Fig. 5.9 shows the transient lock-in process with different loop damping factors ζ= 0.36, 0.71, 0.95.

For a smaller ζ, the loop settles down with a larger over-shoot and in a longer time. To further characterize the loop settling time, Fig. 5.9 is re-plotted as the transient behavior of the normalized frequency error in $\log(\Delta\omega/\omega_0)$ in Fig. 5.10. In this work, the locking point is defined as when the normalized frequency error reduces below -80 dB, which is 0.01% of the targeted frequency. For $\zeta = 0.36$, the settle time is 0.5 µs; and reduces to 0.21 and 0.18 µs when ζ increases to 0.71 and 0.95. The other loop parameters for the variable damping factor simulation are listed in Tab. 5.7.

When the difference between the initial frequency and the target frequency is larger than the loop bandwidth, a pull-in process occurs. As in (3.10), the pull-

Table 5.6: Parameters of the transient simulation of the integer-N PLL with variable loop bandwidth

Unity-gain Bandwidth, MHz	**4**	**8.3**	**18**
ω_n, rad/s	12 M	24 M	47 M
Divider Ratio, N	32		
f_{comp}, MHz	1000		
Damp factor, ζ	0.71		
K_ϕ, V	0.8		
K_{VCO}, rad/(s·V)	1800M		
R_1, Ω	16k	4k	4k
C_2, pF	20	20	5
R_2, Ω	6k	3k	6k
R_3, Ω	400		
C_3, pF	5		

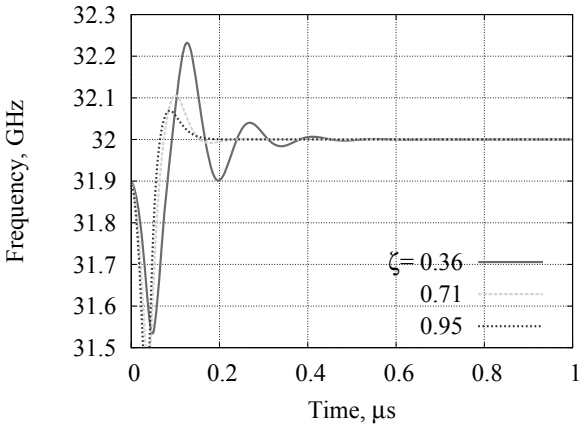


Figure 5.9: Transient simulation of the PLL with variable damping factors ζ = 0.36, 0.71, 0.95

in time of an APLL is a function of ω_n, ζ and proportional to the square of the initial frequency offset $\Delta\omega_0$. Fig. 5.11 shows the transient simulation of the PLL with variable initial frequency offset $\Delta\omega$ = 20M, 120M and 200M rad/s. The loop bandwidth ω_n is 18M rad/s, and the damp factor ζ is 0.71.

The 20M rad/s offset frequency is comparable with the loop bandwidth ω_n , and the pull-in time can be neglected. For the one with 120M rad/s frequency offset, the pull-in time is 0.2 µs; and increases to 0.6 µs for the 200M rad/s frequency offset. In practical designs with wide tuning range VCOs, the frequency offset can be even larger than 600M rad/s; and the correlated pull-in time can be as long

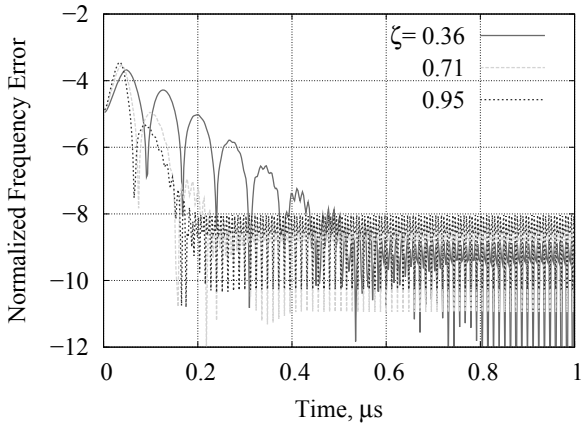


Figure 5.10: Transient normalized frequency error in the lock-in process with different damp factors $\zeta = 0.36, 0.71, 0.95$.

Table 5.7: Parameters of the transient simulation of the integer-N PLL with variable damp factors

Damp factor ζ	**0.36**	**0.71**	**0.95**
Divider Ratio, N	32		
f_{comp}, MHz	1000		
Unity-gain bandwidth, Hz	18 M		
K_ϕ, V	0.8		
K_{VCO}, rad/(s·V)	1800M		
R_1, Ω	4k		
C_2, pF	5p		
R_2, Ω	3k	6k	8k
R_3, Ω	400		
C_3, pF	5		

as 5 µs. In worst cases, due to the initial DC offset of the phase detector or the active loop filter, if the polarity of the DC offset does not correspond with the final tuning voltage of the VCO, the PLL may never achieve the locked state.

In this work, the pull-in process is replaced by a frequency acquisition loop using a 3-state PFD, which has a much shorter pull-in time than a mixer type PD, especially when the frequency offset is larger than the comparison frequency. The pull-in time of a DPLL is proportional to the initial frequency offset $\Delta\omega_0$ instead of $\Delta\omega_0^2$ (see (3.17)). Fig. 5.12 shows the simulated transient response of a DPLL when a 3-state PFD is applied comparing with an APLL as discussed above. The initial frequency offset is set to 200M rad/s (around 31.25 MHz) at 1 GHz comparison

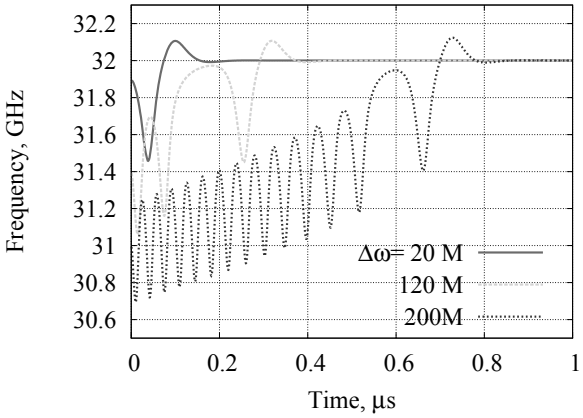


Figure 5.11: Transient simulation of the PLL with variable initial frequency offset $\Delta\omega$ = 20M, 120M, 200M rad/s

frequency. The loop bandwidth of both types of PLLs is designed as 18 MHz. The pull-in time by using the DPLL is now reduced from 0.5 µs to less than 0.05 µs.

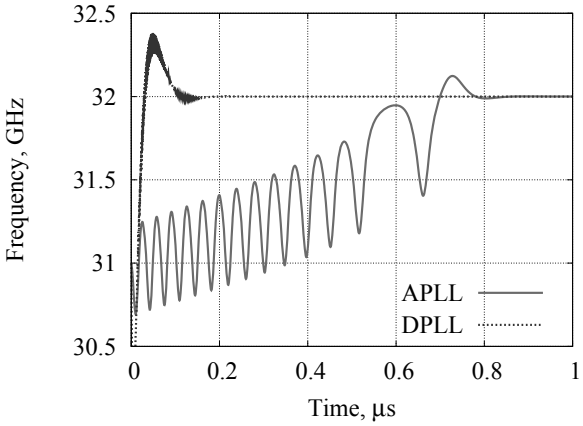


Figure 5.12: Transient simulation of the APLL in comparison with DPLL at 200M rad/s offset frequency

One of the most common methods to reconfigure the lock time of a DPLL is to tune the loop bandwidth by varying the maximum current I_{cp} of the charge pump [74]. Fig. 5.13 shows the transient simulation of a DPLL with variable charge pump current with an initial frequency offset of 400M rad/s. At I_{cp} = 0.2 mA, the pull-in time is around 0.3 µs. In this work, I_{cp} is set to around 2 mA, and the pull-in time is reduced to 0.03 µs.

In the dual-loop PLL designs, the phase error is indicated by a phase-lock indicator. Once the phase error is below a certain threshold, the DPLL is switched off and the APLL works as the dominant loop and locks the signal. Fig. 5.14

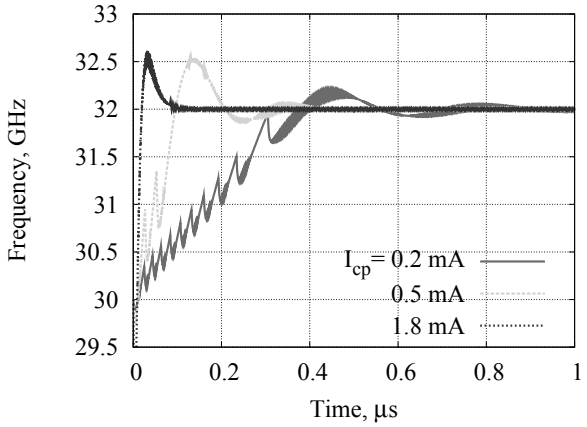


Figure 5.13: Transient simulation of the DPLL with variable maximum charge pump current I_{cp} = 0.2, 0.5, 1.8 mA

shows the transient behavior of the single APLL and Dual Loop PLL. The initial frequency offset $\Delta\omega$ is 176M rad/s. The dual-loop PLL improves the pull-in time from 0.4 µs to 0.03 µs.

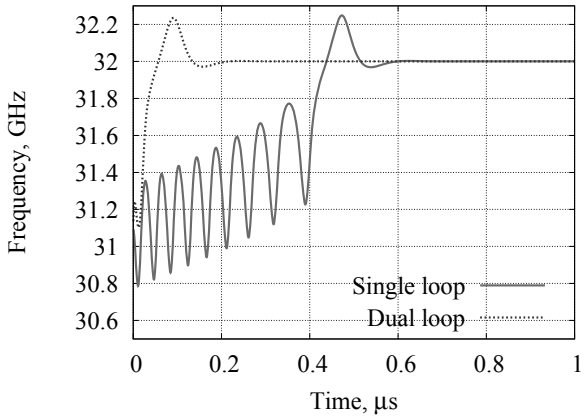


Figure 5.14: Transient simulation of the APLL and Dual-loop PLL

6

System Integration and Experimental Results

In this chapter, three demonstrators are presented. The first demonstrator is a fully integrated 35 GHz dual-loop PLL, with ultra-low phase noise and a fast lock time, targeting Ka-band radar applications. The second demonstrator is a fully integrated frequency synthesizer with ultra wide frequency tuning range from 16 to 24 GHz for multi-band satellite communications. The third demonstrator shows a 3 to 5 GHz reconfigurable receiver, where the wideband LO signals were generated from the 16-24 GHz frequency synthesizer.

6.1 A 35 GHz Dual-Loop PLL

The block diagram of the 35 GHz dual-loop PLL is shown in Fig. 6.1. The design is a modified version based on the PLL described in [51]. The frequency divider ratio N is set to 64. The reference frequency centers at 550 MHz, and the output frequency of the PLL centers at 35.2 GHz. The performance of the mixer type PD, PFD, charge pump, frequency dividers, loop filter and the lock indicator was discussed in detail in Chapter 4. The rest of the loop parameters are listed in Table. 6.1.

Table 6.1: Loop filter parameters of the 35 GHz dual-loop PLL

R_1, R_1', R_2	4 kΩ	R_C	2 kΩ
C_2, C_2'	5 pF	R_2'	6 kΩ
C_3	5 pF	R_3	400 Ω
C_4	1 pF	R_4	400 Ω

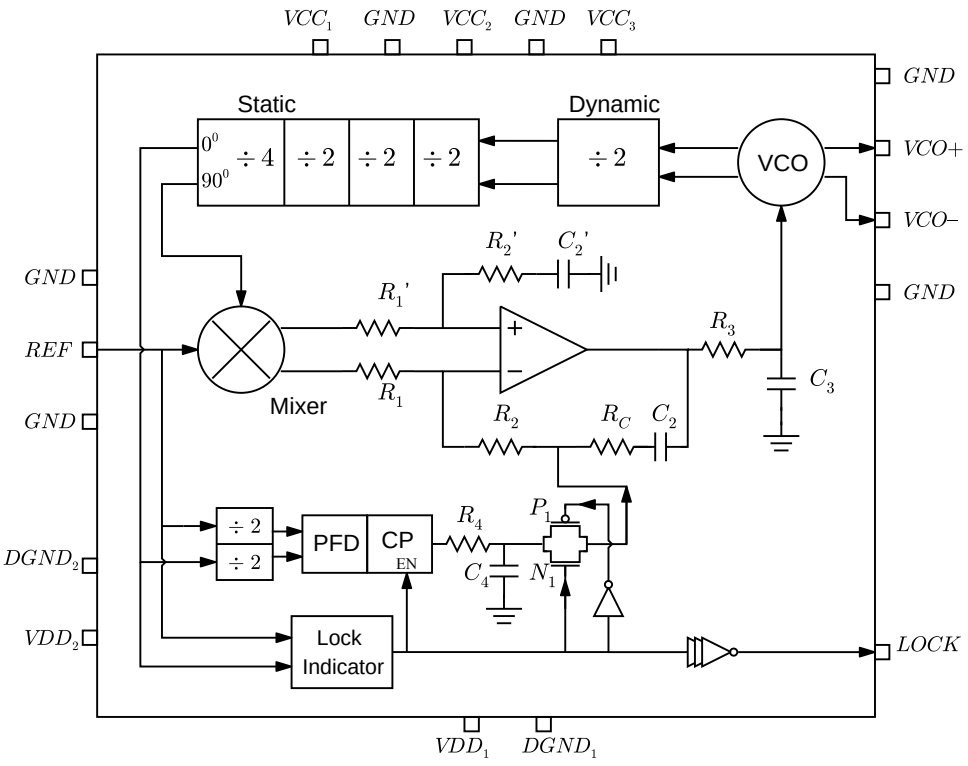


Figure 6.1: Block diagram of the 35 GHz dual-loop PLL

As discussed in Section 4.2, the frequency detecting range of the 3-state PFD degrades for comparison signals above 500 MHz. In this design, additional frequency dividers are implemented in front of the PFD, which reduce the comparison frequency to half of the one for the mixer type PD. The quadrature outputs of the frequency divider feed the two phase detectors respectively. The pin descriptions of the chip are listed in Tab C.1 in Appendix C.

All the blocks as shown in Fig. 6.1 are integrated on a single die. The chip micrograph is shown in Fig. 6.2, with a chip area of 780 $\times$ 580 μm^2. The total power consumption is 220 mW.

The chip was characterized by on-wafer measurement. An Agilent 8254A signal source was used to generate the reference signal. The spectrum of the PLL output was assessed using an Agilent 8565 EC spectrum analyzer. The frequency acquisition loop has a separated voltage supply to minimize the noise interference to the phase locked hold loop. When the frequency acquisition loop is disabled, the locking range of the phase locked hold loop is only around 550 MHz. When the frequency acquisition loop is enabled, the locking range is improved to 6.9 GHz. The complete frequency tuning range of the PLL is from 31.9 GHz to 38.8 GHz.

The spectrum of the PLL output at 35 GHz center frequency is shown in

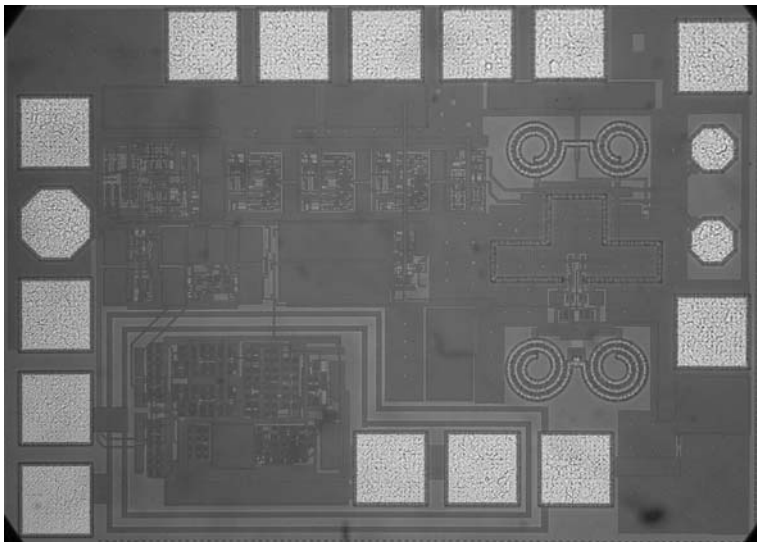


Figure 6.2: Chip micrograph of the 35 GHz dual-loop PLL. The die size is 780×580 μm^2

Fig. 6.3. The differential output power is -2 dBm after the compensation of the loss on the cables and on-wafer probes.

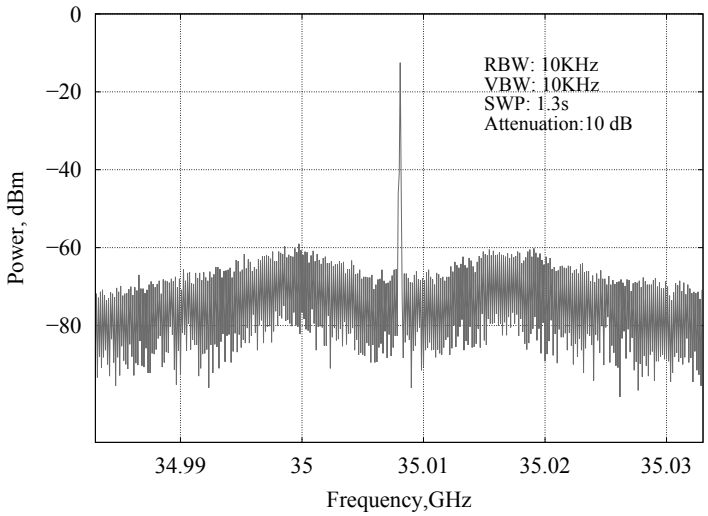


Figure 6.3: Spectrum of the PLL output with a center frequency of 35.008 GHz and a span of 50 MHz

Fig. 6.4 shows the measured phase noise at 35 GHz center frequency for offsets from 3 kHz to 300 MHz. The phase noise at 100 kHz offset is -100 dBc/Hz and -106 dBc/Hz at 1 MHz offset. The first order reference spur at 550 MHz is -64 dBc due to the leakage from the noisy charge pump after the switch of the frequency acquisition loop. The bandwidth of the PLL is around 15 MHz. This work is compared with previous publications in Tab. 6.2.

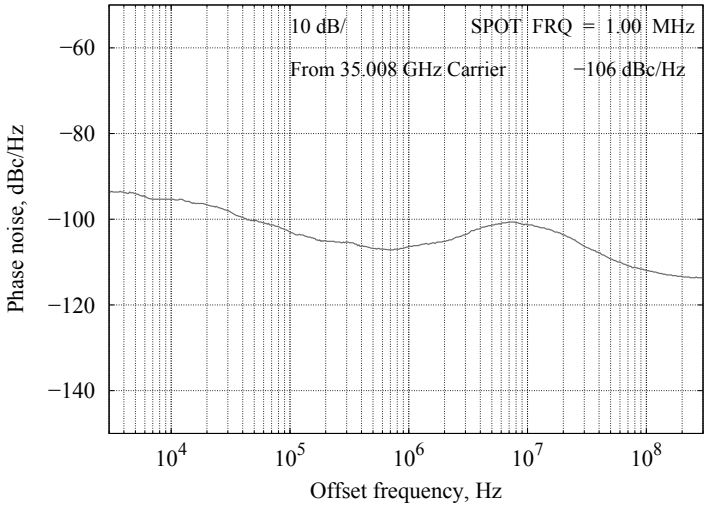


Figure 6.4: Measured phase noise of the PLL at 35 GHz center frequency

Table 6.2: Measured performance compared with prior published work

	This work	[75]	[76]	[77]
Technology	0.25 µm BiCMOS	65 nm CMOS	90 nm CMOS	0.25 µm BiCMOS
Frequency range(GHz)	31.9 to 38.8	35 to 41.9	39.1 to 41.6	28.5 to 32
Phase Noise (dBc/Hz) 1 MHz offset	-106	-97.5	-90	-81
f_{ref} (MHz)	550	36	50	125
Ref. Spur (dBc)	-64	-50	-54	-42
Power (mW)	220	80	64	287.5
Area (mm^2)	0.58×0.78	1.6×1.9	1.77×0.87	0.7×0.8

6.2 A 16-24 GHz Frequency Synthesizer

The block diagram of the 16 to 24 GHz frequency synthesizer is shown in Fig. 6.5. The dual-loop topology is similar to the one shown in Fig. 6.1. The prescaler design was described in Section 4.4. The multi-modulus frequency divider has a programmable divider ratio from 16 to 31. The dual-band VCO with 40% frequency tuning range which was discussed in Section 4.3.4 is implemented in this design. The comparison frequency is set to 210 MHz, which is mainly limited by the operating frequency range of the programmable divider after the trade-off with

the power consumption. A ÷2 frequency divider is used at the reference input to generate the 90° phase shift for the two types of phase detectors. The reference frequency is set to 420 MHz. The pin descriptions of the 16-24 GHz frequency synthesizer are listed in Tab. C.2 in Appendix C.

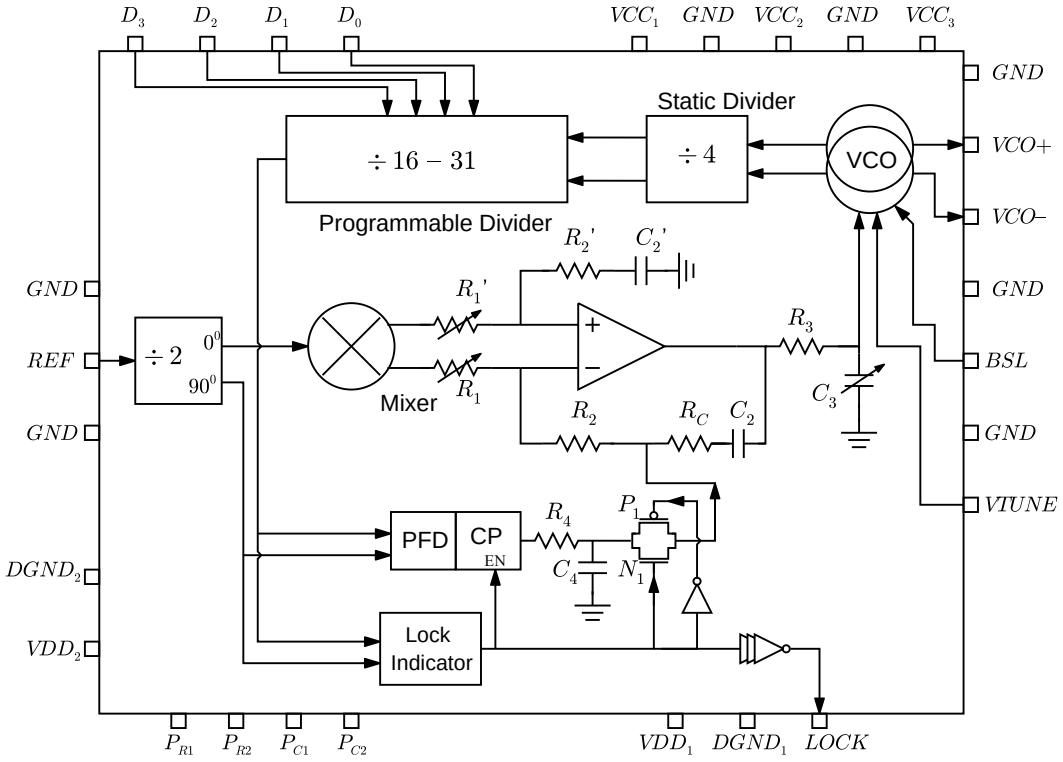


Figure 6.5: Block diagram of the 16 to 24 GHz frequency synthesizer

In this work, the loop response is designed to be reconfigurable by adjusting the filter parameters R_1, C_3 (see Section 5.1) and the external coarse tuning voltage (see Section 4.3.4). Tab. 6.3 lists the values of the filter parameters.

The chip micrograph is shown in Fig. 6.6 with a chip area of 1200×860 μm^2. The total power consumption is 520 mW. The chip is mounted on a Rogers 5880 substrate for characterization. An FR4 carrier was used below the Rogers substrate. The evaluation board was cased in an aluminum package as shown in Fig. 6.7.

The board was characterized using a method similar to the one used in the first demonstrator. The output frequency of the PLL varies from 15.96 to 23.52 GHz in steps of 0.84 GHz. When the external coarse tuning for the VCO is applied, to compensate the resonator capacitance and maintain the lock state, the fine tuning voltage which is controlled by the loop has to shift against the coarse tuning voltage. The spectrum of the PLL output at different coarse tuning voltages is

Table 6.3: Loop filter parameters of the 16-24 GHz dual-loop frequency synthesizer

Name	**Values**
R_1, R_1',kΩ	2.1, 2.8, 4.4, 10
R_2, kΩ	2
R_C, kΩ	4
R_2', kΩ	6
C_2, C_2', pF	5
R_3, kΩ	1.5
C_3, pF	1, 3.5, 6, 8.5
R_4, kΩ	5
C_4, fF	200

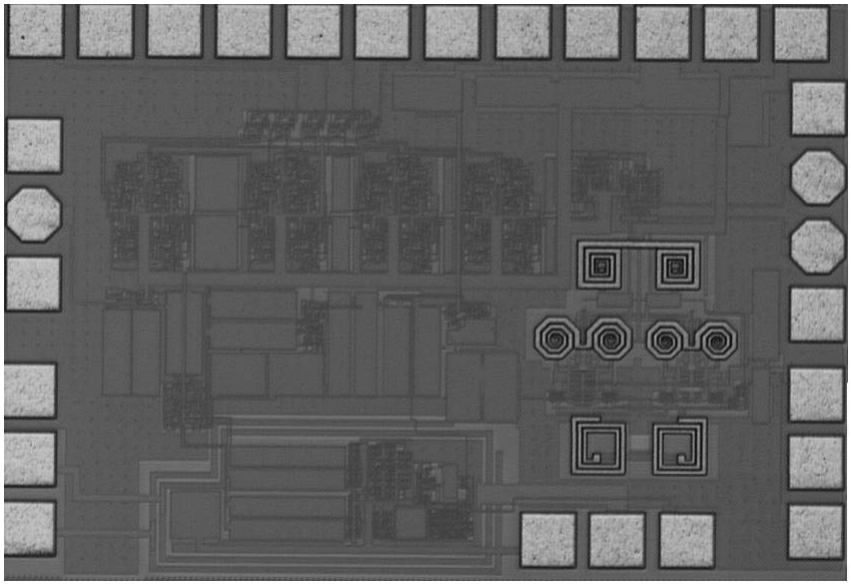


Figure 6.6: Chip micrograph of the 16 to 24 GHz frequency synthesizer. The die size is 1200×860 μm^2

shown in Fig. 6.8 with a center frequency of 22.68 GHz and a span of 20 MHz. The resolution bandwidth is 20 kHz. With various external coarse tuning voltages, the loop behavior changes corresponding to the variation of the VCO control gain K_{VCO}. With a lower external tuning voltage, K_{VCO} and the loop bandwidth are increased, and the in-band phase noise behavior is improved. Together with the switchable RC networks in the loop filter, the coarse tuning port can be calibrated to achieve the best noise performance.

The differential output power is 0 dBm after the compensation of the cable and connector losses. The measured phase noise is shown in Fig. 6.9, with the offset

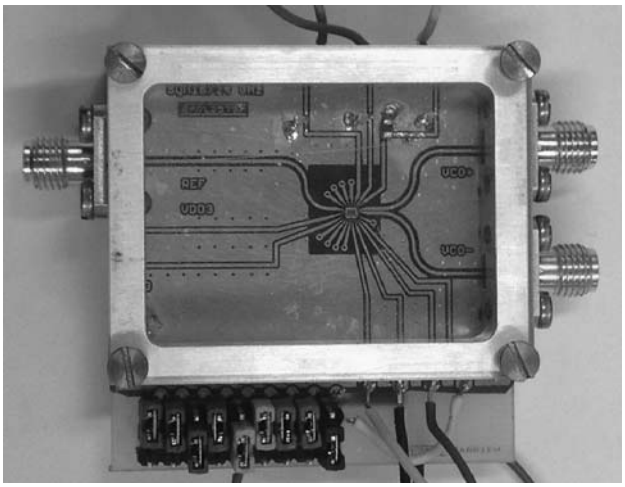


Figure 6.7: Evaluation board of the 16-24 GHz frequency synthesizer

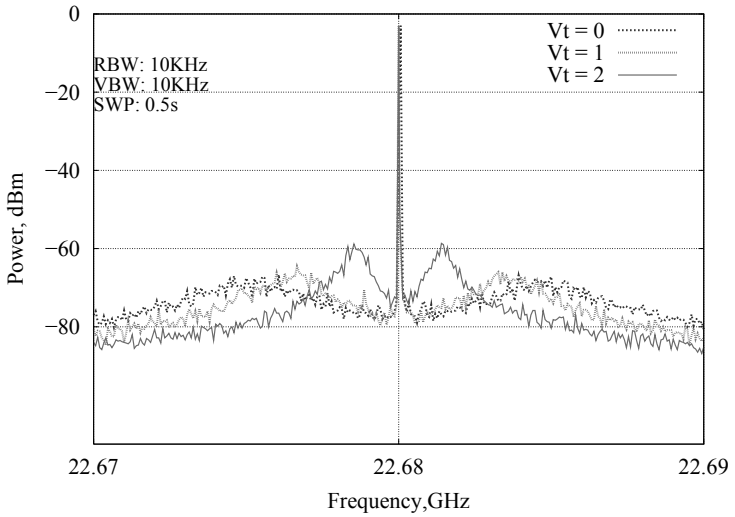


Figure 6.8: Spectrum of the PLL output in the lock state with a span of 50 MHz, with various external coarse tuning voltages

frequency varying from 3 kHz to 30 MHz at center frequencies of 15.96, 20.16 and 22.68 GHz. For the 22.68 GHz center frequency, the phase noise at 100 kHz offset is -104 dBc/Hz and -106 dBc/Hz at 1 MHz offset, which agrees well with the simulation results. Due to the leakage from the noisy charge pump after the switch of the frequency acquisition loop, a first order reference spur of -60 dBc is observed at the 210 MHz offset. Table 6.4 lists the comparison of the key parameters with previous publications.

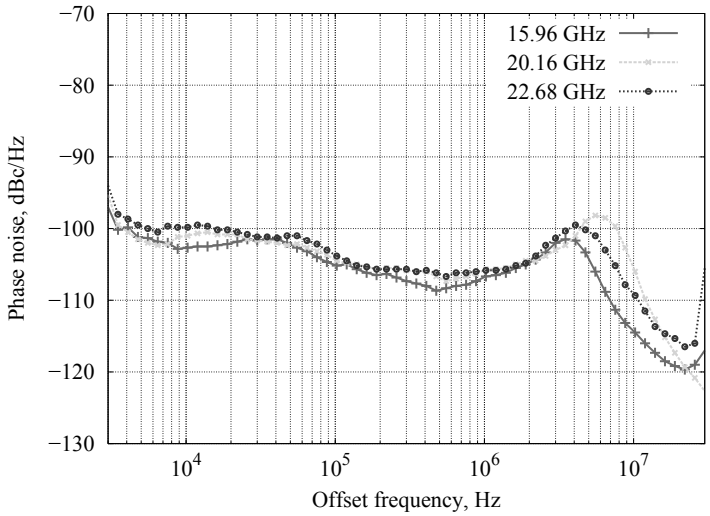


Figure 6.9: Measured phase noise of the PLL output at various center frequencies

Table 6.4: Measured performance of the 16-24 GHz PLL compared with prior published work

	This work	[78]	[79]	[80]
Technology	0.25 µm BiCMOS	65 nm CMOS	0.13 µm BiCMOS	0.25 µm BiCMOS
Frequency range(GHz)	15.96 to 23.52	20 to 28	15.95 to 18.81	17.5 to 18.9
Phase Noise (dBc/Hz) 1 MHz offset	-106	-91	-101	-110
f_{ref} (MHz)	210	27	285.7	N/A
Ref. Spur (dBc)	-60	N/A	-60 to -77	-65
Power (mW)	520	N/A	144	N/A
Area (mm^2)	1.2×0.86	N/A-	1×0.68	5

6.3 A 3-5 GHz Reconfigurable Receiver

With the emergence of new communication standards and allocated frequency bands, a highly reconfigurable RF front-end which is able to adjust to the targeted operating frequency ranges and applications is desired. An agile frequency synthesizer which covers all the specified frequency bands is one of the biggest challenges in the RF frond-end design. As a proof of concept, a 3-5 GHz reconfigurable receiver targeting small cell base station applications was designed with a

fully integrated frequency synthesizer.

A direct down conversion architecture is proposed for the reconfigurable receiver design, because of its many attractive qualities over a heterodyne architecture such as: higher flexibility, fewer components and lower costs [81][82]. However, it also has some well known design challenges such as 1/f noise, DC-offset, IQ mismatch, LO radiation and so on. Several techniques have been proposed to solve the 1/f noise and DC-offset problems. An approach using a modified differential voltage current conveyor to replace the high value capacitor in the high pass filter was proposed in [83] for DC-offset cancellation. In [84], a method to achieve the DC-offset cancellation with a faster settling time using pre-stored DC offset values through a feedback loop was proposed. IQ mismatch within a certain tolerance can also be corrected in the base band processing to achieve sufficient attenuation of the interferences. Some algorithms for IQ imbalance correction with different post and pre-FFT estimation and correction techniques were discussed in [85]. In [86], a method for IQ imbalance correction for the application of OFDM WLAN receivers was proposed; based on the estimation of a long OFDM preamble symbol, an IQ imbalance of 3 dB in amplitude and 10° in phase can be tolerated.

The block diagram of the proposed receiver is shown in Fig. 6.10, which includes an LNA, an IQ demodulator, two Variable Gain Amplifiers (VGAs) and two channel select filters and a frequency synthesizer for LO generation. The pin descriptions of the 3-5 GHz direct down conversion receiver are listed in Tab. C.3 in Appendix C.

LNA

The schematic of the LNA is shown in Fig. 6.11(a). A cascode topology is used to reduce the Miller capacitance of T_1, thus increasing the gain and bandwidth. A 0.17 nH inductive degeneration is used at emitter of T_1 to improve the noise figure [87]. A weak resistive feedback R_{feed} of 700 Ω with a serial capacitor C_{feed} of 50 fF is used to further increase the bandwidth, under the penalty of degraded gain and noise performance. A 2 nH inductive load L_C is used instead of a resistive load to reduce the power consumption; a 15 Ω series resistor R_2 is added to the load to improve the stability. A 1.5 nH inductance L_b is required for the 50 Ω input impedance matching at 4 GHz center frequency, which can be realized by the indispensable bond wire at the input of the LNA.

Fig. 6.11(b) shows the comparison of the simulated S-parameters with the measurement results. At a frequency range from 3 to 5 GHz, it has 17 dB gain with ±1 dB variation. The best input matching is achieved at 3.7 GHz by using a 1.5 nH

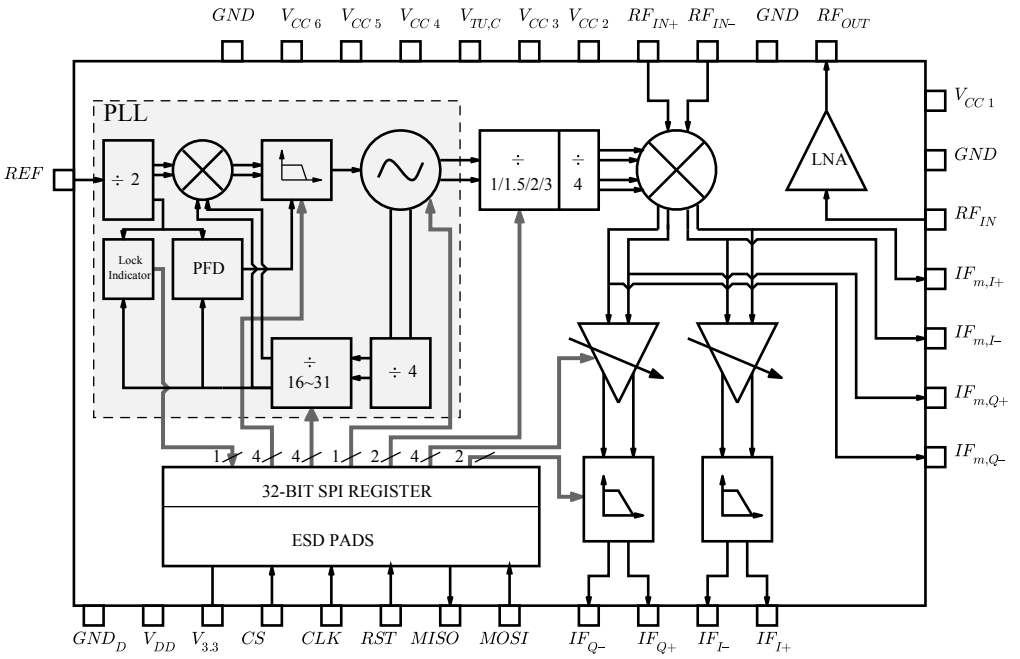
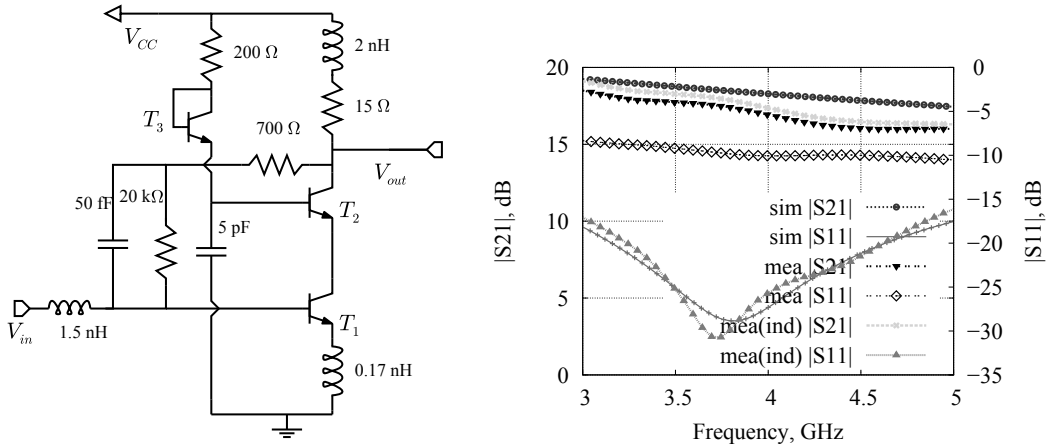


Figure 6.10: Block diagram of a 3-5 GHz direct down conversion receiver



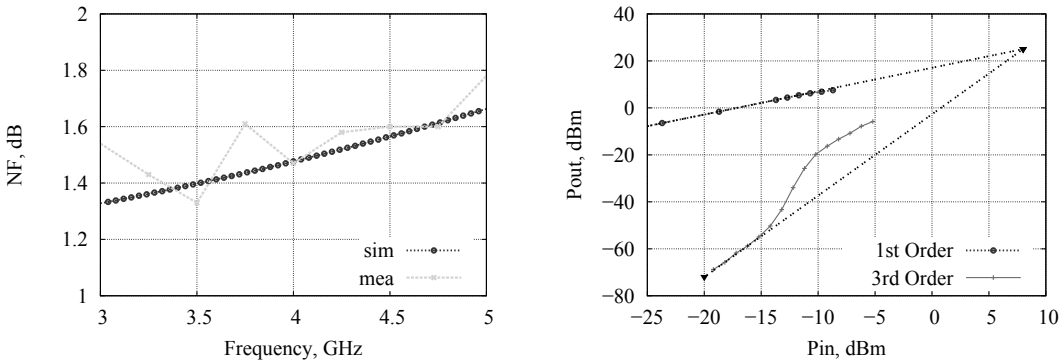
(a) (b)

Figure 6.11: (a) Schematic of a 3-5 GHz LNA (T_1 = shp×40, T_2 = shp×16, T_3 = shp×8 (see Tab. 4.1)) (b) Simulated and measured S-parameters

bond wire at the input. As shown in Fig. 6.12(a), the noise figure varies from 1.4 to 1.8 dB, which matched well with the simulation. The measured linearity is shown in Fig. 6.12(b): at 4 GHz, the input 1 dB compression point is -7.2 dBm; the input IP3 is 8 dBm. The complete power consumption is around 75 mW.

IQ demodulator

The IQ demodulator is designed based on a Gilbert Mixer. The simplified schematic



(a) (b)

Figure 6.12: (a) Noise Figure of the 3-5 GHz LNA (b) Linearity at 4 GHz

of the IQ mixer is shown in Fig. 6.13. To minimize the IQ mismatches, the transconductance stages of the in-phase and quadrature signals are merged to one common emitter pair. The HBTs in the transconductance stage are optimized to an emitter width of 0.84×16 μm and a collector current of 5 mA. The emitter width of the HBTs in the switching quads is 0.84×4 μm. The input linearity is improved by applying 50 Ω resistive emitter degeneration. Emitter followers and RC low pass filters are added after the IQ outputs of the mixer. The corner frequency of the RC filters is 530 MHz.

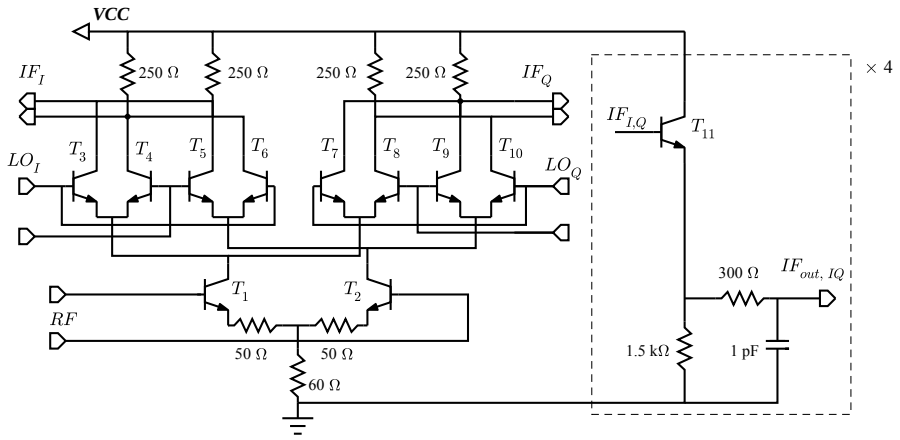
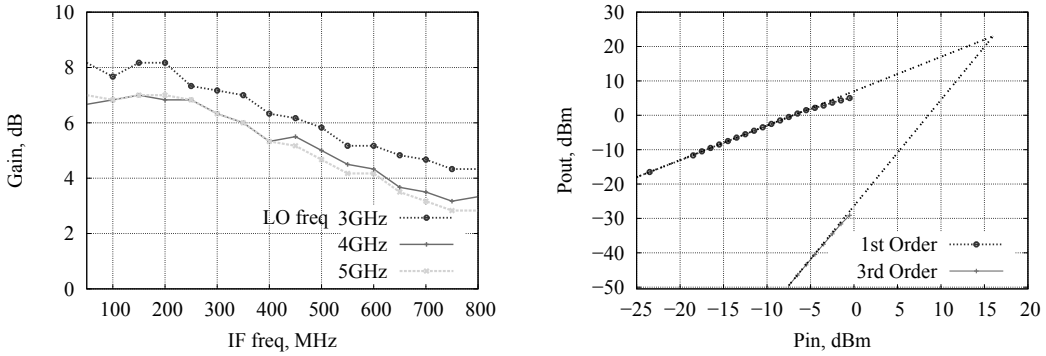


Figure 6.13: Simplified schematic of an IQ mixer ($T_{1,2}$ = shp×16, T_{3-10} = shp×4, T_{11} = shp×8 (see Tab. 4.1))

The measured conversion gain is shown in Fig. 6.14(a): at 250 MHz IF frequency, a conversion gain of 7-8 dB was achieved for the LO frequency from 3 to 5 GHz. The 1-dB input compression point of RF at f_{LO} = 4 GHz and f_{IF} = 200 MHz is -2 dBm. The RF IIP_3 is 16 dB as shown in Fig. 6.14(b). The power

consumption of the mixer is 68 mW.



(a) (b)

Figure 6.14: (a) Voltage conversion gain and (b) Linearity (f_{LO} = 4 GHz, f_{IF} = 200 MHz) of the IQ demodulator

VGA

The VGA is implemented based a common emitter differential amplifier with variable emitter degeneration values. The simplified schematic of the VGA is shown in Fig. 6.3. The degeneration is realized using the on-resistance R_C of the CMOS switch N_2. The gate voltage of N_2 is controlled through a programmable resistor R_X.

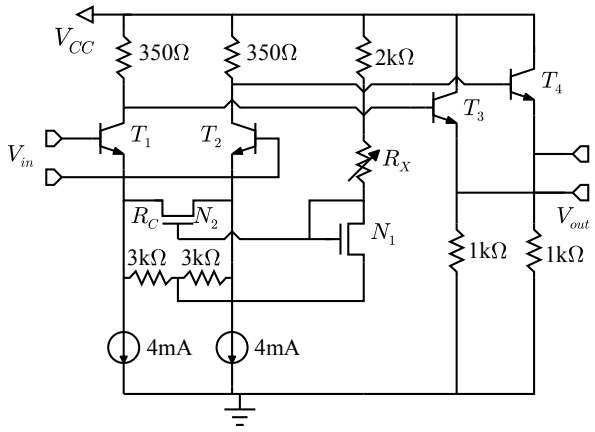
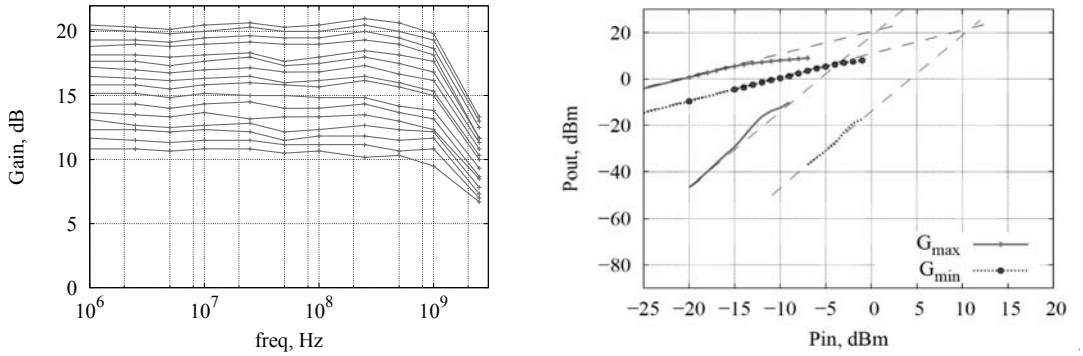


Figure 6.15: Simplified schematic of the variable gain amplifier ($T_{1,2}$= MV8×2, $T_{3,4}$= MV4×2, $N_{1,2}$:w = 10 µm, l = 240 nm)

The measured VGA gain is shown in Fig. 6.16(a), which varies from 10 to 21 dB in steps of 0.7 dB. The linearity of the VGA at 100 MHz is shown in Fig. 6.16(b).

At the maximum gain state, the input 1 dB compression point is -13 dBm and the IIP_3 is 1 dBm; at the minimum gain, the input 1 dB compression point is -2 dB, and the IIP_3 is around 12 dBm. The power consumption of the VGA is 45 mW.



(a) (b)

Figure 6.16: (a) Measured gain of the VGA (b) Linearity of the VGA at maximum and minimum gain at 100 MHz

Channel Select Filter

The channel select filter is implemented using a 4^{th} order active RC low pass filter with a multiple feedback Butterworth topology as shown in Fig. 6.17. The operational amplifiers designed in CMOS have a DC gain of 23 dB and a bandwidth of 600 MHz. Since the filter is placed after the LNA and VGA in the receiver chain, the noise behaviour of the filter is not critical. The bandwidth is reconfigurable with 4 specified bandwidths. The resistor and capacitor values for the filter are listed in Table. 6.5.

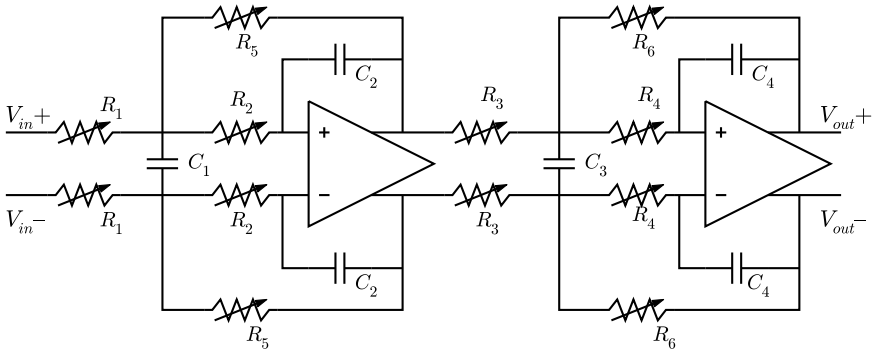


Figure 6.17: Simplified schematic of a channel select filter

The measured frequency response of the filter is shown in Fig. 6.18, which achieved 4 tunable bandwidths: 65, 97, 130 and 210 MHz. In the pass band, the

Table 6.5: Resistor and capacitor values for the channel select filter

Capacitance	**pF**	**Resistance**	Ω
C_1	1.2	R_1	720 - 4K
C_2	0.135	R_2	360 - 2K
C_3	4	R_3	300 - 1.7K
C_4	0.45	R_4	150 - 850
		R_5	1.1K- 5.5K
		R_6	400 - 2.2K

filter has 1 dB attenuation for all the 4 tunable bands. The out of band rejection in the first alias is 32, 29, 28 and 27 dB respectively. The power consumption of the filter is 160 mW.

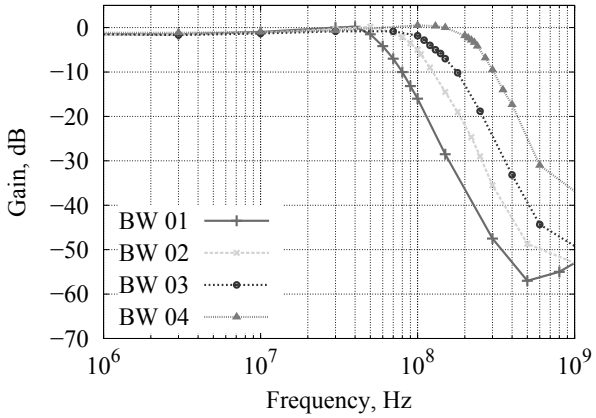


Figure 6.18: Measured gain of the channel select filter

The key performance of the sub blocks including gain, noise figure and linearity is summarized in Tab. 6.6.

Table 6.6: Summaries of the key parameters of the sub circuits of the receiver

Parameters	LNA	Mixer	VGA_{MAX}	Channel Filter
Gain (dB)	16	7	21	-1
NF (dB)	1.5	8.5	4.5	25-30
IIP_3 (dBm)	7	16	1	23

The reconfigurability is focused on the variation of the operating frequency band, the receiver gain, and the bandwidth of the baseband, which were real-

ized by the wideband frequency synthesizer, the VGA and the channel select filter respectively. The components and techniques which were used for the reconfigurable designs include RF-NMOS switches, variable capacitors and bias adjustment through a digital controlled bus and D/A converters [88].

3-wire SPI slave registers, designed by IHP Microelectronics, were implemented together with the receiver to configure the on chip operating parameters. The SPI slave has 32 bits, realized using four 8-bits registers. In this design, 17 bits were used for the receiver configuration; 1 read bit was used to indicate the PLL locking status. The functions of the control bits are listed in Table 6.7 [89]. The SPI master was from a commercial USB to SPI adaptor.

Table 6.7: Functions of the SPI control bits

Bit Counts	**Functions**
4	Variable gain
2	Variable channel bandwidth
1	VCO core selection
4	Prescaler
2	Multi-ratio frequency divider
4	PLL loop bandwidth optimization
1	PLL lock indication

The chip micrograph is shown in Fig. 6.19 with a chip area of 2×1.3 mm^2. The LNA, as the most noise sensitive block, is placed on the top right corner of the layout. The noisy digital blocks were placed at the bottom left of the layout and isolated from the RF blocks using guard rings. The chip was packaged in a $5\times5\times0.9$ mm^3 QFN32 package with a thermal ground pad of 3.1×3.1 mm^2 as shown in Fig. 6.20(a). The bonding diagram is shown in Fig. 6.20(b).

The packaged chip was mounted on a Rogers 5880 substrate with an FR4 carrier designed as the test board as shown in Fig. 6.21 with a size of 65×50 mm^2.

The voltage supply for the dividers, LNA, Mixer, channel select filter and the digital block is 3.3 V, and 5V for the VGA. The VCO is supplied with 5.5 V and the active loop filter is supplied with 6 V. Power management blocks were designed on the test board to generate multi-voltages to supply difference sub circuit blocks. The complete board is supplied with 6 V and the current consumption is 390 mA.

Before the characterization of the receiver performance, the first step is to obtain the stabilized LO signals. An external coarse tuning is added to the VCO to optimize the phase noise performance. The value of the external tuning voltage

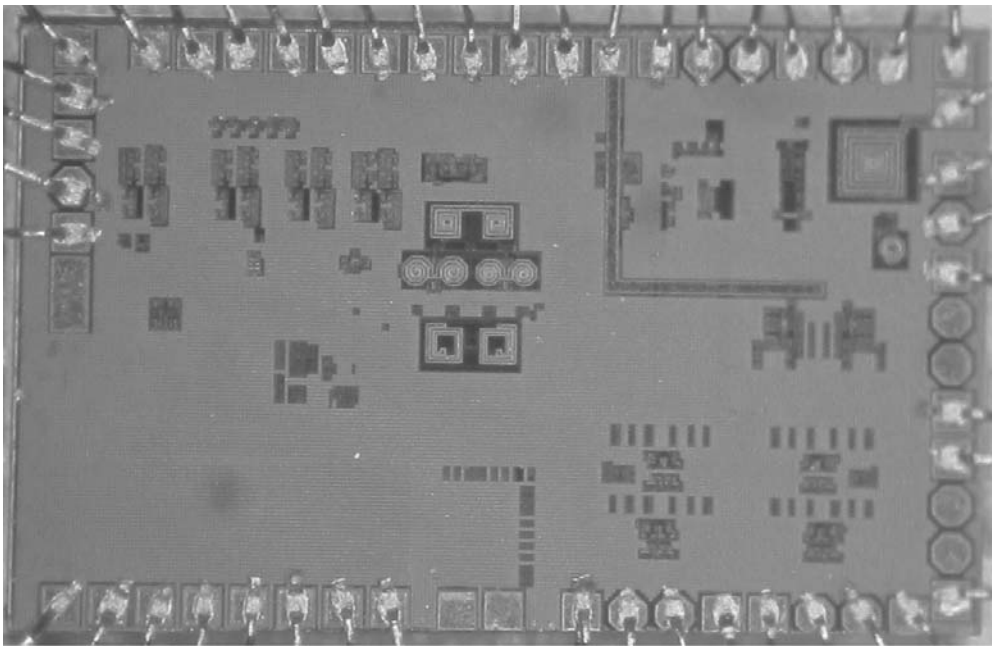
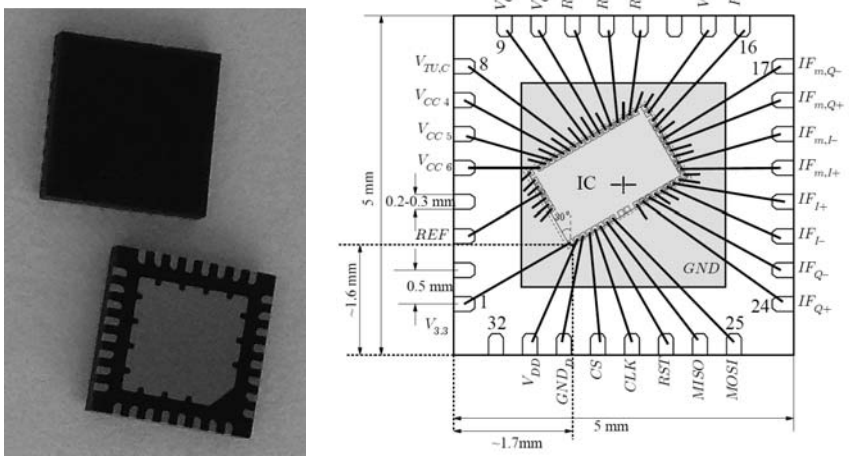


Figure 6.19: Chip micrograph of the 3 to 5 GHz receiver frond-end. The die size is 2×1.3 mm^2



(a) (b)

Figure 6.20: (a) Chip photo of the packaged 3-5 GHz reconfigurable receiver (b) Bonding diagram of the reconfigurable receiver chip for packaging

needs to be pre-characterized at each LO frequency. In future work, the coarse tuning can also be realized using on chip integrated digital-to-analog converters and configured by the 3-wire interface. At f_{LO} = 4 GHz, the phase noise of the 40 MHz IF signal is shown in Fig. 6.22, after adjusting the loop filter parameters as discussed in the last section.

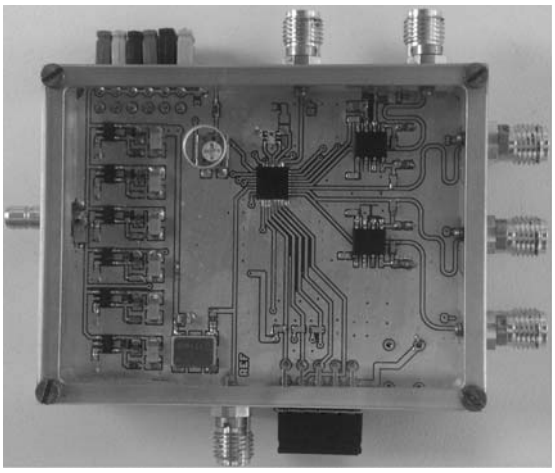


Figure 6.21: Evaluation board of the receiver frond-end

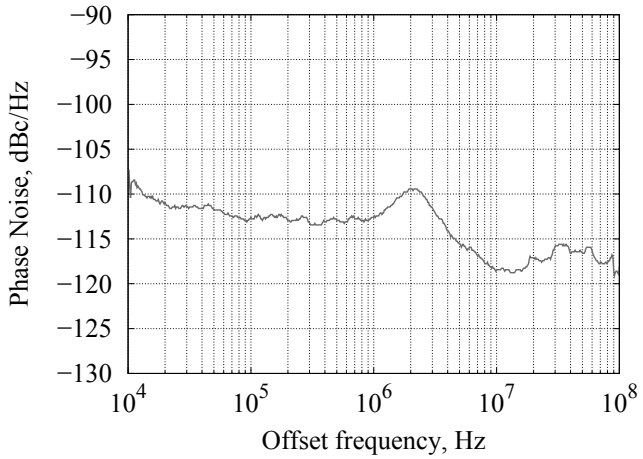
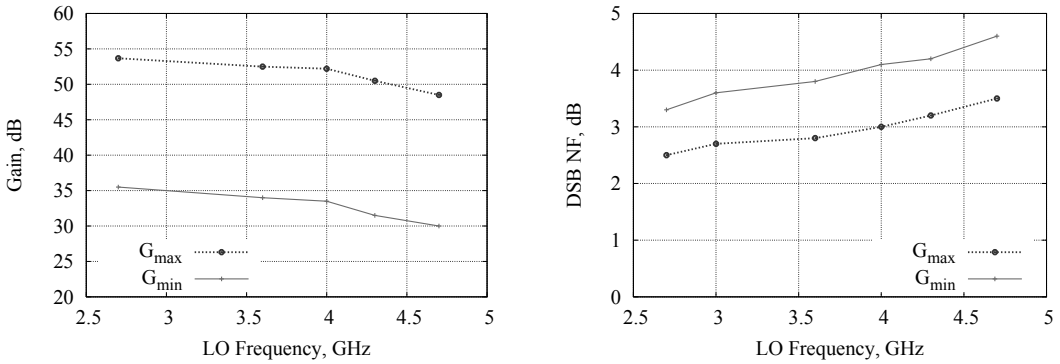


Figure 6.22: Phase noise of the 40 MHz IF at the receiver output, f_{LO} = 4 GHz (data was accessed from previous test board with non-packaged chip).

The measured receiver gain performance is shown in Fig. 6.23(a). For example, at 4 GHz LO and 50 MHz IF frequency, the gain varies from 34 to 52 dB. The Double Side Band (DSB) noise figure of the receiver is shown in Fig. 6.23(b). The noise performance degrades around 1 dB when the receiver gain is changed from maximum to minimum.

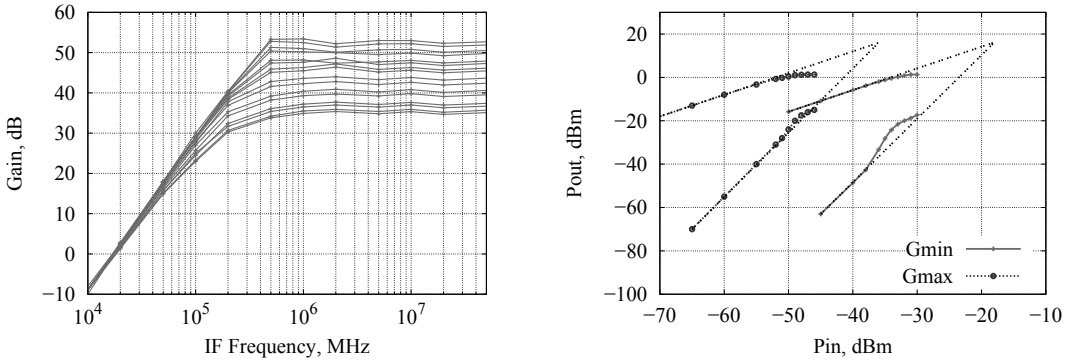
The measured variable gain behavior of the receiver is shown in Fig. 6.24(a), the DC and low frequency signals are attenuated through an off-chip DC offset cancellation unit. The linearity of the receiver is shown in Fig. 6.24(b). The IIP_3 is -36 dBm for maximum gain, and -18 dBm for minimum gain.

Fig. 6.25(a) and 6.25(b) shows the measured receiver gain at different channel select filter bandwidths with maximum and minimum gain at 4 GHz LO frequency. At maximum gain, the 3 dB bandwidth is around 60, 85, 105, 150 MHz; at min-



(a) (b)

Figure 6.23: Measure receiver (a) gain and (b) DSB noise figure at 50 MHz IF frequency

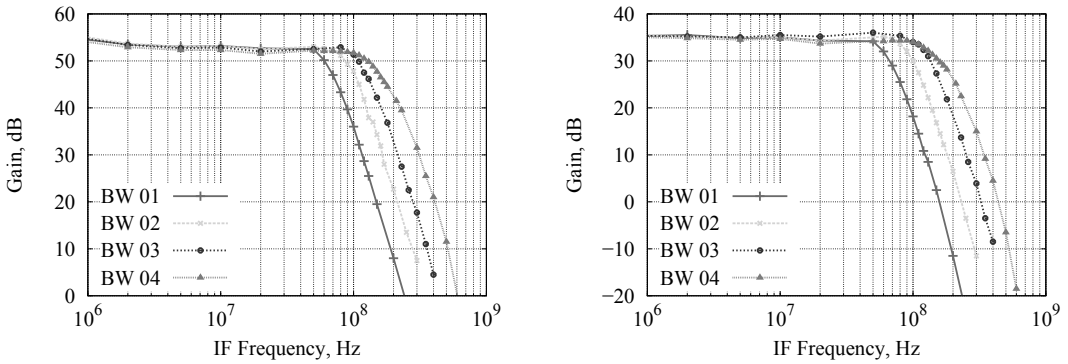


(a) (b)

Figure 6.24: (a) Receiver gain with variable gain steps and DC-offset cancellation at $f_{LO} = 4$ GHz (b) Linearity at maximum and minimum gain at $f_{RF,1} = 4.05$ GHz, $f_{RF,2} = 4.06$ GHz

imum gain, the bandwidth is around 60, 90, 105, 130 MHz. Comparing with the performance of the channel select filter, the bandwidth of the receiver is decreased especially at higher frequency bands. This is mainly caused by the parasitics on the testing board.

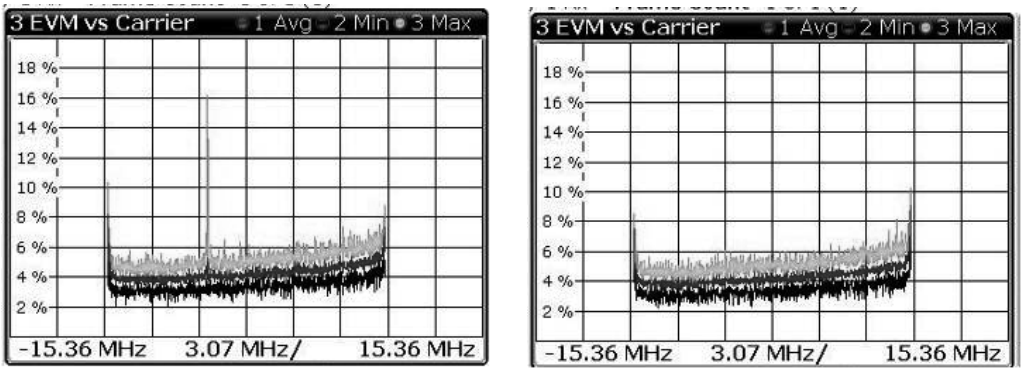
EVM (Error Vector Magnitude) is one of the most important figure of merits to characterize the performance of wireless communication systems. EVM offers insightful information about the transceiver such as phase noise, IQ mismatch, non-linearity, LO leakage, thermal noise and so on. The EVM measurement of this receiver was performed in the laboratory in Ericsson AB (Department EAB/FJB/RLA, Stockholm), using a test bench for a base station receiver at 20 MHz LTE channel bandwidth for the 4^{th} generation mobile communication sys-



(a) (b)

Figure 6.25: Measured receiver gain at different channel select filter filter bandwidths with (a) Maximum gain and (b) Minimum gain, $f_{LO} = 4$ GHz

tems. The EVM for LTE base station applications was specified below 9% for PDSCH (Physical Downlink Shared Channel) under modulation scheme 64QAM [90]. The measurement results (Fig. 6.26(a) 6.26(b) [91]) show that this receiver has a EVM value of around 4% (64QAM) and it is qualified for 4G base station applications.



(a) (b)

Figure 6.26: EVM measurement of the 3-5 GHz receiver, 20 MHz downlink LTE channel, channel select filter is set to (a) 150 MHz (b) 60 MHz and full IF-gain

7

Conclusions

In this thesis, fully integrated solutions for LO signal generation in wireless communication systems for microwave and millimeter wave applications have been achieved in a 0.25 μm SiGe BiCMOS technology SG25H3 from IHP Microelectronics. A novel dual-loop PLL topology was investigated, which achieved ultra low phase noise and fast locking simultaneously. The performance of the proposed PLL is superior than the conventional digital PLLs. The key parameters for PLL designs were analyzed in terms of frequency range, frequency resolution, phase noise, spurious tones and lock time.

The sub block designs including phase frequency detectors, VCOs, frequency dividers, loop filters and so on were discussed in detail:

A mixer type phase detector was designed with an operating speed up to 2 GHz and a phase noise of -157 dBc/Hz at 1 MHz offset. A 3-state phase frequency detector was designed in a CMOS technology, which had a low power consumption of 3.3 mW.

Several static frequency dividers were designed, which covered the frequency range from 200 MHz to 60 GHz; the trade-off between the operating speed and the power consumption was analyzed. A ÷2 dynamic frequency divider was designed; it had higher speed than static types under the same technology. A ÷3 semi-dynamic frequency divider was also designed, with input frequency range from 12 to 57 GHz. A ÷16-31 prescaler was designed with an input frequency range up to 7 GHz, which is suitable for fractional-N PLL designs. A multi-ratio frequency divider was also realized, with an output frequency range from 0.83 to 8 GHz.

Methods to optimize the Colpitts type VCO were discussed; a 35 GHz Colpitts VCO was designed with a frequency tuning range from 32.8 to 39.33 GHz and a phase noise of below -90 dBc/Hz at 1 MHz offset. A 16 to 24 GHz dual-core VCO was realized using switchable resonator cores, which achieved a frequency tuning

range of 40% and a phase noise of below -100 dBc/Hz at 1 MHz offset; the chip area was optimized to 0.1 μm^2.

The PLL was simulated and optimized at a system level. Based on the intrinsic phase noise performance of the individual sub blocks, a proper designed loop bandwidth optimized the overall phase noise performance of the phase locked hold loop. The restriction of the lock time by the loop bandwidth and pull-in range was relaxed by switching to the frequency acquisition loop in the pull-in process.

Three demonstrators were implemented. A 35 GHz dual-loop PLL with 6.9 GHz tuning range, a ultra-low phase noise of -106 dBc/Hz at 1 MHz offset and a lock time of less than 0.1 μs. The PLL achieved the-state-of-the-art performance in terms of phase noise and locking speed. A 16 to 24 GHz frequency synthesizer was designed with reconfigurable loop parameters and a phase noise below -106 dBc/Hz at 1 MHz offset. By adding a multi-ratio frequency divider at the 16 to 24 GHz PLL output, a continuous frequency sweep from 3 to 5 GHz was realized for the LO signals of a wideband direct down-conversion reconfigurable receiver with an EVM value of around 4% under modulation scheme 64QAM. The receiver was the first ever reported receiver with wideband (3-5 GHz) continuous LO generation units fully integrated on chip. It was qualified for the 4G base station applications.

Different voltage supply values were used for the sub blocks in the design, in order to achieve the optimum output power, linearity or frequency range. Multiple voltage regulators or charge pumps are required, which reduce the power efficiency. In future work, the trade-off between the power efficiency and the other parameters such as frequency range, chip area and so on needs to be further investigated. Instead of generating a wide tuning voltage range (1 to 6 V) for the VCOs, VCOs with multiple resonator cores can be implemented to increase the frequency tuning range. To achieve a finer frequency step size for the frequency synthesizer, a sigma delta modulator using the CMOS provided by the technology shall be studied. The trade-offs among the speed, power consumption of the sigma delta modulator and the comparison frequency of the PLL need to be investigated.

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Appendix A

List of Symbols

Symbol	Units	Description
A_E	μm^2	Emitter area of a transistor
BV_{CEO}	V	Transistor breakdown voltage at the Collector-Emitter with open base
BV_{CEO}	V	Transistor breakdown voltage at the Collector-Base with open emitter
$\Delta\omega_0$	rad	Initial frequency error of the PLL
f_{comp}	Hz	Comparison frequency of the PLL
f_{in}	Hz	Input frequency of the frequency divider
f_{LO}	Hz	Frequency of the local oscillator
f_{max}	Hz	Maximum oscillation frequency of a transistor
f_{ref}	Hz	Frequency of the reference
f_T	Hz	Transient frequency of a transistor
f_{VCO}	Hz	Frequency of the VCO
f_0	Hz	Center frequency of a VCO, no external tuning voltage applied
$G, G(s)$	-	Open loop gain of the PLL
G_{filter}	-	Open loop gain of the loop filter
H	-	Feed back factor of the PLL
I_B	mA	Base current of a transistor
I_C	mA	Collector current of a transistor
I_{ee}	mA	DC current of a common emitter differential amplifier
I_{cp}	mA	Output current of a charge pump
K_Φ	$V \cdot rad^{-1}$	Gain of the phase detector
K_{VCO}	$rad \cdot s^{-1} V^{-1}$	Frequency tuning gain of the VCO
$L(\Delta\omega)$	dBc/Hz	Phase noise of an oscillator
N, R	-	Frequency divider ratio
NF_{min}	dB	Minimum Noise Figure
P_{VCO}	Hz	Power of the VCO signal
P_{ref}	Hz	Power of the reference signal
PN_{PLL}	dBc/Hz	Phase noise of the PLL
PN_{Ref}	dBc/Hz	Phase noise of the reference signal

PN_{PD}	dBc/Hz	Low frequency noise of the phase detector
PN_{Flt}	dBc/Hz	Phase noise of the loop filter
PN_{Div}	dBc/Hz	Phase noise of the frequency divider
PN_{VCO}	dBc/Hz	Phase noise of the VCO
ϕ_{VCO}	rad	Phase of the VCO signal
ϕ_{ref}	rad	Phase of the reference signal
ϕ_{error}	rad	Phase error of the PLL
$\phi_{error,max}$	rad	Maximum phase error of the PLL
Q_L	-	Load quality factor of a resonator
Q_U	-	Unload quality factor of a resonator
S_{I_B}	A^2Hz^{-1}	Flicker current noise at the base of a transistor
S_{I_C}	A^2Hz^{-1}	Flicker current noise at the collector of a transistor
T_P	s	Pull-in time
T_L	s	Lock-in time
τ_1, τ_2, τ_3	s	ime constant of the loop filter
V_{CC}	V	Supply voltage of the circuit with BJTs
V_{CE}	V	Collector emitter voltage of a transistor
V_H	V	Voltage at logic high
V_L	V	Voltage at logic low
V_{Tune}	V	Tuning voltage of the VCO
V_{error}	V	Error voltage at the phase detector output
ω_c	$rad{\cdot}s^{-1}$	Loop bandwidth of the PLL
ω_n	$rad{\cdot}s^{-1}$	Natural frequency of the PLL feed back loop
ω_0	$rad{\cdot}s^{-1}$	Initial offset frequency of the VCO signal

Appendix B

Abbreviations

APLL	Analog Phase Locked Loop
BiCMOS	Bipolar junction and CMOS transistor
CMOS	Complementary Metal-Oxide-Semiconductor
DDS	Direct Digital Synthesizer
DECT	Digital Enhanced Cordless Telecommunications
DL	Down Link
DLL	Digital Locked Loop
DPLL	Digital Phase Locked Loop
ECL	Emitter Coupled Logic
EM	Electro-Magnetic
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
E-UTRA	Evolved Universal Terrestrial Radio Access
EXOR	EXclusive OR
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FMCW	Frequency-Modulated Continuous-Wave
HBT	Hetero-junction Bipolar Transistor
HSPA	High Speed Packet Access
IF	Intermediate frequency
IIP_3	Third-order Input Intercept Point
IQ	In-phase and Quadrature
LNA	Low Noise Amplifier
LO	Local Oscillator
LTE	Long Term Evolution
MASH	Multi-Stage Noise Shaping
MEMS	MicroElectroMechanical Systems
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
OFDM	Orthogonal Frequency-Division Multiplexing
PA	Power Amplifier

PD	Phase Detector
PDSCH	Physical Downlink Shared Channel
PED	Phase Error Detector
PFD	Phase Frequency Detector
PI	Proportional Integral
PLL	Phase Locked Loop
Q factor	Quality factor
RF	Radio Frequency
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SSB	Single Side Band
TFMSL	Thin-Film Micro-Strip Line
UL	Up Link
UMTS	Universal Mobile Telecommunications System
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
XTAL	Crystal Oscillator
YIG	Yttrium Iron Garnet

Appendix C

Pin Descriptions

Table C.1: Pin description of the 35 GHz dual-loop PLL

Name	**Pin Description**
REF	PLL reference signal input
$VCO+$	PLL RF output, positive
$VCO-$	PLL RF output, negative
$LOCK$	Phase locked indication signal output
VCC_1	Power supply for PD; frequency dividers, 3.3 V
VCC_2	Power supply for the active loop filter, 7.5 V
VCC_3	Power supply for the VCO, 6.5 V
GND	Analog ground
VDD_1	Power supply for the PFD and other digital blocks, 3.3 V
$DGND_1$	Digital ground
VDD_2	Guard ring power supply, 3.3 V
$DGND_2$	Guard ring ground

Table C.2: Pin description of the 16 to 24 GHz frequency synthesizer

Name	**Pin Description**
REF	PLL reference signal input
$VCO+$	PLL RF output, positive
$VCO-$	PLL RF output, negative
$VTUNE$	Coarse tuning voltage of the VCO
BSL	Band select control of the VCO, 0: 16-20 GHz, 1: 20-24 GHz
$LOCK$	Phase locked indication signal output
$D_{3:0}$	4 bits programmable frequency divider control
P_{R1}, P_{R2}	2 bits bandwidth control, resistive
P_{C1}, P_{C2}	2 bits bandwidth control, resistive
VCC_1	Power supply for PD; frequency dividers, 3.3 V
VCC_2	Power supply for the active loop filter, 7.5 V
VCC_3	Power supply for the VCO, 6.5 V
GND	Analog ground
VDD_1	Power supply for the PFD and other digital blocks, 3.3 V
$DGND_1$	Digital ground
VDD_2	Guard ring power supply, 3.3 V
$DGND_2$	Guard ring ground

Table C.3: Pin description of the 3 to 5 GHz direct down conversion receiver

Name	**Pin Description**
REF	PLL reference signal input
GND	Analog ground
V_{CC6}	Power supply for PLL loop filter
V_{CC5}	Power supply for frequency divider
V_{CC4}	Power supply for VCO
$V_{TU,C}$	Coarse tuning voltage of the VCO
V_{CC3}	Power supply for channel select filter
V_{CC2}	Power supply for Mixer and VGA
RF_{IN+}	RF input of the demodulator
RF_{IN-}	RF input of the demodulator
RF_{OUT}	RF output of the LNA
V_{CC1}	Power supply for LNA
RF_{IN}	RF input of the LNA
$IF_{m,I+}$	IF output of the demodulator
$IF_{m,I-}$	IF output of the demodulator
$IF_{m,Q+}$	IF output of the demodulator
$IF_{m,Q-}$	IF output of the demodulator
IF_{I+}	IF output of the channel select filter
IF_{I-}	IF output of the channel select filter
IF_{Q+}	IF output of the channel select filter
IF_{Q-}	IF output of the channel select filter
$MOSI$	SPI aster output slave input
$MISO$	SPI master input slave output
RST	SPI reset
CLK	SPI clock
CS	SPI chip select
$V_{3.3}$	Power supply for digital blocks
V_{DD}	Power supply for SPI
GND_D	Digital ground

Appendix D

List of Publications

- Xiaolei Gai, Trasser A., Schumacher H. A Fully Integraged Low Phase Noise, Fasting Locking, 31 to 34.9 GHz Dual-Loop PLL, 2011 European Microwave Integrated Circuits Conference (EuMIC), Manchester, UK, 10-11, Oct. 2011, pp. 648-651

- Xiaolei Gai, Chartier, S., Trasser, A., Schumacher, H. A 35 GHz Dual-Loop PLL with Low Phase Noise and Fast Lock for Millimeter Wave Applications. 2011 IEEE MTT-S International Microwave Symposium Digest (IMS), Baltimore, US, 5-10 Jun. 2011, pp. 1-4

- Xiaolei Gai, Liu G., Chartier S., Trasser A., Schumacher H. A PLL with Ultra Low Phase Noise for Millimeter Wave Applications, Proceedings of 40th European Microwave Conference (EuMC 2010), Paris, France, 28-30, Sep. 2010, pp. 69-72

Parts of this dissertation have been published in the following article:

- Xiaolei Gai, Chartier, S., Trasser, A., Schumacher, H. A 35 GHz Dual-Loop PLL with Low Phase Noise and Fast Lock for Millimeter Wave Applications. 2011 IEEE MTT-S International Microwave Symposium Digest (IMS), Baltimore, US, 5-10 Jun. 2011, pp. 1-4

Curriculum vitae

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