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Pseudomorphic and metamorphic HEMT-technologies for industrial W-band low-noise and power applications

DISSERTATION

zur Erlangung des akademischen Grades eines

DOKTOR-INGENIEURS
(DR.-ING.)

der Fakultät für Ingenieurwissenschaften
und Informatik der Universität Ulm

von

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Ulm, 14. Dezember 2009

This work has been prepared from January 2001 to March 2009 at United Monolithic Semiconductors GmbH, and the University of Ulm, department of electron devices and circuits.

Parts of this work have already been published:

J. Grünenpütt, C. Gässler, D. Geiger, R. Deufel, C. Woelk, E. Kohn, "Selective double recess technology on metamorphic HEMTs improving the on-state breakdown behavior", Technical Digest CS-MAX, San Jose, CA, Nov 2002

A. Bessemoulin, C. Gaessler, J. Gruenenpuett, B. Reig, "Hot via-interconnects: A Step towards Surface Mount Chipscale Packaged MMICs up to 110GHz", Technical Digest: 26^{th} IEEE CSIC Symposium, Monterey, Oct. 2004

J. Gruenenpuett, C. Gaessler, C. Gaquière, E. Kohn, "800mW/mm power density @ 94GHz for a 70nm-pHEMT technology", Technical digest CS-MAX04, Monterey, Oct. 2004

A. Bessemoulin, J. Gruenenpuett, P. Fellon, A. Tessmann, E. Kohn, "Coplanar W-Band Low Noise Amplifier MMIC Using 100-nm Gate-length GaAs PHEMTs", 12^{th} GaAs Symposium - Amsterdam, Oct. 2004

A. Bessemoulin, P. Fellon, J. Grünenpütt, A. Tessmann, H. Massler, W. Reinert, E. Kohn, "High gain 110GHz Low Noise Amplifier MMICs using 120-nm Metamorphic HEMTs and Coplanar Waveguides", 13^{th} GaAs European Microwave Week, 2005

C. Gaquière, J. Grünenpütt, D. Jambon, E. Delos, D. Duccatteau, M. Werquin, D. Théron, P. Fellon , "A High Power W-Band Pseudomorphic InGaAs Channel PHEMT", IEEE Electron Device Letters, vol. 26, Aug. 2005, pp. 533–534

Pseudomorphic and metamorphic HEMT-technologies for industrial W-band low-noise and power applications

Abstract: The W-band ranging from 75 to 110 GHz marks a frequency window of low atmospheric absorption which is suited for high bandwidth data transmission but also for radar applications. Especially the 94 GHz absorption minimum is used for cloud profiling radars to detect rain from satellites. Active radar systems are found for traffic control on runways but also to identify debris as a severe danger to the safety and integrity of aircrafts. Multi channel passive radar imaging allow the detection of concealed weapons at security gates. With an increased demand for such security systems there is a growing market for W-band low noise and power amplifiers to be addressed by industry.

Up to 77 GHz integrated circuits are realized by commercial 150 nm gate length pseudomorphic high electron mobility transistors (pHEMT). To address higher frequency levels, the active devices have to provide more gain. The development and fabrication of such devices are part of this work, where fabrication processes have to be compatible with the 4"-fabrication environment of United Monolithic Semiconductors including the industry requirements regarding fabrication yield and device reliability. Besides the progression of the pHEMT technology by down scaling of the gate length to 80 nm, two single recess and one double recess metamorphic HEMT technology on GaAs substrate have been developed to improve the RF-gain by the superior transport properties of the low bandgap $In_xGa_{1-x}As$ channel. A channel indium concentration of 60 % and 43 % has been investigated for device optimization depending on the application such as low-noise and power.

After a general discussion of the pseudomorphic and metamorphic HEMT structures including the gate recess configuration and device breakdown, the fabrication modules and optimizations referring to the particular technology are presented with respect to reproducibility and fabrication yield. An acceptable wafer fabrication yield of 73 % with good prospectives for further improvement has been realized for the pHEMT technology. The fabrication yield of 26 % for the metamorphic low-noise technology is low and does not comply with the production requirement of 60 %. MESA-isolation in combination with device passivation at temperatures above 250°C has been identified to be responsible for the low yield and requires further optimization.

The 120 nm low-noise metamorphic HEMTs show a transit frequency of 200 GHz and a maximum oscillation frequency around 300 GHz. The associated gain of 5.4 dB at 94 GHz with a noise figure of 3 dB is in line with institute results for well passivated devices. Several low-noise demonstrator amplifiers are presented providing a gain of 6 dB per stage at 94 GHz with noise figures around 4.5 dB. Similar performances have been demonstrated by a two-stage common source low noise amplifier fabricated with the pseudomorphic HEMT technology. Although not optimized for low-noise the pHEMT demonstrator had even the lower noise figure of 3.7 dB.

The metamorphic power technology provides state-of-the-art performance with a power density of 380 mW/mm at 94 GHz and a linear gain of 8.5 dB for 3 V operation. Despite a high off-state breakdown voltage above 10 V, the devices cannot be operated at

higher voltage levels due to impact ionization related device burn-out. The pseudomorphic HEMT technology is less sensitive towards impact ionization because of the higher bandgap in the channel. Although the off-state breakdown voltage of the pseudomorphic HEMT of 6.5 V is considerably low, the devices can be operated up to 4.5 V and demonstrate state-of-the-art output power densities up to 900 mW/mm at 94 GHz. Together with a linear gain of 10 dB, the pseudomorphic HEMT technology provides the better RF-power performance compared to the metamorphic power HEMTs and was selected for non-linear modeling and demonstrator design. Three-stage power amplifiers have been fabricated providing a maximum output power of 180 mW at 94 GHz with a linear gain of 11 dB for 3.5 V operation.

Due to the limitation of the gate length to 120 nm for the 3-layer resist gate technology, the metamorphic HEMT technology could not demonstrate its whole potential regarding RF-gain and noise figure. As a consequence of the high yield fabrication, superior power performance at 94 GHz, and similar or even better low-noise properties the industrialization of the 80 nm pseudomorphic HEMT technology started at United Monolithic Semiconductors to provide low noise and power amplifiers for the next generation of W-band applications. However, to target for even higher frequencies, further investigations have to be performed on the metamorphic devices for reduced gate length and improved fabrication yield.

Contents

1 Introduction

Over decades, the progress in millimeter wave semiconductor technologies has been strongly driven by military requests [1]. However, also an increasing number of wireless civil applications such as telecommunication-, sensor- and navigation-systems require more and more low-noise and power devices at high frequencies up to 100 GHz. Considering the atmospheric attenuation spectrum in figure 1.1, there is higher damping of millimeter waves for increasing frequencies. Absorption peaks at 24 GHz, 180 GHz and 330 GHz are related to the vapor content in air; at 60 GHz and 120 GHz absorption is caused by interaction with O_2 molecules. Atmospheric properties provide windows for long-range transmission (e.g. at 35, 94, 140 and 220 GHz) and narrow highly damped frequency bands that are suited to short-range use (e.g. at 24 GHz or 60 GHz) [2, 3]. The impact of the weather situation on the absorption characteristics can be used for meteorological investigations. At frequencies of low attenuation, below 20 GHz, there are X- and Ku-band satellite communication as well as far reaching radar systems. Generally, the strong impact of climate conditions has to be regarded as a limitation of the bandwidth for data transmission; the range of a radar gets reduced. Rain fade on the other hand can be used for radar assisted weather monitoring. The absorption peaks, especially at 24 GHz are helpful to realize short range radar systems as used for automotive parking assistants or pre crash detection. Higher frequencies allow more band-width for data transmission and increased radar accuracy. At W-band (75 GHz to 110 GHz), there is an atmospheric window of low attenuation allowing multi gigabit short distance communication, radar assisted automotive cruise control (77 GHz) and high resolution millimeter wave radar systems.

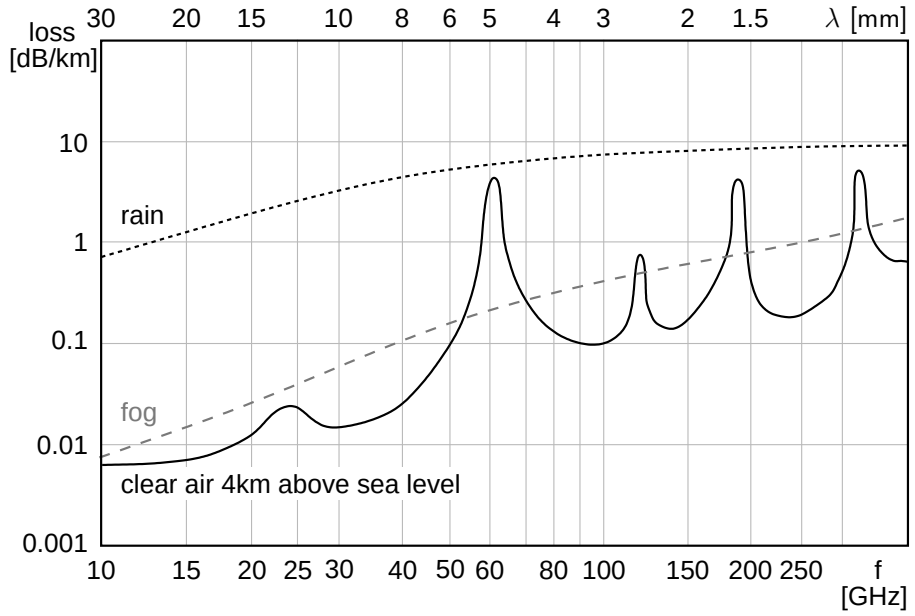


Figure 1.1: Attenuation (absorption) spectrum between 10 and 300 GHz (resp. 30 to 1 mm wavelength) in air [1] including attenuation by fog and rain [4].

At the 94 GHz absorption minimum, cloud profiling radars [3] allow the detection of rain from satellites. Active radar imaging is used at airports for traffic control on runways but also to identify debris, a severe danger to the safety and integrity of aircrafts [5]. Since most wall materials are transparent for millimeter waves, active radar imaging systems are suited for observation but also for rescue activities to search for people hidden in concealed rooms of collapsed buildings. Passive radar imaging systems [6] demonstrate non-intrusive people screening at security portals e.g. of an airport. Based on a high millimeter wave absorption of the human skin, concealed weapons that typically strongly reflect can be identified even through several layers of clothing. Such passive systems need no active microwave source - reflected radiation is thermally emitted by the surroundings.
While passive millimeter wave imaging systems only need a high quality low noise amplifier, also a power amplifier is needed for the active version. Low-cost silicon technologies significantly improved high frequency properties during recent years. At high frequency level, however, either market volumes are too small for cost effective mass production or RF-performance such as noise figure and output power do not meet the requirements. These niche markets are addressed by III-V semiconductor technologies based on GaAs, InP and GaN, providing superior low-noise and RF-power performance. Up to 77 GHz, low noise amplifiers are realized by commercial 150 nm gate length pseudomorphic HEMTs (**H**igh-**E**lectron-**M**obility-**T**ransistor) on GaAs substrate [7]. To address higher frequency levels such as 94 GHz, the active device has to provide more gain. This is the target of this work. Furthermore, the new HEMT technologies (low-noise & power) have to comply with following conditions:

- compatibility to the 4" wafer area production facility
- modular device fabrication for high yield production
- minimum device breakdown of 4 V for the low-noise technology
- minimum device breakdown of 6 V for the power technology
- minimum device breakdown of 3 V for the turned-on power device

HEMT structures on InP substrate have demonstrated excellent RF-performance [8, 9, 10, 11] due to superior transport properties of the InGaAs quantum well. However, the InP-approach has been no option due the non-availability of 4"-wafers at the beginning of this work. Moreover, the high brittleness of the InP substrates is critical for automatic wafer handling which is frequently used in the pHEMT production line.

Alternatively, there is down scaling of the existing HEMT technology to a shorter gate length [12, 13] to improve the RF-gain. This option is highly compatible to existing UMS pHEMT technologies and has been considered in this work.

Metamorphic HEMT structures promise a combination of the benefits of a low bandgap $In_xGa_{1-x}As$ channel known from InP with less brittle 4" GaAs substrates [14, 15, 16]. Thanks to the metamorphic buffer, the indium concentration x for the channel gives some degree of freedom between 20 and 80 % [17]. This has been used to optimize the metamorphic devices regarding low-noise and power requirements.

1.1 Motivation

High-Electron-Mobility-Transistors are used in low-noise and power radio frequency applications due to their high electron mobilities and saturation velocities. In this work, band-gap engineering has been performed to optimize metamorphic and pseudomorphic HEMT-structures as roughly sketched in figure 1.2 for low-noise and power operation.

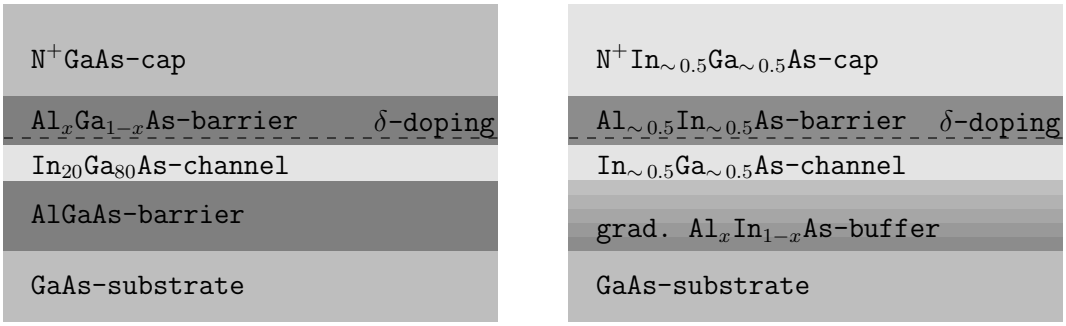


Figure 1.2: Sketch of pseudomorphic (l) and metamorphic (r) HEMT epitaxy structures.

The aim of this work is not to target for world record device performances linked to ultra-short gate length [18] but to develop production worthy pseudomorphic and metamorphic HEMT technologies for W-band low-noise and power applications providing state-on-the-art performance. Metamorphic HEMT technologies based on 100 nm and 70 nm gate length and an indium concentration of 65 and 80 % have demonstrated transit frequencies of 200 and 290 GHz with maximum oscillation frequencies of 280 and 340 GHz, respectively [19, 20, 21]. With this, cascode single stage LNA reached a linear gain of 10.5 dB at 94 GHz with a noise figure around 3 dB. By reduction of the indium content, a higher operation voltage and device breakdown has been realized for metamorphic power devices; a concentration of 43 % is found as a good compromise between output power and RF-gain [16]. For a gate length of 0.15 μm, a power density of 320 mW/mm with a power added efficiency of 28 % and a linear power gain of 6 dB have been reported at 95 GHz for a 150 μm device [22].

Table 1.1 gives a summary of all types of heterostructures used in this work including a rough rating with respect to the epitaxy quality. Indices indicate the location within the epitaxy sequence such as ΔE_{c_u} is linked to the conduction band discontinuity towards the upper barrier and similar for ΔE_{c_l} referring to the lower barrier. The growth of the epitaxial material was performed in solid source MBE-tools on semi-isolating GaAs substrates. The diameters of the wafers are 3” for material grown at the Daimler-Research Laboratory and 4” for wafers purchased from a commercial epitaxy supplier.

To target for low-noise applications, a 120 nm metamorphic HEMT technology has been developed in this work based on an indium concentration of 53 to 70 %; the grading allows to increase the conduction band discontinuity ΔE_{c_u} towards the barrier compared to a pure lattice matched structure for high charge density and RF-gain. Low-noise properties have been characterized in V- and W-band on device and MMIC level showing state-of-the art performance in chapter 6.

Regarding power applications, a double recess configuration on a metamorphic HEMT with a high indium content up to 60 % has been investigated in comparison to a single recess metamorphic HEMT based on 43 % channel indium content. Alternatively, a single recess pseudomorphic power HEMT technology with a down scaled gate length of 80 nm has been developed in this work. Power properties of the different technologies are compared at 94 GHz on device level. State-on-the art power amplifiers based on the pseudomorphic HEMT technology are presented in chapter 6.

application	low-noise	power		
type	metamorphic single recess	metamorphic double recess	metamorphic single recess	pseudomorphic single recess
supplier	4" commercial	3" Daimler-Research	4" commercial	4" commercial
$E_{g_u}(barrier)$	1.49 eV (47%Al)	1.74 eV (60%Al)	1.95 eV (65%Al)	1.74 eV (25%Al)
ΔE_{c_u}	0.64 eV	0.75 eV	0.77 eV	0.42 eV
ΔE_{v_u}	0.28 eV	0.32 eV	0.34 eV	0.2 eV
$E_{g_u}(channel)$	0.57 eV (70%In)	0.67 eV (60%In)	0.85 eV (43%In)	1.11 eV (25%In)
$\overline{E_g}(channel)$	0.66 eV (60%In)	0.76 eV (50%In)	0.85 eV (43%In)	1.11 eV (25%In)
$E_{g_l}(channel)$	0.74 eV (53%In)	0.85 eV (43%In)	0.85 eV (43%In)	1.11 eV (25%In)
ΔE_{c_l}	0.52 eV	0.63 eV	0.63 eV	0.42 eV
ΔE_{v_l}	0.23 eV	0.27 eV	0.27 eV	0.20 eV
$E_{g_l}(barrier)$	1.49 eV (47%Al)	1.74 eV (60%Al)	1.75 eV (57%Al)	1.74 eV (25%Al)
n_s	$4.1 \cdot 10^{12}\text{cm}^{-2}$	na	$\sim 2.2 \cdot 10^{12}\text{cm}^{-2}$	$2.2 \cdot 10^{12}\text{cm}^{-2}$
μ	$10000\,\text{cm}^2/\text{Vs}$	na	$\sim 6000\,\text{cm}^2/\text{Vs}$	$6000\,\text{cm}^2/\text{Vs}$
R_{sh}	100-120 $\Omega_\square$	(101 $\Omega_\square$)	100-120 $\Omega_\square$	100 $\Omega_\square$
homogeneity	good	poor	medium	excellent
roughness	~ 2 nm	~ 4 nm	~ 2 nm	smooth
reproducibility	R_{sh}-drift	na	R_{sh}-drift	good

Table 1.1: Properties of the epitaxy-structures used in this work.

2 Field Effect Transistor

The principles of unipolar active semiconductor devices, such as field effect transistors (FETs), are known since many years. Although patented first in 1925 by Julius Edgar Lilienfeld [23], research articles and devices were ignored by industry because of difficult control of electronic surface states. Further patents and descriptions of field effect transistors including the description of the first JFET based on pn-junction current control followed until 1945 [24, 25] before the official birth of the (bipolar)-transistor at Bell Labs on 23^{rd} December 1947 [26]. Five years later, first field effect transistors recognized by industry have been realized in 1953 by G.C. Dacey and I.M. Ross [27] gaining remarkable importance in semiconductor technology evolution. Today, digital signal processing found in CPUs and random access memory are dominated by silicon based MOSFET technologies. For analog radio frequency applications, however, compound semiconductor devices like High-Electron-Mobility-Transistors on GaAs substrates are found due to their superior microwave low-noise and power performance compared to Si-RFMOS.

2.1 Idea of the HEMT structure

High-Electron-Mobility-Transistors (HEMTs) represent a special type of Field-Effect-Transistors (FETs) deriving its name from a superior mobility of the majority charge carriers. Growth techniques like Molecular Beam Epitaxy (MBE) and Metal Organic Vapor Phase Deposition (MOCVD) allow an industrialized fabrication of semiconductor structures with optimized composition and high crystal quality. The control of semiconductor growth on an atomic scale is mandatory to define reproducible heterojunction structures between two semiconductor materials of different composition and interfaces within limitations like mechanical strain based on different lattice constants. Double heterojunctions are used to form a channel structure where electrons are guided within a two dimensional electron gas (2DEG). A cross section of the HEMT device is shown in 2.1 as a sketch and a SEM-image. For device operation, two voltage sources are required; one for the device supply at the drain contact (V_{DS}) and another one for charge control at the gate (V_{GS}). The highly doped cap layer is required to realize a good electron transfer from the drain and source contacts to the channel. To form the Schottky contact at the gate, the cap layer is removed by a recess that further has strong impact on device properties like the breakdown behavior discussed later.

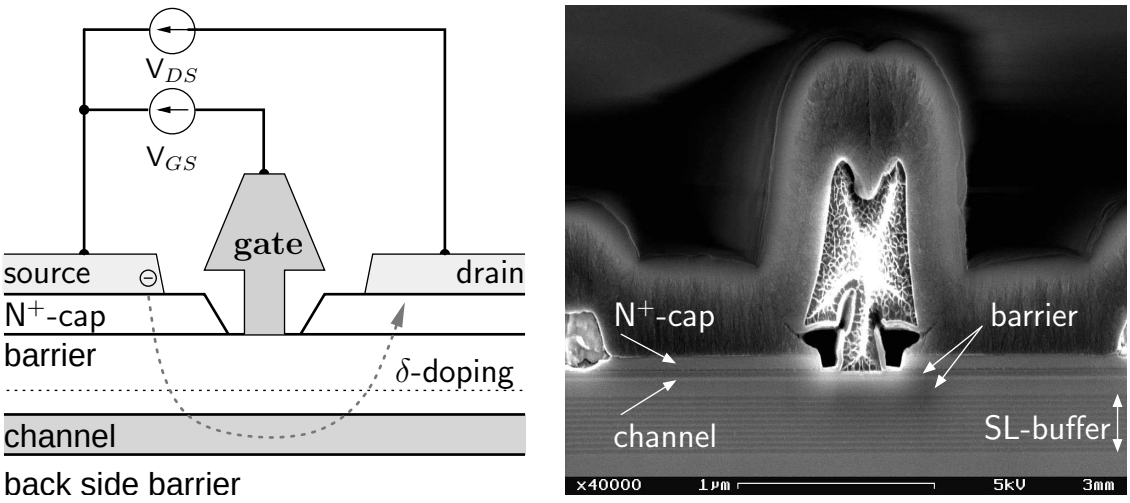


Figure 2.1: Sketch (l) and cross section SEM-image (r) of a HEMT.

The modulation of the charge density is realized by setting the energy level of the discrete states in the channel by V_{GS} with respect to the Fermi level. Such modulation of the 2DEG in GaAs-AlGaAs heterojunctions has been described first in 1979 by G. Abstreiter and K. Ploog [28] based on gate voltage dependent Raman-spectroscopy. Usually pulse doping outside the channel is preferred for charge supply allowing a separation in space between the activated donators and the 2DEG. This separation mainly helps to reduce Coulomb scattering as a noise source; for similar charge densities, the two dimensional electron gas shows superior electron mobilities compared to bulk electrons [29]. First applications of such field effect transistors were published in 1980 by T. Mimura [30] and D. Delagebeaudeuf [31, 32].

Following, the principles of the HEMT are discussed with respect to the pseudomorphic and metamorphic HEMT approach. A simple linear model is used to derive the charge density in the channel as a function of the gate voltage; non-linearities of the real device are discussed afterwards for low-noise and power application operation.

2.1.1 Charge control model

The conduction band of a HEMT structure shown in figure 2.2 was computed with a self consistent Schrödinger-Poisson solver [33] for two gate voltages of $V_{GS} = 0\,\mathrm{V}$ and $V_{GS} = +0.6\,\mathrm{V}$. At zero gate bias, only one discrete electron state of the channel is below the Fermi level and occupied; the electrons are located at the front part of the quantum well, and the distance to the barrier can be roughly described by the barrier thickness. Increasing the gate voltage, more electron states are occupied broadening the 2DEG. For strong enhancement, electrons enter into the barrier forming a parasitic MESFET close to the delta doping profile. Here, the electron mobility is worse compared to the 2DEG in the quantum well related to strong interaction with activated Si-donators. However, the impact on device performance is minor since the parasitic MESFET is not relevant for low-noise biasing at low current level or shows similar saturation velocities compared to channel electrons when operated at high drain voltage for high output power.

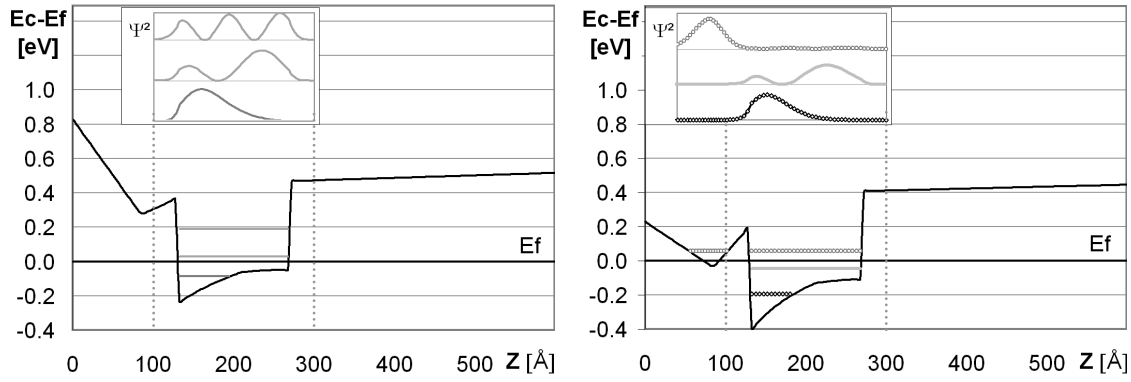


Figure 2.2: Simulation of a HEMTs conduction band and discrete channel states (c-band [33]) for zero gate voltage (l) and enhancement mode (r) with V_{GS} = +0.6 V. The inlay shows the probability function of electron location. While only one electron level is below E_f at zero gate bias, more occupied states are below the Fermi level for enhancement mode operation.

For a simple linearized charge control model, non-linear effects due to the parasitic MESFET and gradual pinch-off related to substrate doping are neglected. Bending of the conduction band can be described by the electrostatic potential $V(z)$. With the effective electron mass, the eigenenergies E_i and wave functions $\Psi_i(z)$ can be calculated from the Schrödinger equation. The electron concentration is given by the squared wave-function. The location of the charge centroid depends on the channel structure and the surface potential controlled by the gate voltage which becomes evident by the inset charts of the squared wave functions in figure 2.2. Since the electro static potential $V(z)$ is only linked to vertical z-direction, the wave-function $\Psi(x, y, z)$ can be described as follows

$$\Psi(x, y, z) = \zeta(z)\, exp(i\theta z)\, exp(ik_x x + ik_y y)\ , \tag{2.1}$$

with lateral components of the wave vector k_x and k_y, the wave vector θ and effective mass m_z in vertical z-direction and the solution $\zeta_i(z)$ of the one-dimensional Schrödinger equation given in equation 2.2.

$$\left[-\frac{\eta^2}{2m_z}\frac{d^2}{dz^2} - eV(z)\right] \cdot \zeta_i(z) = E_i \cdot \zeta_i(z) \quad \text{with} \quad \zeta_i(z) = 0 \text{ for } z \to \pm\infty \tag{2.2}$$

Two dimensional movement of the electrons along the quantum well channel can be described by the two-dimensional Schrödinger equation given in equation 2.3 with the effective mass m_x and m_y parallel to the interfaces.

$$\left[-\frac{\eta^2}{2m_x}\frac{d^2}{dx^2} - \frac{\eta^2}{2m_y}\frac{d^2}{dy^2}\right]\ exp(ik_x x + ik_y y) = E_{x,y}\, exp(ik_x x + ik_y y) \tag{2.3}$$

With the eigenvalues E_i from the one-dimensional Schrödinger equation representing discrete sub-bands within the quantum well and free two dimensional electron movement in lateral direction, the energy dispersion of the two dimensional electron gas is given by equation 2.4.

$$E_i(k) = E_i + \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y}, \qquad i = 0, 1, 2, ... \tag{2.4}$$

In order to calculate the electron concentration of the two dimensional electron gas in the quantum well, the product of density of states D_{2D} given in 2.5 [34] and the Fermi-distribution $f(E)$ has to be integrated over the energy by equation 2.6.

$$D_{2D}(E) = \frac{m^{\star}_{ll}}{\pi\hbar^2} \sum_i H(E - E_i), \qquad H(x) = \begin{cases} 0 & \text{for} \quad x < 0 \\ 1 & \text{for} \quad x \geq 0 \end{cases} \tag{2.5}$$

$$N_s = \int_{E_L}^{\infty} f(E)\, D_{2D}(E)\, dE \tag{2.6}$$

In first order, the electron concentration is given by the occupied states located below the Fermi level. This interpretation is valid for very low temperatures close to T = 0 K where the Fermi-distribution is described by a step function; at higher temperature, states above the Fermi energy may get occupied due to the thermal energy of the electrons. A simple capacitor model can be used to describe the charge density of the channel electrons as a function of gate voltage V_{GS}. In contrast to the MESFET, the distance d_b between the gate electrode and the channel electrons is constant for HEMT structures in first order and is given by the barrier thickness neglecting the wave function charge centroid. Equation 2.7 describes the linearized relation between charge density and gate voltage with the dielectric constant ε_b of the barrier material and the threshold voltage V_{th}.

$$N_s = \frac{\varepsilon_b}{e\, d_b}(V_{GS} - V_{th}) \tag{2.7}$$

The threshold voltage is defined by the barrier height of the Schottky contact Φ_b, the conduction band discontinuity ΔE_c between channel and barrier, the pinch-off voltage V_p required for complete depletion of the barrier, the distance between the gate electrode, the δ-doping plane $d^{\star}$ and the charge concentration of activated donors N_b within the barrier.

$$V_{th} = \Phi_b - \frac{(\Delta E_c - E_f)}{e} - V_p, \qquad \text{with} \qquad V_p = \frac{e\, d^{\star}}{\varepsilon_b} N_b \tag{2.8}$$

Deviations from the linear charge control approximation may occur due to the parasitic MESFET and a non-ideal gradual device pinch-off; the effective distance between the electron gas and the gate electrode is not constant due to the bias dependent location of the charge centroid. Moreover, influence from real device operation like drain biasing and charge transport in the channel are totally neglected. A more accurate hyperbolic tangent charge control model for the HEMT is discussed by Karmalkar [35]. The onset of the parasitic MESFET is shown in figure 2.3 where the charge density is calculated separately versus V_{GS} for the electrons in the channel and the barrier. A low-noise device has to be operated at low current levels to suppress effects related to the parasitic MESFET that are: Low RF-gain due to low electron mobilities in the barrier layer and Coulomb scattering with activated donators causing RF-noise.

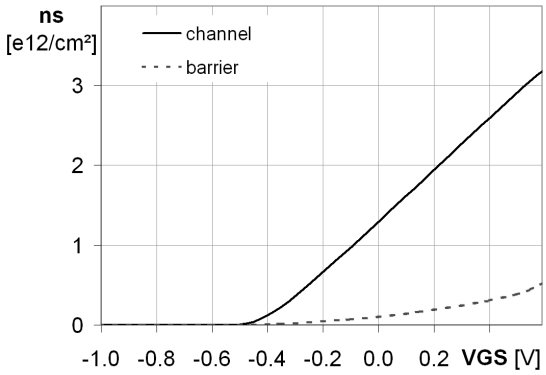


Figure 2.3: The charge-density is calculated over V_{GS} for electrons in the channel and the barrier forming a parasitic MESFET (c-band [33]).

To optimize for a large area of linear charge control, the depth of the quantum well has to be maximized linked to a optimization of the conduction band discontinuity ΔE_c at the heterostructures. The conduction band offset is mainly given by the different bandgap of the semiconductors used for the channel and the barrier layers. An overview of the bandgap E_g for several III-V compounds as a function of the lattice constant r_0 is shown in the left part of figure 2.4.

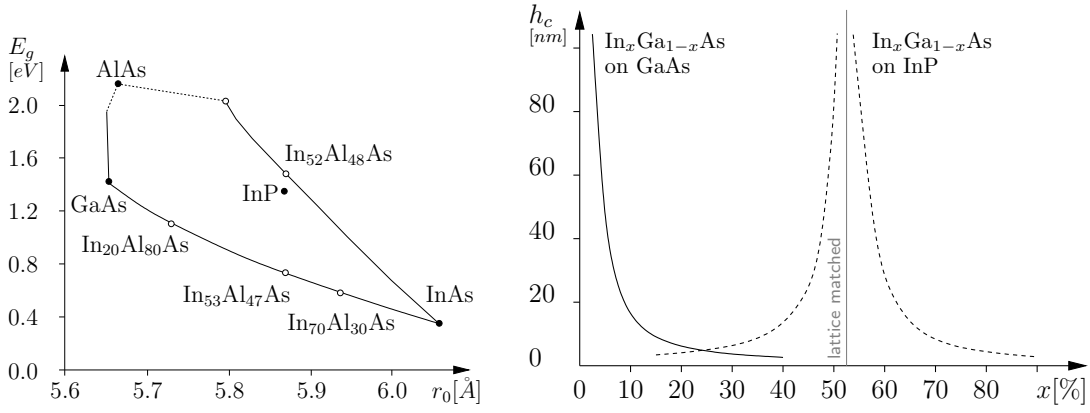


Figure 2.4: The lattice constant and bandgap of common III-V semiconductors (l) and the critical thickness h_c of $In_xGa_{1-x}As$ grown on GaAs- and InP substrates (r) as a function of the indium-content [36].

Due to mechanical constraints not any variation of the barrier and channel can be realized by epitaxy growth. On GaAs substrates, $Al_xGa_{1-x}As$ can be grown for any mole fraction x due to an almost similar lattice constant; therefore it is well suited to form the barrier layers. Since the barrier also includes the Si-based delta doping profile, the aluminium concentration is limited to 25 % to prevent deep DX-center states that reduce donor activation. To optimize for the conduction band discontinuity, $In_xGa_{1-x}As$ is used for the channel of the pseudomorphic HEMT having a lower band gap than GaAs. However, there is a tradeoff between the indium concentration, the layer thickness and defect density due to mechanical strain that can be realized by epitaxy growth. Using low temperature **M**olecular **B**eam **E**pitaxy, the indium content is limited to around 20 % for

a 12 nm thick $Al_{25}Ga_{75}As$ / $In_xGa_{1-x}As$ / $Al_{25}Ga_{0.75}As$ pseudomorphic channel structure grown on GaAs substrate; the conduction band discontinuity is limited to $\Delta E_c = 0.42\,eV$ (c-band simulations [33]). Based on the lattice constant for InP - either by using InP substrates or metamorphic buffer growth on GaAs - a higher conduction band discontinuity can be realized for the $In_xAl_{1-x}As$ / $In_xGa_{1-x}As$ / $In_xAl_{1-x}As$-system. With a channel indium concentration of 70 % and 47 % in the barrier, the conduction band discontinuity is $0.64\,eV$. The metamorphic structures offer better charge confinement of the 2DEG than the pseudomorphic HEMT structure based on GaAs. However, the one dimensional view of the linear charge control model neglects all lateral impact coming from drain biasing for real device operation.

2.1.2 Channel electron transport

The electron movement in the channel from source to drain is driven by electric fields linked to the drain voltage V_{DS}. The drain current can be calculated from the charge density $n_s(x)$ at the position x of the channel, the electron velocity $v(x)$ and the gate width of the device W.

$$I_D = e\,W\,n_s(x)\,v(x) \tag{2.9}$$

The electron velocity $v(x)$ itself can be described by the product of the low electric field electron mobility μ_n and the electrical field $E_x(x)$ along the channel. The field dependence of the electron velocity over the electrical field is shown in the left part of figure 2.5 for several semiconductor materials. For the III-V-compound semiconductors there is velocity overshoot. While $In_{53}Ga_{47}As$ shows a more pronounced velocity overshoot compared to GaAs the saturated drift velocity at high fields is almost equal. Velocity overshoot is linked to the retarded transfer of central valley electrons to the higher mass satellite valleys of the conduction band; electrons of the central valley are accelerated by electrical fields exceeding the saturated velocity until they have enough energy to scatter into the satellite valley of significantly higher mass and therefore lower velocity. The analytical approximation for the drift diffusion model (DD) of the carrier mobility in equation 2.10, does not consider velocity overshoot since carrier temperatures are assumed to be constant.

$$\mu_n(E) = \frac{\mu_n}{\sqrt{1 + \left(\frac{\mu_n E}{v_{sat_n}}\right)^2}}\,; \qquad \text{with the low field mobility } \mu_n. \tag{2.10}$$

A hydrodynamic (HD) model has been developed by Hänsch [37] given in equation 2.11with the fitting factor β depending on the semiconductor material. T_n and T_L denote for the electron and lattice temperature with the carrier energy relaxation time τ_{wn}.

$$\mu_n(T_n) = \frac{\mu_n}{\left(1 + \alpha_n (T_n - T_L)^{\frac{1}{\beta}}\right)^{\beta}} \quad \text{with} \quad \alpha_n = \left(\frac{3k_B\,\mu_n}{2e\tau_{wn}\,v_{sat_n}^2}\right)^{\frac{1}{\beta}} \tag{2.11}$$

In this approach an additional parameter β was introduced based on HEMT simulations [38] to match with static overshoot obtained by Monte Carlo simulations in the channel. The field dependent electron mobility reads as:

$$\mu_n(|E|) = \frac{2^\beta \mu_n}{\left(1 + \sqrt{1 + \left(\frac{2\mu_n|E|}{v_{sat_n}}\right)^{\frac{2}{\beta}}}\right)^\beta} \tag{2.12}$$

To illustrate the electron transport for a real HEMT a cross sectional schematic diagram of the device is shown in the right part of figure 2.5. Below the gate, electrical fields are low at the source-side (area 1), and electron velocity is below the saturation level. From $x = L_s$ towards the drain (area 2), velocity saturation is reached. However, there is velocity overshoot, and the mean electron velocity exceeds the saturation velocity. The expansion of the drift zone $x = L_d$ between the gate and the drain side of the recessed cap at $x = L_{gs}$ (area 3) strongly depends on the applied drain voltage and the influence of surface states; electrons move with saturated velocity. Outside the drift region towards the drain (area 4) the electron velocity is again below saturation due to low electrical fields.

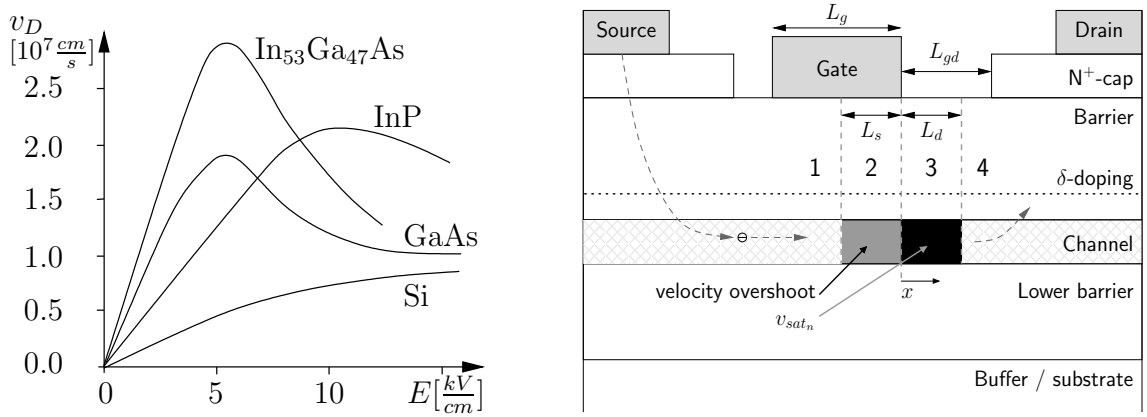


Figure 2.5: Drift velocities of electrons (l) depending on the electrical field E for several semiconductor materials. Cross sectional schematic diagram of the HEMT (r) showing the areas of different electron velocity. At the source side of the gate (1) and the end of the drift zone (4) electrical fields are low linked to a slow electron velocity. In the high electric field drift zone, velocity overshoot may occur in area (2) described by the hydrodynamic transport model, while velocity saturation is found in area (3). Velocity overshoot is important for low-noise operation; a high saturation velocity is required for power devices.

An iterative solution for the drain current I_D as a function of biasing at V_{GS} and V_{DS} is given in [39] based on the drift diffusion model by the calculation of the saturation zone L_s underneath the gate and the drift zone L_d. However, the basic dependencies between the electron transport in the channel and device RF-properties can be discussed in a simple way. To improve the RF-gain of the device, one has to optimize for a short electron transfer time τ from source to drain. The electron transfer time of the intrinsic device can be summarized from the transfer time of regions 1 to 3 with the mean velocities V_i and saturation drift velocity v_{sat_n}.

$$\tau = \frac{L_g - L_s}{v_1} + \frac{L_s}{v_2} + \frac{L_d}{v_{sat_n}} \tag{2.13}$$

To optimize the transfer time, the gate length L_g can be reduced also supporting the impact of velocity overshoot in region 2 [40]. Furthermore, the expansion of the drift zone can be minimized by low drain voltage operation. However, this is only an option for low-noise devices that do not have to provide much output power.
To assess the different transport properties for metamorphic and pseudomorphic HEMT structures, simulations of generic device structures have been performed with the commercial tool ATLAS (Silvaco) 2.6. For the device model, the structure of the HEMT is split into segments of different material and physical parameters. For each semiconductor segment Poisson's equation and the continuity equation have to be solved numerically for each carrier type to calculate the electric field and charge density; thermionic-field emission and tunneling has to be taken into account at heterojunction interfaces while surface states, especially at the gate recess, form a built-in electrical field perpendicular to the semiconductor surface. Models and most materials parameters are provided by the simulators library. Detailed investigations on numerical device simulations of HEMT structures have been performed by Brech [38].

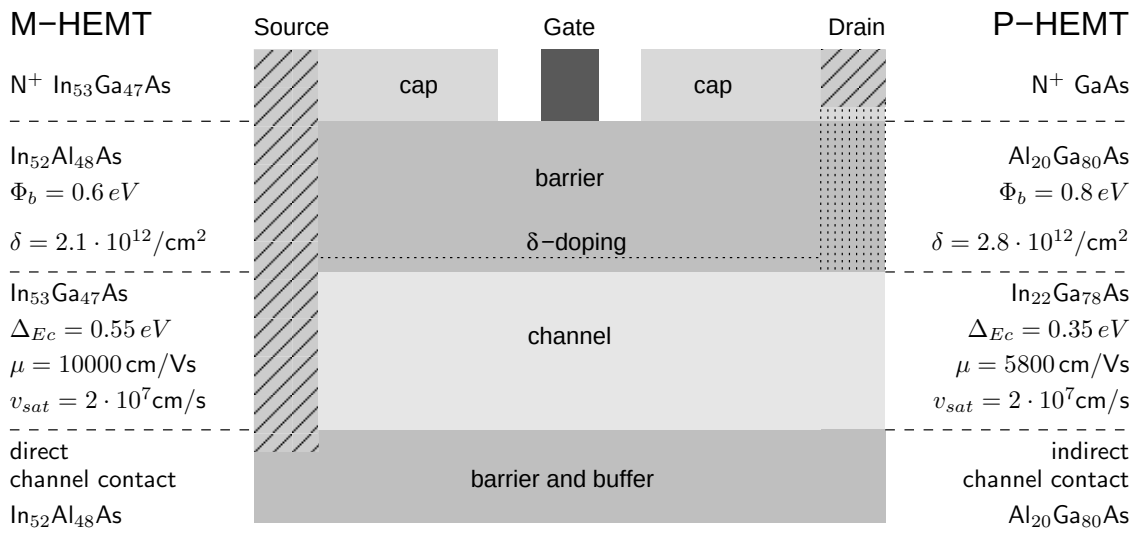


Figure 2.6: Generic metamorphic and pseudomorphic HEMT structure including physical parameters required for device simulation. Geometry aspects like the gate length, gate recess and barrier thickness are similar for both structures; merely the ohmic contact is realized differently with direct contacting of the metamorphic channel.

The generic device structure used for simulation is shown in figure 2.6; the left part of the picture represents the metamorphic, the right part the pseudomorphic structure. For comparison, similar geometry parameters like the barrier thickness (18 nm), recess size (270 nm) and gate length (70 nm) have been chosen for both technologies. Unstrained $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ layers are used for the channel of the metamorphic structure

showing a higher conduction band discontinuity Δ_{Ec} and low field electron mobility μ compared to the pseudomorphic device structure. Referring to figure 2.5, the saturation velocity v_{sat} at high electrical field as found in the drift zone of the device is almost equal for both channel materials. However, there is velocity overshoot in the channel area underneath the gate foot before electrons are retarded to their high field saturation velocity. Velocity overshoot described by the hydrodynamic transport model is more pronounced for higher indium concentration and electrons of the metamorphic device can achieve a higher overshoot velocity and therefore a higher mean velocity for charge transfer. Physical parameters of the materials have been taken from the library of the simulation tool without modification. Merely the doping levels and the height of the Schottky barrier have been adjusted to reach typical values for device pinch-off obtained in previous work [15, 41].
Device simulations shall only provide a qualitative view on the DC-transport properties of the metamorphic and pseudomorphic HEMT structures and will deviate from results obtained by experiment. The transfer characteristics have been simulated for a constant drain voltage of V_{DS} = 1.5 V for both HEMT structures as shown in figure 2.7. Due to the higher conduction band discontinuity for the metamorphic device, more carriers are confined in the channel and a higher current density combined with a more negative pinch-off are observed. Since surface states located near the gate recess have been neglected in the simulation, the maximum saturation currents exceed typical measured results presented later by around 20 % on both structures. The peak transconductance G_{max} of more than 1000 mS/mm is significantly higher for the metamorphic structure compared to 740 mS/mm for the pseudomorphic structure.

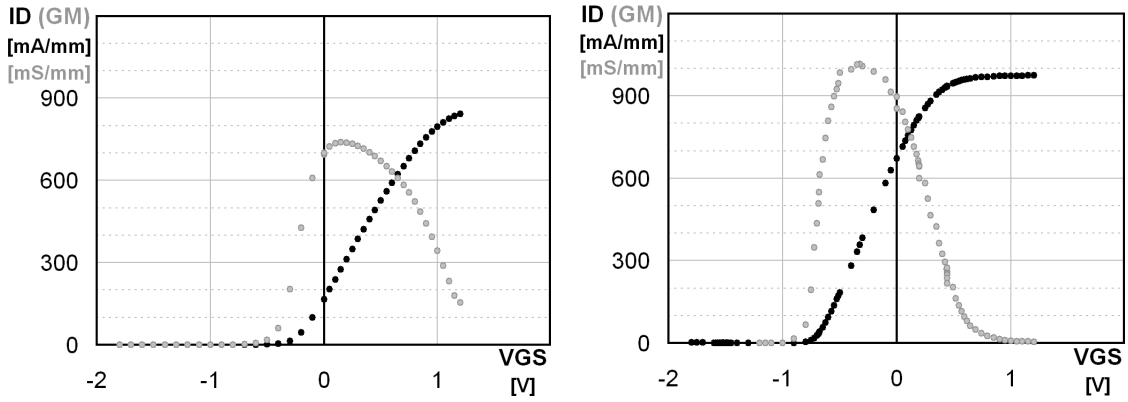


Figure 2.7: Simulated transfer characteristic of the pseudomorphic (l) and metamorphic (r) HEMT structure at V_{DS} = 1.5 V.

Besides the calculation of the IV-characteristics, the distribution of the electrical field been simulated for open channel operation at V_{GS} = 0.4 V and V_{DS} = 1.5 V and device pinch-off at V_{GS} = -1.2 V and V_{DS} = 2.5 V. Results are presented in figure 2.8 for the metamorphic structure. The pinched off device shows a maximum electric field of around 600 kV/cm at the drain-side of the gate foot. For the open channel operation condition at V_{GS} = 0.4 V, the maximum electric field is still observed at the drain-side of the gate foot but lowered to around 100 kV/cm. This is due to the reduced drain to gate voltage V_{GD} and the appearance of a second high field domain at the drain-end of the gate recess but also real space transfer of hot electrons into the barrier and buffer layers [42]. Simulations of the pHEMT

structure showed no remarkable qualitative difference for the electric field distribution.

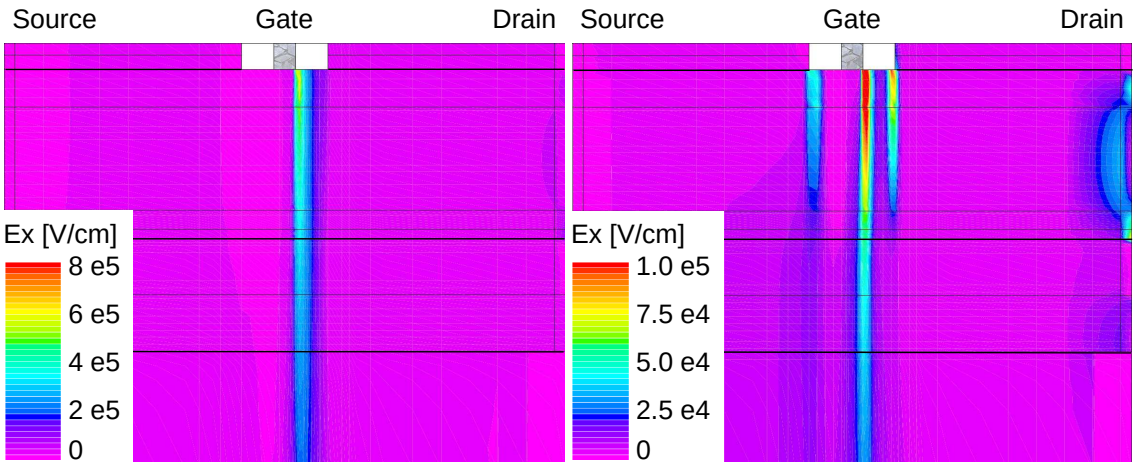


Figure 2.8: Simulated electrical field distribution of the metamorphic HEMT structure for pinch-off (l) and open channel condition (r) at $V_{DS} = 2.5$ V and 1.5 V, respectively.

Due to the assumption of ideal boundary conditions in this model there are too large errors for a quantitative evaluation of the HEMT structures. For a more accurate model, the surface states in the gate recess area which affect the electric field distribution have to be considered carefully, and several simulation iterations are required to obtain good agreement with experimental data. Usually, the model parameters have to be adjusted by fitting factors to find a compromise for the DC- and RF-behavior. Fitting of material parameters has to agree with literature data that frequently show large variations.

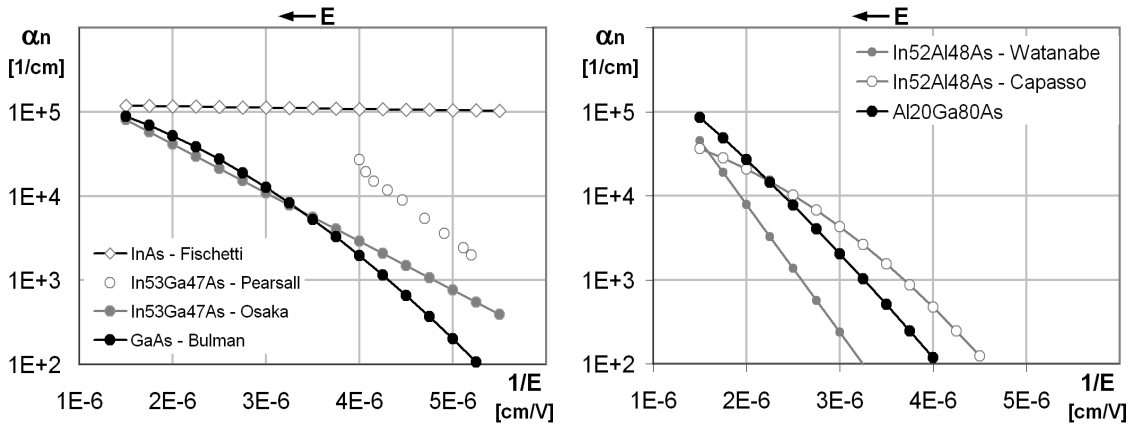


Figure 2.9: Impact ionization coefficient α_n for electrons in typical channel (l) [43, 44, 45, 46] and barrier (r) material [47, 48, 49, 50].

For instance in figure 2.9, there is a is a big difference for the ionization coefficient α_n for the metamorphic channel material $In_{53}Ga_{47}As$ depending on the literature source [43, 44]. Compared to GaAs, Osaka observed slightly higher impact ionization rates for $In_{53}Ga_{47}As$ only at low electrical fields. Much more pronounced impact ionization between that of GaAs and InAs has been reported by Pearsall [44]. However, the lower α-values given by Osaka are considered as the correct ones due to good agreement to

noise simulations [43] and are implemented in the library of ATLAS. Similar uncertainties are found for the $In_{52}Al_{48}As$ barrier material. Therefore, it is difficult to simulate the device breakdown precisely as desired to optimize the channel of the device regarding impact ionization. In sub-channel architectures for instance [51], hot-electrons may transfer from the low band gap high mobility channel into the sub-channel of higher band gap before impact ionization is observed.

2.2 DC-characteristics and parameters

The output characteristics shown in figure 2.10 can be separated into three areas. In the access region (I) at low V_{DS}, the electron velocity is below saturation and the device works as an voltage controlled resistor; this area is of less interest for a transistor working as an amplifier but becomes more important if the device is used as a mixer. In the second area (II), the device represents a voltage controlled current source with the saturation current $I_D(V_{GS})$; the expansion of the drift zone at the drain side of the gate strongly depends on the drain voltage V_{DS}. Device breakdown occurs in the third area (III) due to several mechanisms discussed later.

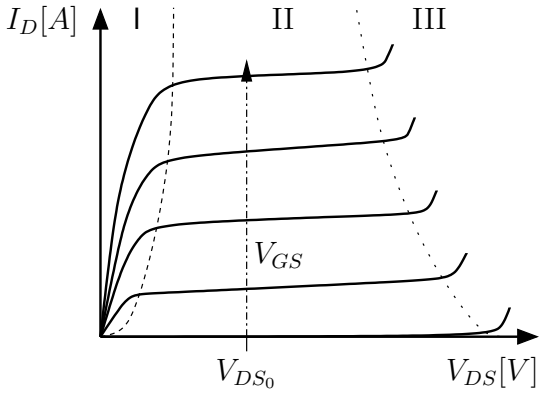


Figure 2.10: Schematic output characteristics of a HEMT with the access (I), saturation (II) and breakdown area (III).

There are several key DC-parameters to describe the properties of the device as shown in figure 2.11. For a constant drain voltage V_{DS}, a gate voltage sweep is performed from deep pinch-off to open channel to obtain the transfer characteristic of the device. The maximum saturation current I_{DS^+} is determined at a gate voltage adequate to the Schottky barrier height which is 0.7 V for the pseudomorphic and 0.5 V for the metamorphic HEMT. The definition of the saturation current I_{DSS} at $V_{GS} = 0$ V originates from JFET technologies and represents the drain current at the transition from depletion to enhancement mode device operation; I_{DSS} is close to zero for enhancement mode devices. For depletion mode devices considered in this work, the device pinch-off voltage V_{G100} is defined at a drain current of 1 % of I_{DSS}. The transconductance G_m is derived from the transfer characteristic with the peak transconductance G_{max}. Diode breakdown voltages V_{GD} and V_{GS} are obtained from two port measurements for a reverse current of 1 mA/mm. The device breakdown voltage V_{bDS} is extracted from a gate voltage sweep for a constant drain current of 1 % of I_{DSS} as shown in the right part of figure 2.11. The off-state breakdown V_{bDS} does not have to be related to avalanche breakdown in the channel but might be linked to thermionic field emission or tunneling.

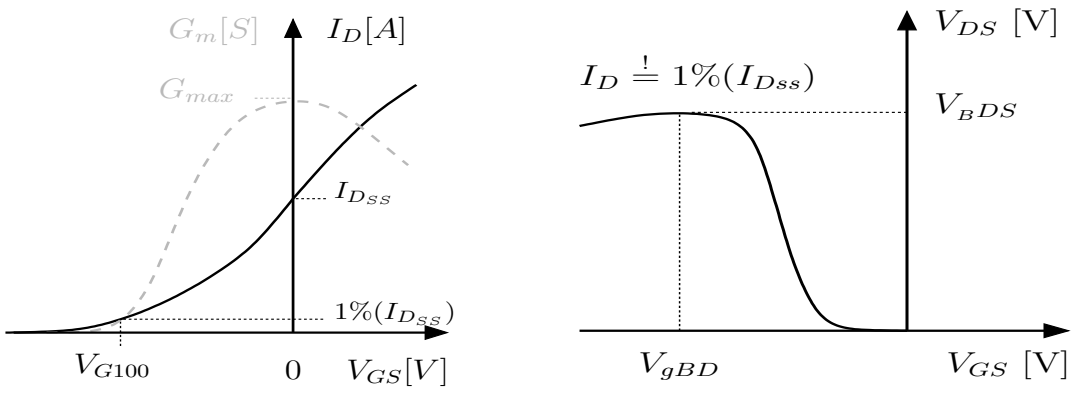


Figure 2.11: Transfer characteristic (l) from a V_{GS} sweep at constant drain voltage V_{DS} including key DC-parameters. The three terminal device breakdown (l) V_{bDS} is obtained from a V_{GS}-sweep for a leakage current of 1 % of the saturation current I_{DSS}.

In contrast to the off-state breakdown V_{bDS}, the evaluation of the on-state breakdown behavior at open channel is more difficult because the open channel represents the counter electrode including lateral current flow. Device operation in this area is very sensitive to oscillations - there is no on-state breakdown parameter that can be systematically assessed by automatic measurement tools. Device breakdown may occur due to:

- Gate breakdown: there are leakage currents over the gate barrier due to thermionic field emission and tunneling mechanisms [52]. The device may work properly, however, these currents can degrade the gate metal by electro migration forming local interruptions of the Schottky contact. Due to locally increased current densities, hot spots are formed that may locally destroy the device by thermal run away. Furthermore, gate breakdown can be linked to avalanche breakdown due to high electric fields in the barrier layer.

- Avalanche breakdown: critical electrical fields can be reached in the active layers causing impact ionization and avalanche current multiplication. The device fails by instantaneous burn-out.

- Substrate breakdown & leakage: Critical electrical fields may occur in the substrate between source and drain but also between the drain areas and the grounded backside metalization of the device. Furthermore, there are leakage pathes supported by impact ionization in the channel; holes injected and accumulated in the buffer lower the energy level of the conduction band and work against device pinch-off.

The breakdown mechanisms of the HEMT are sketched in figure 2.12. In contrast to an ideal Schottky diode, the depletion zone of the gate diode is also expanded laterally causing two barriers in series with a poor ideality factor around 1.4. At high drain voltage or electric field, the conduction band is strongly bent between the Schottky contact and the end of the drift zone at the drain side of the channel. Electrons may overcome the barrier I) by thermionic field emission and tunneling [52] and may contribute to impact ionization due to the high electric field in x-direction. The gate breakdown voltage is usually determined by two-terminal measurements for a fixed reverse leakage current (typically 1 mA/mm).

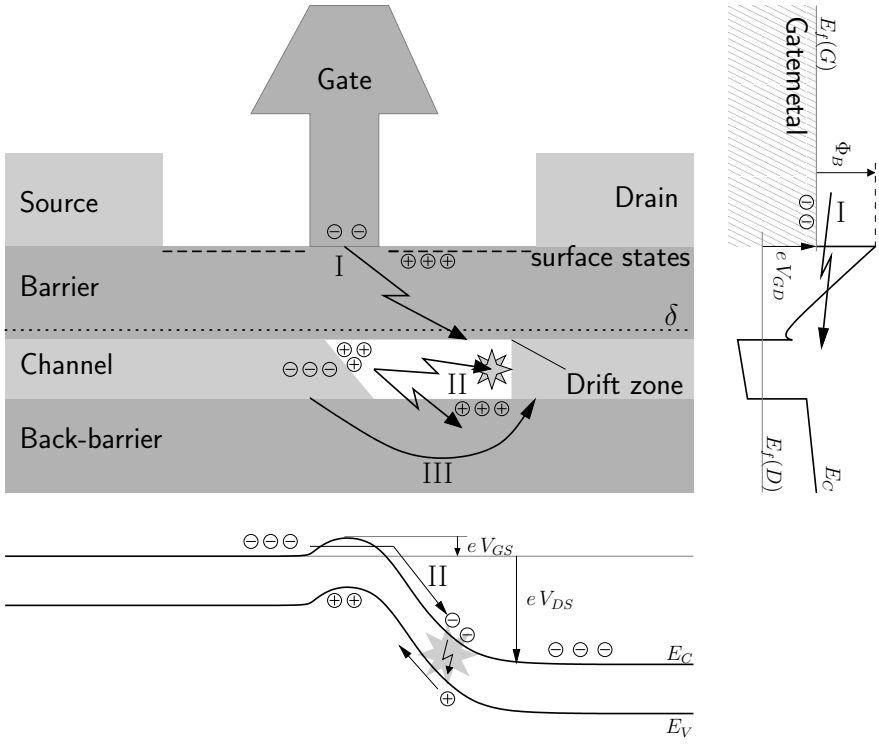


Figure 2.12: Breakdown mechanisms in a HEMT: I) gate breakdown, II) channel breakdown and hot-electron transfer into the buffer and III) substrate leakage. Holes from impact ionization are accumulated at the recess surface and the valence band maximum below the gate. Band diagrams for electron injection across the Schottky barrier and along the channel are sketched right and below the cross section of the device.

The off-state breakdown V_{bDS} is determined from three-terminal measurements where the channel is pinched off down to a fixed drain leakage current. Gate breakdown but also channel breakdown contribute to drain leakage, where source-side electrons are injected into the high field drift zone by overcoming the channel barrier II) towards the drain; this hot electron effect is more pronounced for a short gate length. Holes created by impact ionization accumulate in the valence band maximum [53, 54] right below the gate and may recombine radiative by electroluminescence [55, 56]. However, holes get also injected into layers outside the channel and act as a fixed positive charge, lowering the energy barrier at the source/channel junction and enhancing the electron injection into the high field area of the channel - in the substrate, this phenomenon is often referred as the parasitic bipolar effect [57, 58, 59] (PBE). The parasitic bipolar effect can be successfully suppressed by a p-type doped substrate body contact placed below the back barrier [60]. Depending on the value for the leakage currents, different temperature dependencies might be observed for the off-state breakdown [61] allowing a rough identification of the dominating breakdown mechanism. Compared to MESFETs, HEMTs can achieve a higher off-state breakdown voltage for similar maximum drain current density; this is related to the lateral extension of the drift zone and surface states located at the gate recess which cause surface depletion discussed later in the recess section. At open channel, the on-state breakdown is dominated by hot channel electrons and impact ionization.

2.3 RF-characteristics and parameters

RF-properties of the devices are usually characterized by small signal, RF-noise and power measurements. Based on data from several bias conditions and device geometries, lumped element models are extracted to describe the transistors characteristics and are used for circuit design and simulation. Depending on the application, these models may differ from each other; e.g. the noise elements are neglected for the non-linear model of a power device, while power considerations are not required, if the focus is set on low-noise.

2.3.1 Small signal model and equivalent circuit

In the range of high radio frequencies, voltages and currents cannot be measured directly anymore. Scattering matrices are used to describe the small signal properties based on normalized waves at the device ports i and j. The complex elements s_{ij} of the scattering matrix $\overleftrightarrow{S}$ reflect the linear connection between the entering a_i and emitted b_i waves as given in equation 2.14 for a two port device like the HEMT.

$$\begin{aligned} b_1 &= s_{11}\,a_1 + s_{12}\,a_2 \\ b_2 &= s_{21}\,a_1 + s_{22}\,a_2 \end{aligned} \tag{2.14}$$

During small signal characterizations, the device under test (DUT) is placed between a linear RF-source and a passive load as shown in figure 2.13. At the connections of the building blocks, reference planes are defined where e.g. the emitted wave b_1 of the source is equal to the entering wave a_i at the input of the device. The ratio of the returning b_i and entering wave a_i defines the complex reflection coefficient $\Gamma_k^{(j)}$ indexed with the view-point k with G from the generator and L from the load. The upper index indicates for combinations of building blocks; e.g. Γ_G^1 is the reflection coefficient of the combined source consisting of the source and the device under test. Matching is realized at the reference planes, for a conjugate complex relation between the both reflection coefficients. In the case of input matching $\Gamma_L^{(1)} = \Gamma_G^{(0)\star}$ the total available power of the emitted wave b_1 enters into the test device without any returning power ($b_2 = 0$).

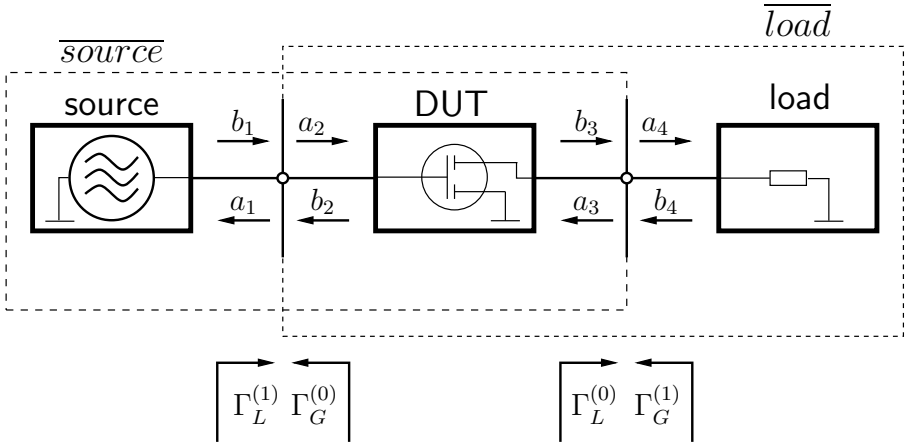


Figure 2.13: Small signal scattering parameter characterization.

A descriptive interpretation of the scattering matrix elements in the case of a two-port device like the HEMT is given as follows:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad \text{Input reflection coefficient for matched output} \tag{2.15}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad \text{Output reflection coefficient for matched input} \tag{2.16}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad \text{Transmission coefficient for matched output} \tag{2.17}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad \text{Transmission coefficient for matched input} \tag{2.18}$$

Comparing the output power of the combined source including the test device with the power of the wave generator alone is the definition of the available power gain G_A with the output conjugately matched in equation 2.19.

$$G_A = \frac{|s_{21}|^2 \left(1 - |\Gamma_G|^2\right)}{|1 - s_{11}\Gamma_G|^2 - |s_{22}\left(1 - s_{11}\Gamma_G\right)|^2} \tag{2.19}$$

Internal feedback may cause device oscillation that generates RF-output power from the DC-supply without external stimulation; the denominator in equation 2.19 is zero leading to infinity gain. Thus, for device stability following conditions have to be fulfilled:

$$|s_{22}| < 1 \tag{2.20}$$

$$|s_{12}|\,|s_{21}| < 1 - |s_{22}|^2 \tag{2.21}$$

$$|s_{11}| < 1 \tag{2.22}$$

$$|s_{21}|\,|s_{12}| < 1 - |s_{11}|^2 \tag{2.23}$$

$$k > 1 \tag{2.24}$$

For normal active two-ports based on transistor devices, most stability conditions are fulfilled automatically and can be reduced to the stability factor k defined by Rollet [62] in equation 2.25.

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |det(\overleftrightarrow{S})|^2}{2|s_{12}|\,|s_{21}|} \tag{2.25}$$

With the stability factor k, the maximum available gain (MAG) can be expressed as follows.

$$MAG = \frac{|s_{21}|}{|s_{12}|}\left(k - \sqrt{k^2 - 1}\right). \tag{2.26}$$

The maximum stable gain (MSG) represents the maximum gain that can be obtained from the originally instable device using external stabilization circuits.

$$MSG = \frac{|s_{21}|}{|s_{12}|} < MAG \tag{2.27}$$

From small signal measurements, important key parameters like the maximum oscillation frequency f_{max} and the transit frequency f_T can be extracted from the frequency dependence of the unilateral power gain MUG and current gain $|h_{21}|^2$ given in equations 2.28 and 2.29.

$$MUG = \frac{|s_{21}/s_{12} - 1|^2}{2k\,|s_{21}/s_{12}| - \Re(s_{21}/s_{12})}\,, \qquad MUG(f_{max}) = 1 \tag{2.28}$$

$$h_{21} = \frac{-2s_{21}}{1 - s_{11} + s_{22} - s_{11}s_{22} + s_{12}s_{21}}\,, \qquad |h_{21}|^2(f_T) = 1 \tag{2.29}$$

At the maximum oscillation frequency f_{max} the unilateral power gain is 1 or 0 dB. Similar for the current gain $|h_{21}|^2$ for the transit frequency f_T representing the electron transition below the gate of the device. The frequency dependencies of the different gain types are shown in figure 2.14 for an exemplary transistor.

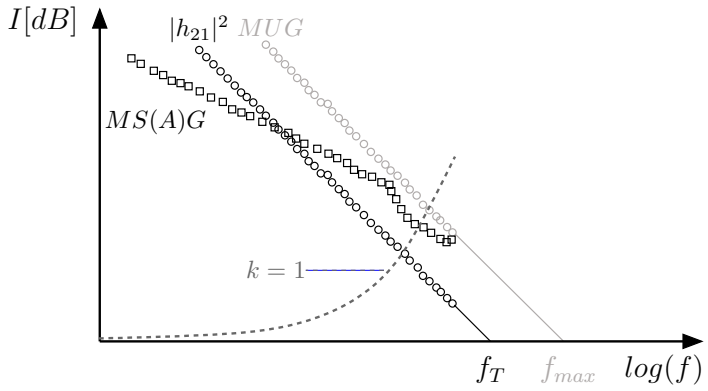


Figure 2.14: Extrapolation of the transit f_T and maximum oscillation frequency f_{max}.

For very high frequencies the maximum oscillation frequency and transit frequency cannot be determined from the measurement directly due to frequency limitations of the vector analyzer setup; values are extrapolated assuming a first order low pass behavior with a slope of 20 dB/decade. For a stability factor k below 1 the slope of the maximum stable gain MSG is 10 dB/decade. The maximum available gain ($k > 1$) shows a significantly larger drop over the frequency approaching the unilateral power gain.

The radio frequency behavior of the HEMT can be described by a lumped element model as depicted in figure 2.15. There is a distinction between intrinsic parts representing the active device and extrinsic elements linked to metallic pads as part of the input lines required to connect the device to the outer world.

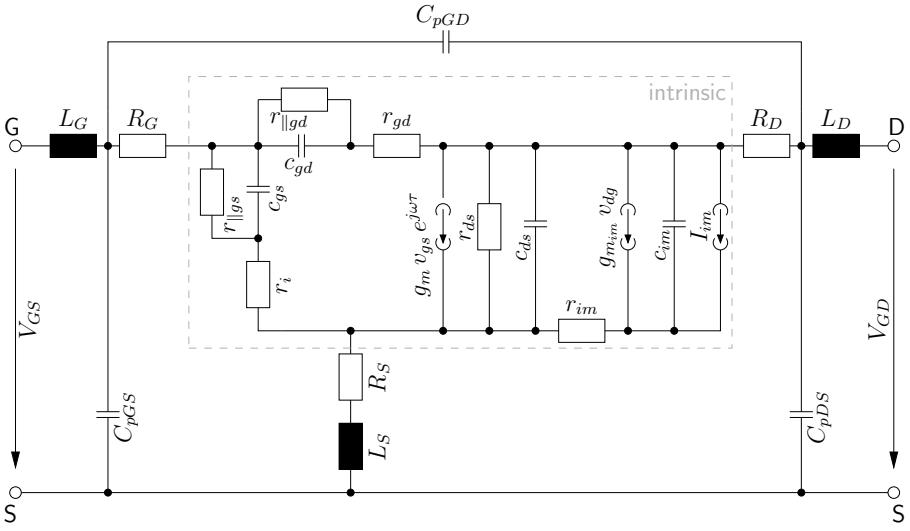


Figure 2.15: Small signal equivalent circuit of a HEMT.

A physical interpretation of the lumped elements for the HEMT is sketched in figure 2.16.

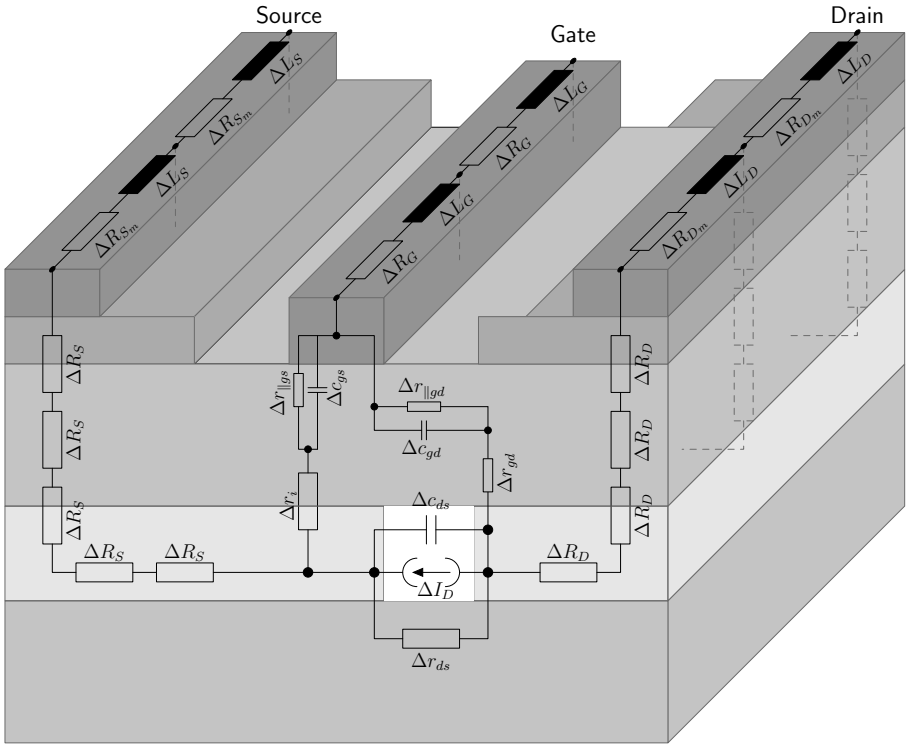


Figure 2.16: Physical interpretation of the intrinsic lumped elements model neglecting impact ionization (r_{im}, $g_{m_{im}}$, c_{im} and I_{im}) found in the small signal equivalent circuit in figure 2.15 .

Elements are distributed along the device periphery. In this parallel plate capacitor model, the input capacitance Δc_{gs} is formed between the gate and the source-side charges. The effective distance between the gate and source-side charges depends on biasing conditions and is in the order of the barrier thickness. Similar for the feedback capacitance Δc_{gd} and output capacitance Δc_{ds} where effective distances strongly depend on the expansion of

the channel drift zone. Parallel resistors $\Delta r_{\parallel gs}$ and $\Delta r_{\parallel gd}$ describe vertical leakage across the Schottky barrier. The access resistance of the device is formed as a series of drain and source resistors ΔR_D and ΔR_D that itself consist in parts to the channel, barrier and the ohmic contact. Neglecting impact ionization, the output conductance is given by Δr_{ds} representing short channel effects linked to the gate length and leakage through the substrate. For increasing drain voltage, impact ionization lowers the output conductance as considered by additional current sources in the small signal equivalent circuit in figure 2.15.
Elements of the small signal equivalent circuit can be approximately extracted from frequency dependent scattering parameter measurements described in [63] and [64]. Parasitic capacitances of the extrinsic device might be gained from "dead" devices having no channel or from active devices under "cold", deep pinch-off conditions. For the resistive and inductive parts, extractions can be carried out from shortened devices (drain-source) or from active devices under "hot", strong forward bias conditions. "Dead" structures offer only the pure metallic part of the parasitic elements. The "hot-cold" method includes depletion effects coming from the semiconductor. Yet, the "hot" measurement may damage sensitive devices due to strong forward gate currents. While extrinsic elements strongly depend on the geometric aspects of the device like pad arrangement and number of gate fingers, the intrinsic parameters linearly scale with the gate width. In order to describe the active devices within a scalable small signal model, devices of different gate width but similar gate configuration have to be characterized and fitted to the geometrical variations.
The small signal model may be extended for some large signal modulation, by fitting lumped elements along the load line. However, this approach is quite inaccurate due to non-linear effects such as current dispersion related to traps or impact ionization [65, 66]. RF-key parameters like the transit f_T and maximum oscillation frequency f_{max} can be brought into relation with small signal equivalent circuit elements. Two definitions are found for the transit frequency as given in equation 2.30 including or neglecting the feedback capacitance c_{gd}. For a high transit frequency, a high transconductance and small capacitances are required.

$$f_{T_i,c} = \frac{g_m}{2\pi(c_{gs} + c_{gd})} \qquad \text{and} \qquad f_{T_i} = \frac{g_m}{2\pi c_{gs}} \tag{2.30}$$

F_{max} can be approximated by equation 2.31 [67]. To optimize f_{max}, a high transit frequency is needed on the one hand but also a low source and gate resistance as well as a low feedback capacitance c_{gd}.

$$f_{max} = \frac{f_{T_i}}{\sqrt{4g_{ds}(r_i + R_G + R_S) + 2\frac{c_{gd}}{c_{gs}}\left(\frac{c_{gd}}{c_{gs}} + g_m(r_i + R_G + R_s)\right)}} \tag{2.31}$$

2.3.2 Noise considerations

All electronic devices show small deterministic fluctuations in measured parameters called noise. Four types of noise are of importance in semiconductors.

- **Thermal noise:** Any resistance R shows spontaneous current or voltage fluctuations according to $S_V = 4k_BT\,R$ or $S_I = 4k_BT/R$. The spectrum thermal noise is white whatever the nature of the conduction process or the mobile charge carriers.

- **Shot noise:** The current carried by electrons that cross a potential barrier in a semiconductor a randomly generated and lead to fluctuations around the current I with the white spectrum $S_I = 2qI$.

- **Generation-recombination noise:** The number of free electrons N in the conduction band may fluctuate because of generation and recombination processes. $S_N = \overline{\Delta N^2}/\,N^2 \cdot 4\tau/\,(1+\omega^2\tau^2)$ where τ is the characteristic trap relaxation time usually in the range of $10^{-6}...10^{-3}$ s.

- $1/f$**-noise or flicker noise:** This is a fluctuation in the conductance with a power spectral density proportional to $f^{-\gamma}$ and $\gamma = 1.0 \pm 0.1$ in a wide frequency range [68]. Unlike the first three well understood noise sources above, the origin of the $1/f$ noise is still open.

Typical noise spectra of above mentioned noise sources are sketched in figure 2.17. Thermal and shot noise contribute to a constant noise level over frequency and dominate the noise performance of the device at high frequencies. At lower frequency, recombination-generation or GR-noise with Lorentzian characteristics may be observed on top of the $1/f$ flicker-noise spectrum. The origin of flicker noise is still open. For finite values for the integral of the power density and the Fourier transform, the slope of the spectrum has to be steeper than -1 below and above a lower and upper cut off frequency. While the upper cut off frequency is hidden by RF-noise in the MHz-regime, the lower cut off frequency could not be experimentally determined by measurements down to 10^{-6} Hz [69].

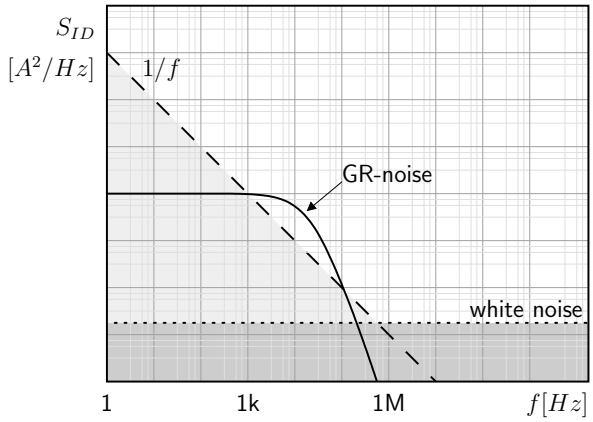


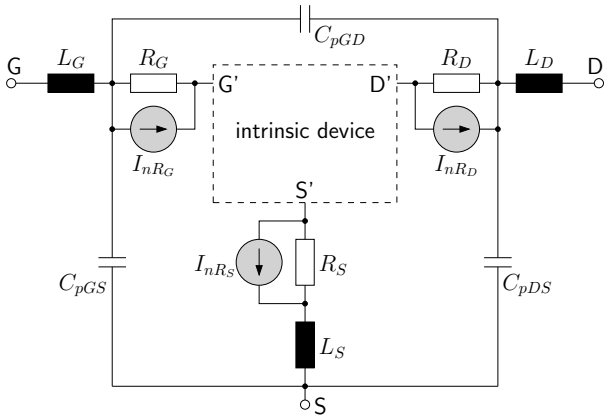
Figure 2.17: Frequency behavior of different noise sources.

Flicker noise has been considered by McWhorter as a surface effect [70], where the $1/f$-spectrum is explained by the superposition of several GR-centers of different recombination constants. With respect to the large bandwidth of flicker noise, relaxation times of a material have to cover a very wide range from 10^6 to 10^{-6} s. In GaAs and InP, $1/f$-noise has been described by charge mobility fluctuations linked to lattice scattering in the semiconductor material [71].

Flicker noise plays an important role in non-linear oscillator or mixer applications showing up-conversion of the $1/f$-noise spectra. Low frequency noise is of minor importance for the W-band low noise amplifiers in this work and was not regarded in the RF-noise model.

2.3.3 Noise model

Resistors of the extrinsic device model shown in figure 2.18 contribute to white RF-noise which is constant over frequency with noise currents I_{nRx} described by pure thermal noise. It is related to charge velocity fluctuations within the resistors caused by the thermal energy of the carriers. The temperature T_0 of the resistors normally is close to the ambient temperature with a slight increase due to device operation and self heating.



$$I_{nRx} = \sqrt{\frac{4k_bT_0}{R_x}\,\Delta f}$$

Figure 2.18: Extrinsic noise elements (grey) of the HEMT creating thermal or Johnson noise.

For the intrinsic device, the contribution to RF-noise may be described by two noise sources - the channel noise source I_{nd} and the correlated gate noise source I_{ng} [72]. Noise currents and the correlation coefficient C are given in equation 2.34 with the dimensionless constants P and R.

$$\overline{|I_{nd}|^2} = 4k_bT_0\Delta f\, g_m\, P \tag{2.32}$$

$$\overline{|I_{ng}|^2} = 4k_bT_0\Delta f\, \frac{\omega^2 C_{gs}^2}{g_m}\, R \tag{2.33}$$

$$jC = \frac{\overline{I_{ng}^{\star}\, I_{nd}}}{\sqrt{\overline{|I_{ng}|^2}\,\overline{|I_{nd}|^2}}}\,. \tag{2.34}$$

A more detailed view on intrinsic noise sources is given in figure 2.19. There is shot noise I_{nL_S} and I_{nL_D} linked to leakage currents I_{Lx} across the non-ideal Schottky barrier. The noise currents are given by $I_{nL_x} = \sqrt{2q\, I_{Lx}\Delta f}$. Since shot noise is also white or constant over frequency, usually, its contribution is modeled by an equivalent thermal noise source [73] with an equivalent noise resistance R_{gs} and noise temperature T_{GS}.

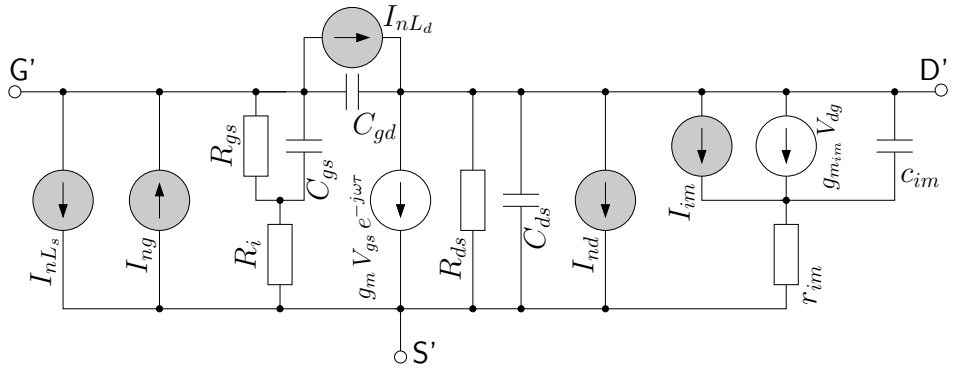


Figure 2.19: Intrinsic noise elements (grey) of the HEMT.

Generation-recombination noise linked to impact ionization is taken into account by the current source I_{im}; the frequency dependence is modeled by the noiseless resistor r_{im} and capacitor c_{im}. The channel noise sources are linked to velocity fluctuations of electrons due to phonon and Coulomb scattering. In a HEMT structure, the part related to Coulomb-scattering is lower compared to the MESFET due to the spacial separation of the channel electrons from the positively charged activated donor-states in the barrier layer. Electron transport properties in the channel of the device show a strong electrical field dependence discussed before (fig. 2.5 page 11). The source of the channel noise I_{nd} is divided into two parts. Before electrons reach velocity saturation, they contribute to Johnson or thermal noise which is inversely proportional to the drain current [74].

$$\overline{|I_{nd_1}|^2} \sim 4\, k_B\, T_0 \Delta f \frac{|V_p|}{I_{ds}\, r_{ds}^2} \tag{2.35}$$

The second part of channel noise comes from the high-field drift zone. Here, the high-field diffusion constant D_H introduced by Pucel [75] describes the formation of dipole layers that drift through the saturation velocity zone. Drift diffusion noise of the channel $\overline{|I_{nd_2}|^2}$ is proportional to the high-field diffusion constant D_H and the drain current; a high saturation velocity v_{sat} helps to reduce diffusion noise [76]:

$$\overline{|I_{nd_2}|^2} \sim 4k_B T_0\, \Delta f D_H \frac{I_{ds} d_{gc}}{W^2 v_{sat}^3 r_{ds}^2} \tag{2.36}$$

Since both parts of channel noise behave oppositely, there is an optimum drain current for minimum channel noise. Drift-diffusion noise is the more dominating factor for open channel and the optimum drain current is found at comparably low current levels as shown in the left part of figure 2.20 [76]. Fluctuations of the current in the channel are directly transferred to the gate by capacitive coupling and create an additional noise source I_{ng} partly correlated with channel noise. Similar for the gate noise, there are two parts related to thermal and diffusion noise as considered by Bergamaschi in detail [76]. There, the principle noise parameter behavior over the drain current is shown in the right part of figure 2.20, where P and R represent the channel and gate-noise, and C the correlation factor.

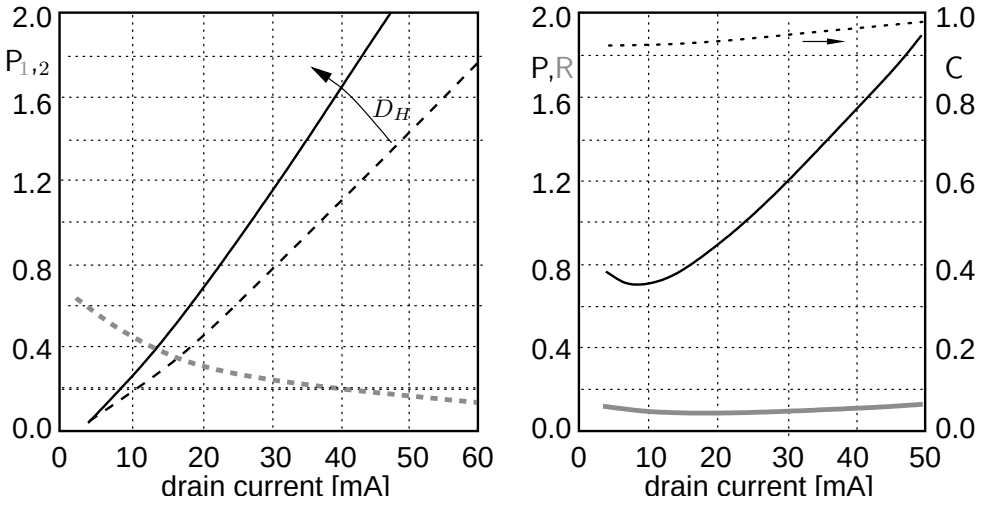


Figure 2.20: Channel noise (l) related to thermal and diffusion noise [76] and noise parameters vs the drain current (r) [76].

Obviously, the channel noise source parameter P shows a significant dependence on the drain current; the channel noise parameter P is significantly higher than the gate noise parameter R. This justifies the omission of the gate noise source for frequencies well below the transit frequency [77] where the gate noise in equation 2.37 is moderate.

$$\overline{|I_{ng}|^2} \sim 4\, k_B\, T_0 \Delta f \omega\, c_{gs}\, R\, \frac{f}{f_T} \tag{2.37}$$

At higher frequencies, the gate noise becomes more dominant and has to be taken into account for an accurate noise model. The RF-noise behavior of the transistor is carried out by noise measurements [78] where the noise figure F is defined in equation 2.38 as a quantitative parameter with relation between the signal to noise ratio $(S_i \,/\, N_i)$ of the intrinsic signal and the amplified signal $(G\, S_i \,/\, (G\, N_i + N_d))$ based on the gain G_d and noise power N_d of the device. For a favorable noise behavior one has to strive for low-noise power and high gain of the device.

$$F = \frac{S_i \,/\, N_i}{G\, S_i \,/\, (G\, N_i + N_d)} \;=\; 1 + \frac{N_d}{G\, N_i} \tag{2.38}$$

Since all RF-noise sources of the intrinsic device show "white" behavior, noise modeling reduces to thermal or Johnson noise based on equivalent noise temperatures. With this, there is the following relationship of the minimum noise figure F_{min} with the elements from the small signal equivalent circuit [79]:

$$F_{min} = 1 + 2\frac{f}{f_{T,i}}\frac{\sqrt{g_{ds} T_d (r_i + r_{gs} + r_s) T_g}}{T_{st}} \tag{2.39}$$

From equation 2.39 it is obvious that a minimization of the parasitic resistors and maximization of the transit frequency helps to reduce the minimum noise figure of the device.

2.3.4 FETs in amplifiers

There is a huge variety how to use a field effect transistor in an amplifier design. To give basic insight about the properties required from the active device [80], the schematic circuit for class-A operation is sketched in figure 2.21. The device is biased with a series inductor L_K to decouple the power supply V_{DD} from the input RF-signal. The input RF-signal is applied to the gate and modulates the drain current. To block the DC-supply voltage towards the output load R_L a blocking capacitor C_K is used which is invisible for the RF-output signal. In the case of amplifier overdrive, generated harmonics are filtered out with the parallel $L_p\,C_p$-circuit.

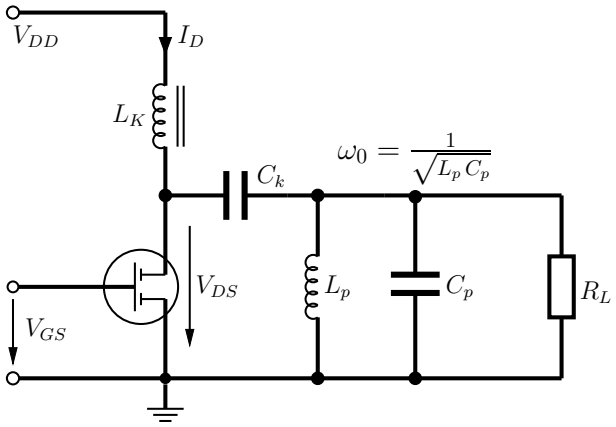


Figure 2.21: Schematic circuit of a class A amplifier.

Biasing conditions (I_{D_0} & V_{DS_0}) for class-A operation of an idealized transistor with constant transconductance are given by the maximum current I_{DS^+}, the knee-voltage V_{knee} and the off-state device breakdown voltage $V_{DS_{max}}$.

$$I_{D_0} = I_{DS^+}\,/\,2 \quad \text{or} \quad V_{GS_0} = V_{GS}(I_{DS^+}/2) \tag{2.40}$$

$$V_{DS_0} = (V_{DS_{max}} + V_{knee})\,/\,2 \tag{2.41}$$

$$R_L = (V_{DS_{max}} - V_{knee})\,/\,I_{DS^+} \tag{2.42}$$

For a resistive load R_L and RF-stimulation at the input, the drain current $I_D(t)$ and voltage $V_{DS}(t)$ are modulated along the straight load line depicted in the output characteristic in figure 2.22. Usually, the optimum performance in noise or power is observed for complex loads causing some phase shift between the modulated drain current and voltage; the load line deviates from the (resistive) straight line and becomes elliptically shaped. In the case of small signal modulation like for low noise amplifiers, the drain current and voltage follow perfectly the stimulation signal amplified by the small signal gain of the device without any distortion.

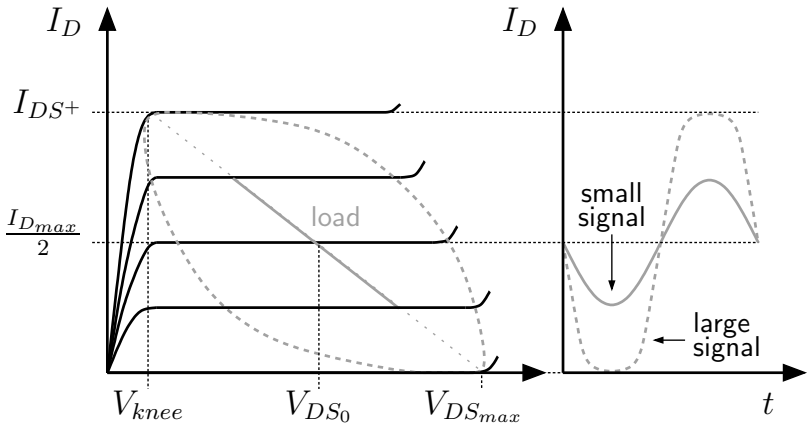


Figure 2.22: FET under small signal operation with resistive load showing a perfect sine-shape output signal I_D. Large signal modulation for non-linear and complex loads leads to deviation from the straight load line. The compressed output signal is linked with the stimulation of higher order harmonics.

Large signal stimulation is the typical case for power amplifiers. The drain current $I_D(t)$ and voltage $V_{DS}(t)$ are modulated along the load line with large amplitude. However, there are limitations of hard clipping at the ends of the load line regarding undistorted amplification of the input signal. At the knee voltage defined by the access resistance of the device, the maximum current level is reached and cannot be exceeded by overdrive. Stronger stimulation only results in an onset of gate current through the forward driven gate-source diode. Similar at the other end, where overdrive pushes the reverse biased gate-drain diode into breakdown. Under clipping conditions, the output deviates from the input signal leading to power in harmonic frequencies. In the worst case, the output is distorted to a rectangular shape. Based on the maximum voltage and current swing, the maximum undistorted RF-output power $P_{RF_{lin}}$ for a class-A amplifier is

$$P_{RF_{lin}} = \frac{(V_{DS_{max}} - V_{knee})I_{DS^+}}{8} \,. \tag{2.43}$$

In class-A, the amplifier consumes DC-power P_{DC_0} under quiescence operation.

$$P_{DC_0} = V_{DS_0}\, I_{D_0} = \frac{(V_{DS_{max}} - V_{knee})I_{DS^+}}{4} \tag{2.44}$$

With this, the power added efficiency η_A of an undistorted class-A amplifier is given by

$$\eta_A = \frac{1}{2}\left(1 - \frac{1}{G_p}\right)\frac{V_{DS_{max}} - V_{knee}}{V_{DS_{max}} + V_{knee}}, \tag{2.45}$$

and is limited to 50 % for a perfect (zero) knee voltage with a linear large signal gain G_p of the device. Higher absolute output powers can be achieved from class-A amplifiers by overdrive. Yet, additional power is not found in the fundamental wave but in higher order harmonic frequencies. For extreme distortion, the maximum power P_{sat} of an class-A amplifier can be calculated by Fourier-analysis [81] of a rectangular output signal.

$$P_{sat} = \frac{16}{\pi^2}\, P_{RF_{lin}} \tag{2.46}$$

The maximum output power of the overdriven transistor is around 1.6 times or 2.1 dBm higher than the maximum linear output power. Assuming infinity gain, the efficiency approaches asymptotically towards 81.5 %. In reality, efficiency versus input power shows a maximum since the output power of a finite gain device does not increase linearly at high input power.

In order to achieve high output power, the FETs have to provide high voltage and current swings. Very high frequency applications require optimized RF-gain, and a high maximum saturation current might be more appropriate than a high device breakdown. For lower frequencies, designers prefer to have optimized device breakdown conditions to prevent losses within the resistive matching networks. Anyway, due to complex loads, power devices have to cope with high current and high electrical field conditions without degrading by impact ionization or burn-out.

2.4 Recess configuration

For GaAs-MESFET devices the lateral spreading model, developed by Wemple [82], results in a constant product for the maximum saturation current I_{DS^+} and the off-state breakdown voltage Vbr. This is due to a strong relation between the charge density in the channel and the recess configuration. In contrast to MESFETs, the highly doped cap layer used in HEMT structures to reduce parasitic resistances has to be removed underneath the gate by recess formation in order to realize Schottky contacts of sufficient quality. The performance of the HEMT also depends on the recess configuration, however, the $(I_{DS^+} \cdot V_{br})$-product is not constant due to a less sensitivity of the 2DEG charge density confined in the heterostructure channel. To the first order, the dimension of the recess affects the off-state breakdown voltage of the HEMT. Figure 2.23 shows a section of the drain side recess proposed by Hikosaka [83] to calculate the off-state breakdown of recessed HEMT structures.

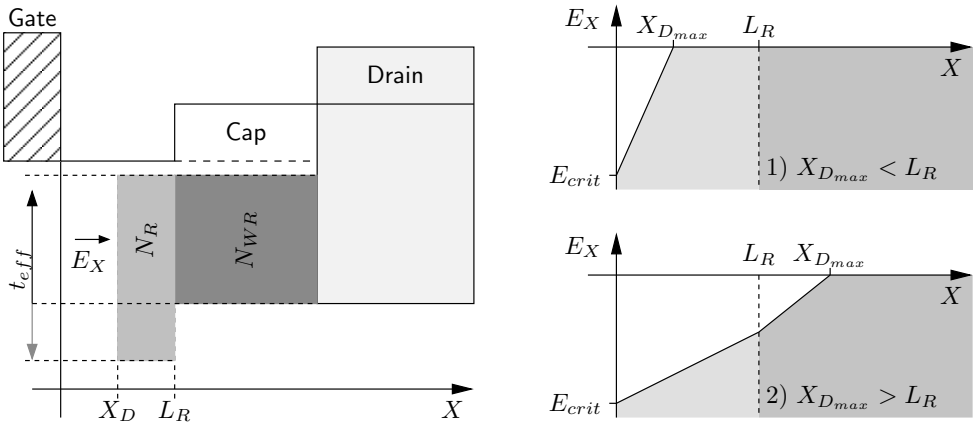


Figure 2.23: Sketch of a HEMT's drain side recess structure (l) of dimension L_R; the two dimensional charge densities N_R underneath and N_{WR} next to the gate recess are distributed over the effective depth t_{eff}. The lateral component of the electric field E_x (r) increases with the expansion of the depletion zone until the critical value for avalanche breakdown is reached; the maximum expansion $X_{D_{max}}$ may be smaller 1) or larger 2) than the recess size.

Calculations are based on the lateral component of the electric field E_x. The extension of the depletion zone $X_{D_{max}}$ is limited by the maximum electric field for avalanche breakdown which is between 400 and 500 kV/cm for GaAs. Since the critical electric field is lower for the $In_xGa_{1-x}As$ channel material with increasing indium content, worse breakdown properties are expected for a metamorphic device compared to the pseudomorphic one for similar charge density and recess configuration. The expansion of the depletion zone depends on the effective two dimensional charge densities N_R and N_{WR} below and next to the gate recess which are transferred into volume densities by the effective depth t_{eff}. Charge densities, again, depend on doping levels but also on the potential at the recess surface which is linked to the barrier material and the density of surface states. At the surface of GaAs and AlGaAs as found in the gate recess of pseudomorphic HEMTs, the Fermi level is pinned close to the middle of the bandgap [84, 85]. Together with the conduction band degeneration at the δ-doping, this forms a vertical electric field causing efficient surface depletion. This built-in electric field can be influenced by surface treatments like oxidation or device passivation. For instance, water rinsing provides a Ga_2O_x enriched surface that lowers the surface charge density and therefore the built-in electric field [86]. The situation is different for InAlAs used for metamorphic HEMTs since surface state densities are too low to force Fermi level pinning at the recess interface [87]. On the right part of figure 2.23, different scenarios are sketched for the lateral component of the electric field under avalanche breakdown. There are two different cases for reaching the critical electric field at the drain side of the gate:

- 1) The maximum extension $X_{D_{max}}$ of the depletion zone may be smaller than the recess dimension L_R; similar breakdown could be realized with a smaller recess showing less parasitic resistance.
- If depletion meets the edge of the recess before the critical electric field is reached, the device breakdown could be increased by a larger recess dimension.
- 2) In the case of a "too small" gate recess, depletion continues in the area next to the recess, and the breakdown voltage depends also on the effective charge concentration N_{WR} and different effective depth. On purpose, this effect is used for power pHEMT technologies having a double recess configuration.

The electric field can be calculated by solving the 1D-Poisson equation in x-direction. For case 1), the maximum electric field in x-direction is reached for a depletion zone smaller than the recess dimension; the maximum lateral electric field is given by

$$X_{D_{max}} = \frac{\varepsilon_0 \varepsilon_r \, t_{eff}}{N_R \, E_{crit}} \, . \tag{2.47}$$

The breakdown voltage V_{br} is calculated by integration of the lateral electric field E_x along the depletion zone and is shown in figure 2.24. With a high constant charge density of $N_{WR} = 5 \cdot 10^{12}$ /cm^2 next to the recess representing a single recess device, the breakdown voltage is calculated as a function of the recess dimension L_R and the charge density N_R below the recess. Considering a large gate recess, the highest breakdown voltage is calculated for the lowest charge density. For a higher charge density, the recess size

is larger than the depletion zone at breakdown. For moderate (500 nm) or small recess (50 nm) dimensions the situation changes. The maximum breakdown is now observed for higher charge densities N_R since the depletion expansion is limited by the recess size due to the high charge density N_{WR} next to the recess area.

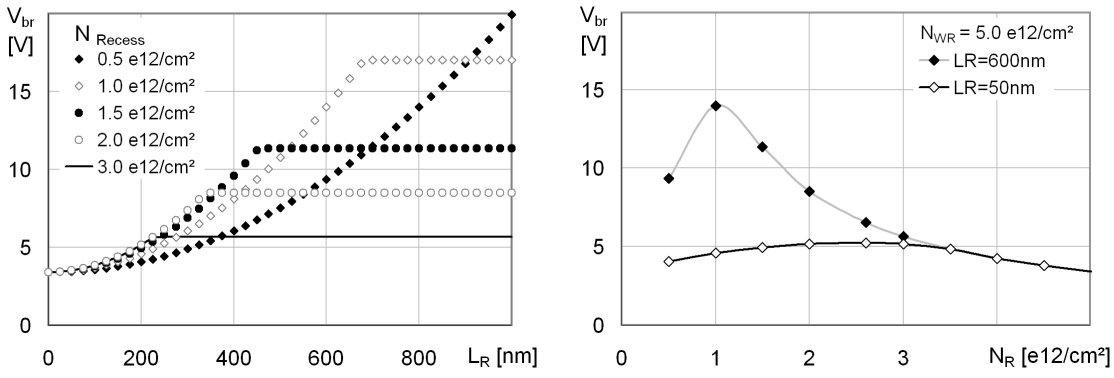


Figure 2.24: Breakdown voltage depending on the size L_R and charge density N_R of the gate recess (l) and comparison for small and large (single) recess configuration (r).

The dependence between the gate recess size and the off-state breakdown performance is confirmed in figure 2.25 for a pseudomorphic HEMT of a 150 nm production technology. Variations of the recess over-etch are small, and the breakdown voltage increases only slightly versus the etch time t_R; the saturation behavior over time indicates the limitation by the charge density N_R in the recess area. Since the breakdown voltage increases more than the maximum saturation current I_{DS+} drops, the not constant $(I_{DS+} \cdot V_{br})$ product for the HEMT is also confirmed by experiment. The impact on the maximum stable gain (MSG) at 10 GHz is rather low since reduction in transconductance and feedback capacitance compensate each other.

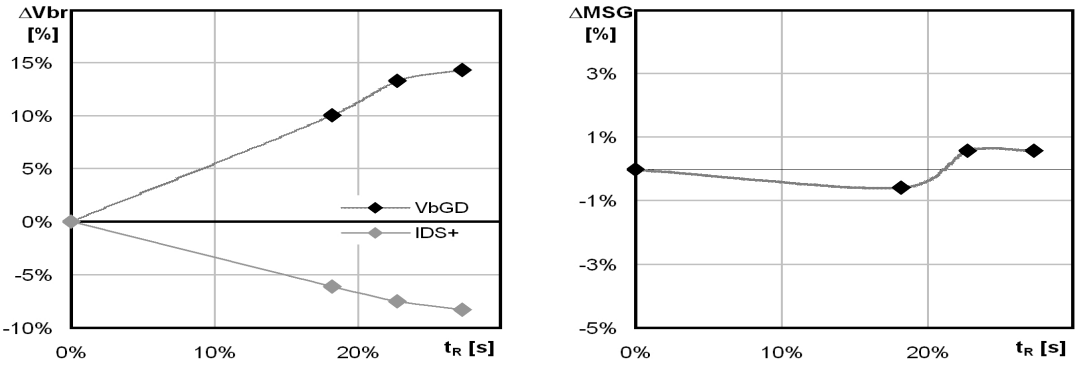


Figure 2.25: Dependence of diode breakdown voltage $VbGD$ and maximum saturation current I_{DS+} (l) from the gate recess etch time t_R on a pseudomorphic single recess HEMT and its effect on the maximum stable gain at 10 GHz (r).

In ideal case, the maximum expansion of the depletion zone corresponds to the recess size. To realize a high breakdown voltage for a single recess device, low charge densities allowing a large gate recess dimension are required. On the one hand, fabrication of a

large single recess is limited by a finite material selectivity of the recess etch process. On the other hand, surface states on the recess area form a parasitic loosely coupled gate and hinder large signal device modulation. This can be detected by current dispersion in pulsed DC-measurements shown in figure 2.26 for a small and large gate recess device of similar gate length. Samples were fabricated on the same wafer by different etch times. For 100 ns pulse duration, the device with the large gate recess shows lower current levels in general that recover with increasing drain voltage due to impact ionization; holes recharge the surface states at the gate recess passivation interface. This is even more pronounced for pulse separation at pinch-off conditions like V_{GS} = -1.2 V and V_{DS} = 2 V, where surface states at the gate recess passivation interface become negatively charged. Comparing the current at open channel between zero bias and pinch-off separation, there is significantly more current dispersion for the large recess device due to the higher absolute amount of surface states that cannot be recharged during the 100 ns pulse. For a longer pulse duration, the differences related to the recess dimension reduce with more efficient recharging of surface states. Since a pulse duration of 100 ns is equivalent to comparatively slow modulation at 10 MHz, a compromise between breakdown voltage and current dispersion has to be found for single recess HEMTs to obtain optimum power performance.

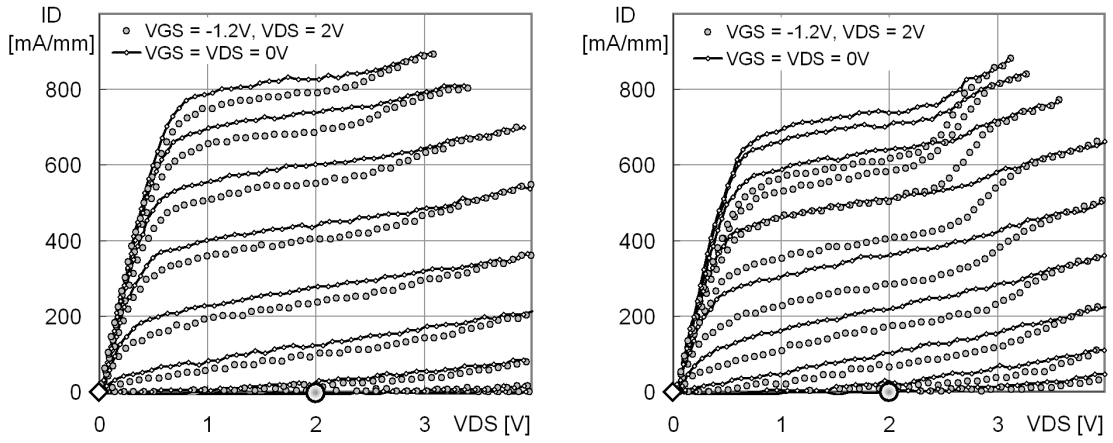


Figure 2.26: Pulsed DC-characteristic (100 ns / 1 ms) of a pseudomorphic HEMT with nominal (l) and doubled gate recess etch time (r). The current dispersion between pinched and zero separation increases significantly with the recess size.

In double recess HEMT technologies, the expansion of the depletion zone penetrates into the area next to the gate recess by purpose and depends on the charge densities below the recess N_R and wide recess area N_{WR}. Assuming a constant effective depth t_{eff} for the gate recess and wide recess area, the maximum expansion of the depletion zone is calculated to

$$X_{D_{max}} = \frac{\varepsilon_0 \varepsilon_r \, t_{eff} \, E_{crit}}{e \, N_{WR}} + L_R \cdot \left(1 - \frac{N_R}{N_{WR}}\right) . \tag{2.48}$$

Again, the breakdown voltage is calculated by integration of the lateral component of the electric field E_x along the depletion zone. For a constant charge density below the

gate recess N_R, the breakdown voltage is shown in figure 2.27 as a function of the gate recess dimension and charge density N_{WR} next to the gate recess. A gate recess larger than $\sim 650\,\text{nm}$ represents case 1), where the maximum breakdown voltage is defined by the charge density N_R below the gate recess. For smaller gate recess dimensions, the depletion zone penetrates into the wide recess area, and the breakdown drops significantly with increasing charge density N_{WR}. The dependence of the breakdown voltage on the gate recess size is smaller for low charge densities N_{WR} in the area next to the gate recess. This allows to reduce current dispersion effects on double recess devices with high breakdown. However, optimization of a double recess power HEMT is still a compromise between the breakdown properties and current dispersion, since low charge density levels in the wide recess area are very sensitive towards surface states.

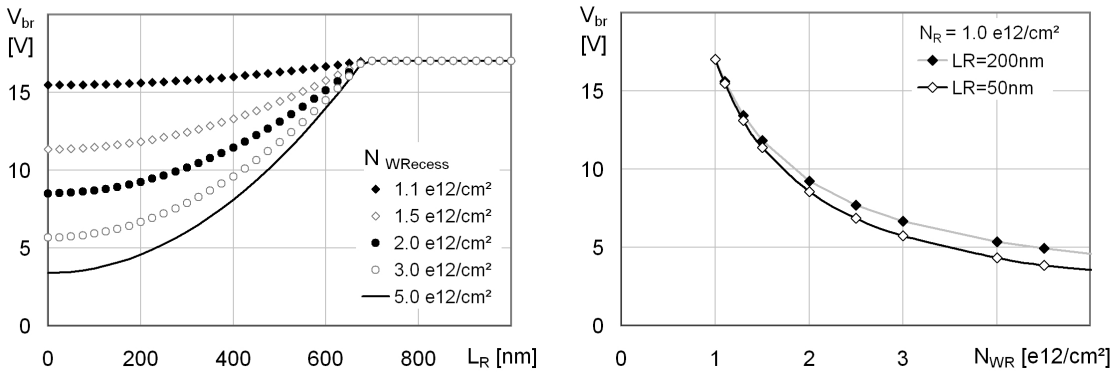


Figure 2.27: Breakdown voltage depending on the size of the gate recess L_R and the charge density N_{WR} next to the gate recess (or wide recess) (l). Comparison of the breakdown voltage for small and large gate recess dimension (r).

Surface treatments like plasma-oxidation, water rinsing or nitride passivation during device fabrication have a strong impact on the surface state density in the recess areas. In contrast to Si-oxidation to SiO_2, several Ga- and As-oxides are formed on GaAs whereas the composition strongly depends on the oxidation conditions. While GaAs-oxidation at thermal equilibrium results mainly in Ga_2O_3 and elemental As [88] - As_2O_5 and $GaAsO_4$ may also be formed - plasma oxidation forms uniformly composed Ga_2O_3 and As_2O_3 in approximately equal composition [89]. However, arsenic oxides and $GaAsO_4$ are not stable and decompose to Ga_2O_3 and elemental As in the proximity of GaAs [89]. Since the different oxide types are linked to different energetic locations, the oxide composition and thickness in the recess area strongly affect surface depletion. Figure 2.28 shows the breakdown voltage and maximum saturation current as a function of the wide recess dimension and different surface treatments. Due to GaAs oxidation of the recess surface by O_2-plasma, charge densities are lowered, and the breakdown is determined by the size of the wide recess. By water rinsing mainly the arsenic oxides are removed, and charge densities in the recess area increase; the breakdown voltage significantly drops compared to the plasma oxidized device. In this case, recess depths or doping levels had to be readjusted to reattain the high device breakdown voltage.

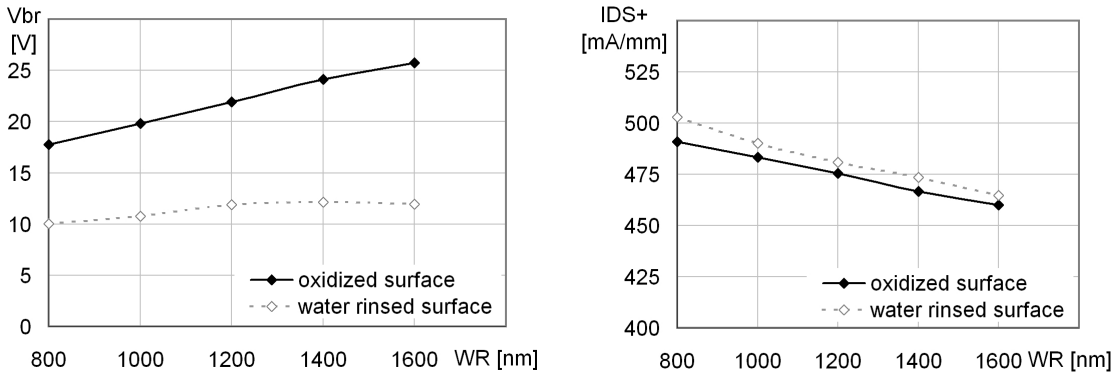


Figure 2.28: Breakdown voltage (l) and maximum saturation current (r) as a function of wide recess dimension for different surface treatment.

Optimization of device breakdown by surface treatment raises some risk linked to the stability and composition of the GaAs-oxide layer. Reliability aspects and current dispersion effects have to be proven carefully. During in-house investigations on double recess power pHEMT technologies the stability of the oxidized wide recess surface has been verified by extensive accelerate life test in on-state, off-state and compressed RF conditions. There is indication that current dispersion effects observed during pulsed DC-characterization

- are not caused by defects formed during gate metal evaporation and lift off,
- strongly depend on surface states related to semiconductor surface treatment and material,
- are not sensitive to charge screen layer thickness ($d \geq 5$ nm), doping or composition (GaAs or $Al_xGa_{1-x}As$, with $X \leq 25\,\%$),
- are dominated by the gate recess area between the gate foot and screening layer,
- decrease with increasing ratio of the gate length to gate recess dimension (L_g/L_R) and indicate a relation either to the gate recess surface or the epitaxy buffer,
- show similar behavior for different epitaxy buffers grown by MBE or MOCVD.

2.5 Epitaxy structures

After a general discussion on pseudomorphic and metamorphic HEMT epitaxy as sketched in figure 2.29 the epitaxy structures used in this work are presented in this section. All structures have been grown in solid source MBEs on semi insulating GaAs substrates, both with 3”-size at Daimler-Research laboratories and on 4” at a commercial epitaxy supplier.

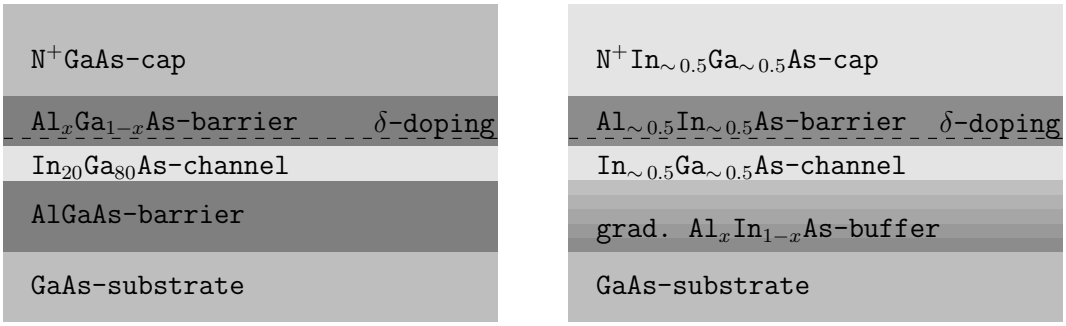


Figure 2.29: Sketched pHEMT and mHEMT epitaxy layer sequence
Sketch of pseudomorphic (l) and metamorphic (r) HEMT epitaxy structures.

A good reproducibility and on-wafer homogeneity is required for production level fabrication. Therefore, calibration of MBE-tools regarding growth rates and doping levels are very important. While the thickness of the layers is monitored in-situ by Reflection High Energy Electron Diffraction (RHEED) sensitive to surface changes on atomic scale, the crystal quality and composition has to be checked after growth by X-ray diffraction. Hall measurements are used to determine the charge density, mobility and sheet resistance.

2.5.1 Pseudomorphic HEMT structures on GaAs substrate

The channel structure of a pseudomorphic HEMT is compressed due to a larger lattice constant of $In_xGa_{1-x}As$ compared to $Al_xGa_{1-x}As$ used for the barrier layers. Since the lattice constant of $Al_xGa_{1-x}As$ is nearly independent of the aluminium mole fraction as shown in the left part of figure 2.31, a high aluminium content helps to increase the conduction band discontinuity and charge density in the channel without suffering from mechanical stress.

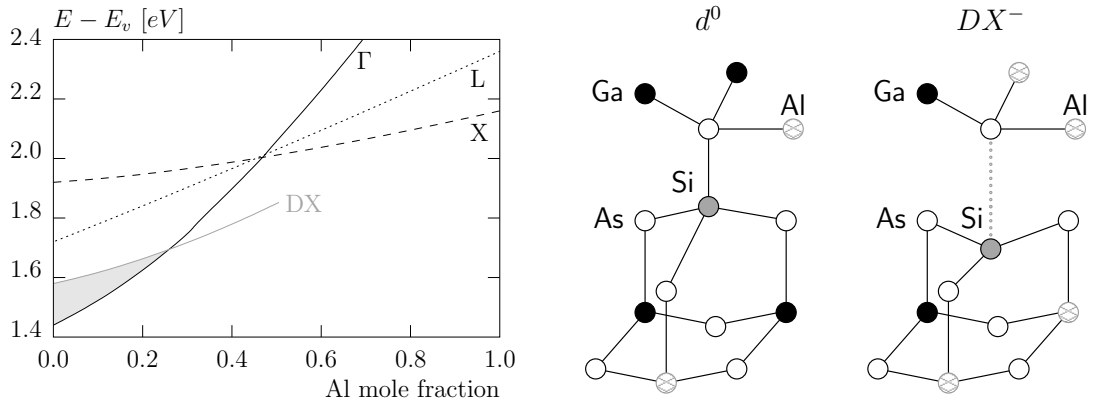


Figure 2.30: Energy-level of the DX-state and conduction band minima for $Al_xGa_{1-x}As$ (l) with respect to the valence band [90]. Schematic view (r) of the normal substitutional sites and broken-bond configuration giving raise to the DX-centers in Si-doped $Al_xGa_{1-x}As$ alloys [91].

Yet, above 48 %, there is less benefit due to the transition from direct to indirect semiconductor type. Barrier layers often contain doping elements for charge supply of the channel. Here, a limitation for the aluminium content is related to the donor atom. While

Si-doping desirably results in shallow donor states close to the conduction band minimum, more and more deep states called DX-centers occur for higher aluminium content. In the left part of figure 2.30, the DX-level is shown for $Al_xGa_{1-x}As$ over the aluminium mole fraction crossing the direct conduction band minimum Γ at an aluminium content of 25 %. Above, the lowest energy level for electrons is formed by the DX-center that acts as a deep dopant reducing the effective doping activation level.
The presence of DX-centers causes persistent photo resistivity described in [92, 90]. At temperatures below 100K, DX-states do not release trapped electrons under dark condition resulting in a meta stable state of low electron density in the 2DEG. The trapped electrons, however, can be released by photo excitation and contribute to the conductivity of the device. Since the probability of recapturing is low at low temperatures, released electrons remain free even if the light source is switched off. A microscopic model of the DX-center is given by Chadi [91] describing two stable atomic configurations of the Si-atom within the GaAs or $Al_xGa_{1-x}As$ crystal as sketched in the right part of figure 2.30; an undistorted one just forming the shallow donor d^0, and a distorted one corresponding to the deep DX^- state raising up for increased Al-content. Although the impact on the charge density coming from DX-centers is less pronounced for the high temperatures of device operation, recapturing of electrons becomes more likely and has to be considered as undesired noise source. Typically, an aluminium content below 25 % is established for pseudomorphic HEMTs on GaAs substrate. The conduction band discontinuity, and therefore the charge transport properties can be also improved by lowering the energy gap of the $Al_xIn_{1-x}As$ based channel. Yet, raising the indium content introduces more strain into the quantum well structure, and high quality epitaxial growth becomes limited due to mechanical aspects. The critical layer thickness of low defect density $In_xGa_{1-x}As$ grown on GaAs and InP substrates is given in figure 2.31 as a function of the indium content and is approximated in equation 2.49.

$$h_c = A\,|x - x_0|^{-b} \tag{2.49}$$

Substrate	X_0	A [A]	b [1]	x-range
GaAs	0	8.16	1.24	$0 < x < 0.4$
InP	0.53	10.27	1.23	$0 < x - x_0 < 0.4$
InP	0.53	7.79	1.31	$0 < x_0 - x < 0.4$

Table 2.1: Parameters for the critical thickness of $In_xGa_{1-x}As$ on GaAs and InP substrate.

Usually, pseudomorphic HEMT structures on GaAs substrates are based on 20 to 25 % of indium content with a channel thickness between 10 to 16 nm. Due to optimized low temperature epitaxy growth, the channel thickness can slightly exceed the critical layer thickness h_c. To realize pseudomorphic structures with a high channel indium content in the range of 40 to 65 %, the epitaxial growth has to be performed on an InP substrate which is lattice matched to $In_{53}Ga_{47}As$. Up to an indium content of 80 % based on a graded channel architecture, pseudomorphic HEMTs based on InP substrates have demonstrated excellent low-noise RF-performance [9]. Yet, the customary in trade size of InP substrates is still 3" making this promising approach incompatible to an existing 4" production line.

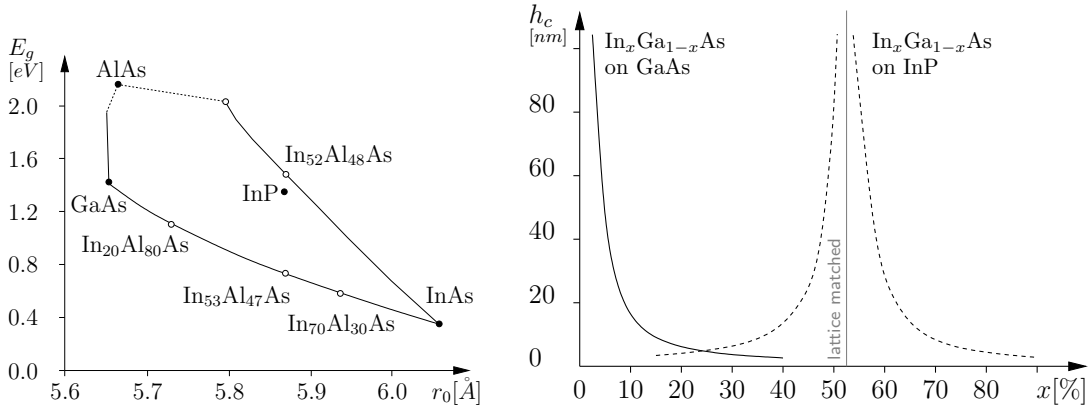


Figure 2.31: The lattice constant and bandgap of common III-V semiconductors (l) and the critical thickness of $In_xGa_{1-x}As$ (r) grown on GaAs- and InP substrates as a function of the indium-content [36].

In order to realize good ohmic contacts and a low device access resistance, pseudomorphic HEMT structures are capped with a highly doped GaAs layer which has to be removed locally by recess for Schottky-contact formation.

2.5.2 Pseudomorphic HEMT epitaxy

Single recess pseudomorphic HEMTs on GaAs substrates with a gate length of 150 nm are used for medium power applications up to 60 GHz [93]. To target for higher frequency applications, the epitaxy structure of an existing and qualified 150 nm-production technology has been scaled down for shorter gate lengths around 90 nm. The layer sequence and band diagram are given in table 2.2 and figure 2.32, respectively.

layer	d [nm]	doping [$cm^{-2(3)}$]	material [%]
cap	50	$> 5.0 \cdot 10^{18}$	GaAs
etch stop	1.5		AlAs
Schottky	4		GaAs
barrier	12		$Al_{25}Ga_{75}As$
Si-pulse		$4.5 \cdot 10^{12}$	
spacer	2		$Al_{25}Ga_{75}As$
channel	12		$In_{25}Ga_{75}As$
spacer	2		$Al_{25}Ga_{75}As$
Si-pulse		$1.5 \cdot 10^{12}$	
barrier	90		$Al_{25}Ga_{75}As$
substrate			GaAs

Table 2.2: Layer sequence of the pseudomorphic single recess power epitaxy.

The indium content of the pseudomorphic structure's channel is 25 %. Two δ-doping plains separated by thin spacers below and above the channel are used for charge supply.

The thickness of the AlGaAs barrier is adapted to the target gate length to keep the aspect ratio. An AlAs etch stop layer allows homogeneous selective recess etching of the highly doped GaAs cap.

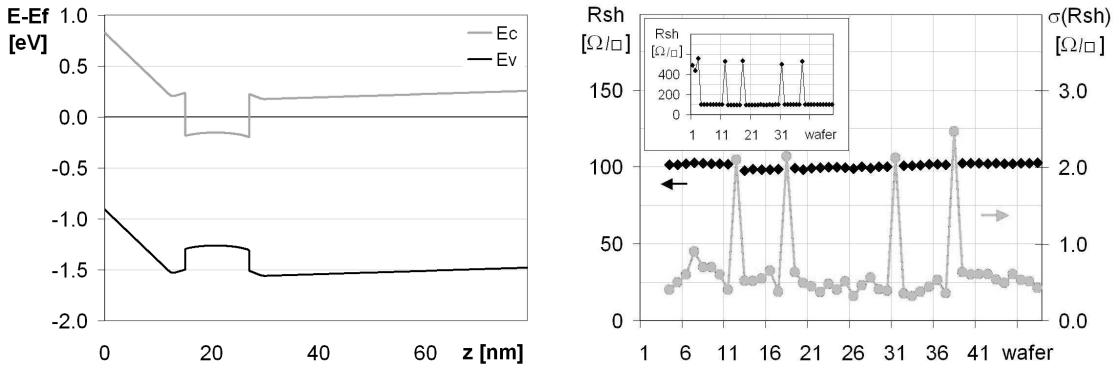


Figure 2.32: Simulated band diagram (c-band [33]) of the pseudomorphic single recess power epitaxy (l) and trend of the sheet resistance (r). Values around $500\,\Omega/\square$ shown in the inlay-box represent wafers with removed cap used for MBE calibration.

The simulation of the band diagram in figure 2.32 results in a conduction band discontinuity of $\Delta E_c = 0.42\,eV$. Hall measurements at room temperature result in a sheet carrier density of $n_s = 2.2 \cdot 10^{12}\,/\mathrm{cm}^2$. The electron mobility of $\mu = 6000\,\mathrm{cm}^2/(\mathrm{Vs})$ is typical for the 25 % channel indium concentration of the pHEMT structure. The high bandgap of $E_g = 1.1\,eV$ promises a high breakdown voltage and robustness required for RF-power operation. Contactless measurement of the sheet resistance based on the eddy current technique is used to characterize the homogeneity and reproducibility of the epitaxy material from different growth runs. The trend of the sheet resistance in the right part of figure 2.32 is stable and confirms a high degree of reproducibility for the commercial pseudomorphic HEMT epitaxy. Similar for the on-wafer homogeneity shown in a mapping in the annex on page 141 with a mean value of $R_{sh} = 88.0\,\Omega/\square$, a small range of $1.1\,\Omega/\square$ and small standard deviation of 0.4 % over the 4" wafer.

2.5.3 Metamorphic HEMT-structures on GaAs substrate

Superior transport properties of low bandgap devices are mainly based on a higher mean drift velocity of the channel electrons. As depicted in figure 2.33, $In_{53}Ga_{47}As$ shows a more pronounced velocity overshoot compared to silicon or GaAs and InP. Since pseudomorphic growth on GaAs substrates is limited to an indium content between 20 and 25 %, an alternative approach was pursued, where the large lattice mismatch between the channel and substrate is accommodated by the formation of misfit dislocations within a metamorphic buffer. In order to avoid island formation and the propagation of misfit dislocations towards the active layers, epitaxial growth of the buffer layers is performed at very low temperatures in the order of 300 to 400 °C. Ternary buffer systems based on GaInAs [94, 95] and AlInAs [96, 97] but also quaternary buffer layers based on AlGaInAs

[98] and AlGaSbAs [99] have been proposed with continuous or step grading of the lattice constant. While the transistor performance is similar for AlGaAs and AlGaSbAs based buffers, the quaternary buffer offers the better surface morphology and a lower roughness [100, 101]. However, the control of four effusion cells during MBE-growth is more complex, and the unavailability of high capacity valved antimonide sources makes it difficult to transfer this approach into commercial production.

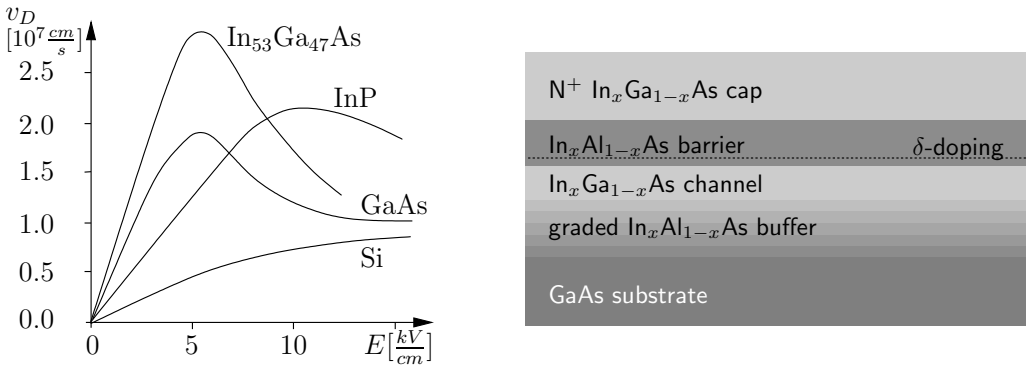


Figure 2.33:
Drift velocities (l) of electrons for several semiconductor materials and sketch of the metamorphic HEMT-structure (r) on GaAs substrate.

In the example of a ternary buffer based on $In_xAl_{1-x}As$, growth starts lattice matched without adding indium. Then, the indium content is increased either gradually or in steps in order to decrease the lattice constant. With increasing thickness of the layers, compressive stress results in misfit dislocations of the crystal causing surface roughness. To lower mechanical strain, the indium concentration is increased during metamorphic buffer growth and finally reduced, again, to the desired value. Due to this so called overgrowth technique, the crystal defects are trapped within the buffer layer resulting in a rough but defect free surface, ready for growth of high indium containing active layers. Due to the metamorphic buffer, the lattice constant of the GaAs substrate is transferred to that of $In_xAl_{1-x}As$. The high degree of freedom for the indium content allows bandgap engineering for the active layers without mechanical stress and limitation of the layer thickness. Metamorphic devices have demonstrated a low-noise performance comparable to InP HEMTs [15, 14] and allow to enter into the lower indium-content range towards the pseudomorphic HEMTs on GaAs as a compromise between superior small signal RF-performance and device-breakdown [16].

Like on pseudomorphic structures based on GaAs, a strained metamorphic structure with increased barrier aluminium content can be used to improve the conduction band discontinuity forming a deeper channel. Similar to the pHEMT structure discussed before, there are also DX-centers in Si-doped $In_xAl_{1-x}As$ layers [102] which stayed unknown for a long time since they behave in resonance with the conduction band for aluminium

contents typically addressed by InP-HEMTs. As depicted in figure 2.34, the DX^--state enters into the bandgap of $In_xAl_{1-x}As$ above an aluminium content of 58 %.

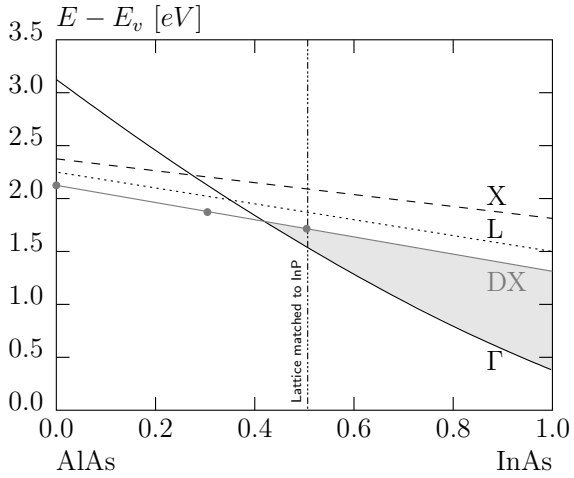


Figure 2.34: Energy level of the DX-center in the InAs-AlAs system.

2.5.4 Metamorphic epitaxy for low-noise devices

Referring to equation 2.39, the low minimum noise figure is mainly related to the high transconductance and transit frequency f_T of the device. For the use in W-band in the range of 70 to 120 GHz, transit frequencies should clearly surpass the upper value of the frequency of application. The layer sequence of the metamorphic low-noise epitaxy is shown in table 2.3. To strive for high cut off frequencies, the structure is based on a single recess and single side δ-doping configuration.

layer	thickness [nm]	doping [$cm^{-2(3)}$]	material [%]
cap	20	$> 6.0 \cdot 10^{18}$	$In_{53}Ga_{47}As$
barrier	8		$In_{53}Al_{47}As$
Si-pulse		$6.0 \cdot 10^{12}$	
spacer	4		$In_{53}Al_{47}As$
channel	8		$In_xGa_{1-x}As$ $53 < x < 70$
	8		$In_{53}Ga_{47}As$
barrier	300		$In_{53}Al_{47}As$
buffer	1000		$In_xAl_{1-x}As$ grad. step-back
substrate			GaAs

Table 2.3: Layer sequence of the metamorphic single recess low-noise epitaxy.

A graded metamorphic step-back buffer is used to overcome the lattice mismatch between the GaAs substrate and the active layers. For a high electron mobility, a mean indium content of 60 % has been selected corresponding to an energy gap of $E_g = 0.66\,eV$. In fact, the indium concentration in the channel is graded from 53 % up to 70 % lowering the channel's bandgap towards the gate; electrons of the first channel sub-band are located closer to the gate compared to a channel of constant indium content. This promises high gain at low current [9]. The band diagram of the metamorphic low-noise epitaxy is shown in the left part of figure 2.35 including wave-functions and sub-bands in the channel.

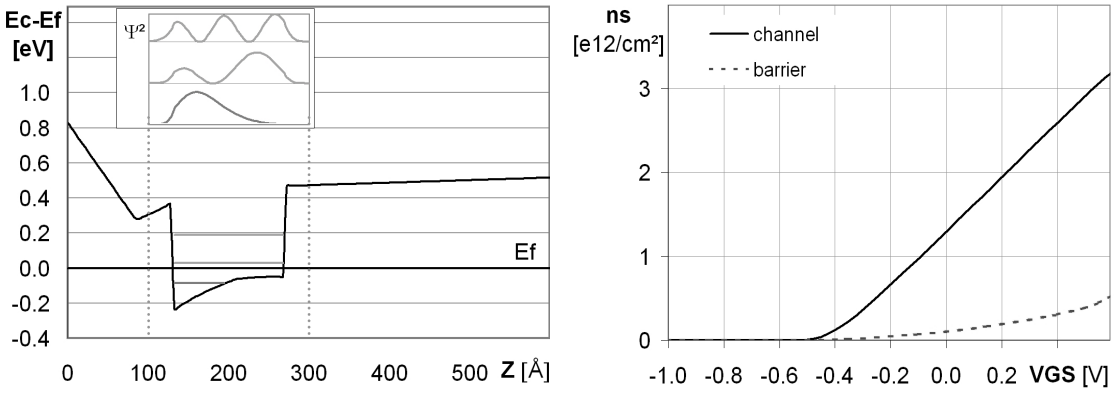


Figure 2.35: Simulations of the conduction band E_c (l) and the charge density n_s (r) as a function of the gate voltage for the low-noise metamorphic epitaxy (c-band [33]).

There is some strain between the $In_{53}Al_{47}As$ barrier and the channel of 70 % indium content. This increases the conduction band discontinuity at the interface by $0.12\,eV$ to $\Delta E_c = 0.64\,eV$ compared to a lattice matched structure. The higher conduction band discontinuity improves the current confinement and reduces parasitic MESFET effects. The thickness of the barrier has been scaled down for a gate length below 100 nm. For improved recess control, the thickness of the highly doped cap has been lowered to 20 nm. Several growth runs with varied doping level were needed to transfer the epitaxy growth from the 3" MBE of the Daimler-Research laboratory to 4" of the commercial epitaxy supplier. The nominal doping level has been fixed to 6e12 /cm^2. For calibration, test wafers with an undoped cap are required to characterize the charge density and mobility in the channel. In contrast to pseudomorphic HEMT structures, removal of the cap results in strong depletion of the channel. At room temperature, the graded metamorphic channel structure shows a high charge density of $n_s = 4e12$ /cm^2 with a mobility of $\mu = 10000\,\mathrm{cm}^2/(\mathrm{Vs})$. The metamorphic low-noise epitaxy offers a significantly higher charge density and mobility compared to the pHEMT material.
The sheet resistance R_{sh} obtained from contactless measurements based on the eddy current technique is shown in figure 2.36 over several growth runs. Increasing trends for the sheet resistance and the standard deviation hint to a difficult reproducibility of the epitaxy structure. The homogeneity is acceptable over the 4"-diameter with a mean value of

92.8 $\Omega/\square$, a range of 2.5 $\Omega/\square$ and a standard-deviation of 0.5 %. A representative mapping of the sheet resistance is given in the annex on page 139.

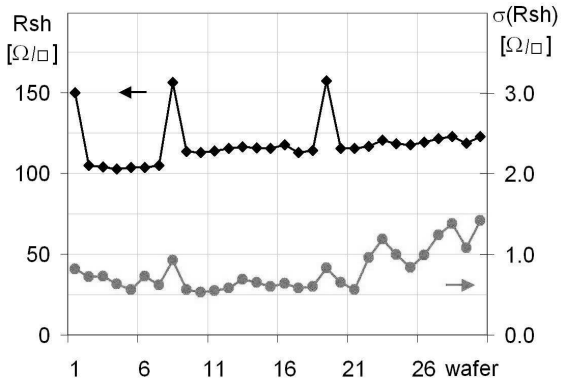


Figure 2.36: Trend of the sheet resistance for the 4" metamorphic low noise epitaxy wafers. Values around 150 $\Omega/\square$ result from calibration structures with un-doped cap.

2.5.5 Metamorphic epitaxy for power devices

Metamorphic structures benefit in their high-frequency performance due to high indium concentrations. However, they suffer in device breakdown, which is important to achieve high output power densities. Two metamorphic technology versions have been investigated to improve the device breakdown properties.

- I) A double recess configuration on a high indium content metamorphic structure to reduce electrical fields as commonly found on pseudomorphic power technologies [103].

- II) A single recess configuration on a metamorphic HEMT structure with reduced (43 %) channel indium concentration; due to the higher band gap, less sensitivity towards impact ionization and a high breakdown voltage are expected [17].

Another option to reduce impact ionization in the channel of the metamorphic device has been proposed C. Gässler of the Daimler-Research group [41] with an InP based sub-channel. However, this option could not be followed in this work due to non-available commercial 4"-epitaxy.

Metamorphic power epitaxy for double recess configuration: Table 2.4 shows the layer sequence for the metamorphic double recess device that has been grown on 3" semi insulating GaAs substrate at the Daimler-Research laboratory. A graded metamorphic buffer is used to overcome the lattice mismatch between the active layers and the GaAs substrate.

layer	d [nm]	doping [cm$^{-2(3)}$]	material [%]
cap	15	$> 6.0 \cdot 10^{18}$	$In_{40}Ga_{60}As$
etch stop	5		$In_{40}Al_{60}As$
charge screen	10	$1.0 \cdot 10^{16}$	$In_{40}Ga_{60}As$
barrier	14		$In_{40}Al_{60}As$
Si-pulse		$5.5 \cdot 10^{12}$	
spacer	4		$In_{40}Al_{60}As$
channel	16		$In_xGa_{1-x}As$ $40 < x < 60$
spacer	4		$In_{40}Al_{60}As$
Si-pulse		$1.5 \cdot 10^{12}$	
barrier	300		$In_{40}Al_{60}As$
buffer	1000		$In_xAl_{1-x}As$ grad. step-back
substrate			GaAs

Table 2.4: Layer sequence of the metamorphic double recess power epitaxy.

There is a graded channel indium concentration from 60 % to 40 % as a compromise of high RF-gain and impact ionization. This corresponds to a channel bandgap from E_g = 0.85 to 0.76 eV as shown in the band structure in figure 2.37.

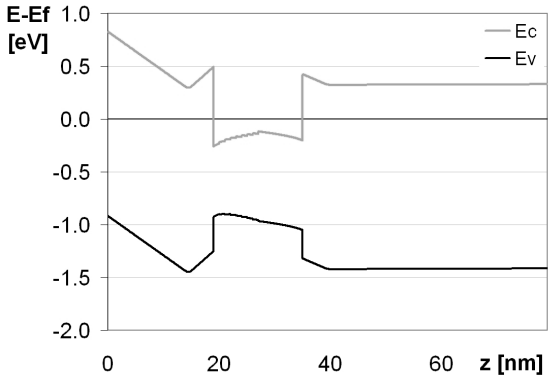


Figure 2.37: Simulated band diagram (SimWindows [104]) of the metamorphic power epitaxy with graded channel and double recess configuration.

Similar to the epitaxy for low-noise devices, the $In_{40}Al_{60}As$ barrier is strained with respect to the channel for a high conduction band discontinuity of ΔE_c = 0.75 eV. Charge supply is realized by two δ-doping planes above and underneath the channel that widen the transconductance characteristic but lower the peak transconductance. The wider range of constant gain over the gate voltage allows a more flexible circuit optimization regarding linear gain, maximum output power and power added efficiency. On top of the barrier, a slightly doped $In_xGa_{1-x}As$ layer is used to adjust the charge density below the wide recess for a high off-state breakdown voltage. In order to realize a good definition of the wide recess an etch stop layer based on $In_{40}Al_{60}As$ is added between the charge screening and the highly doped cap layer. At room temperature, an electron mobility of

$\mu = 8020\,\mathrm{cm}^2/(\mathrm{Vs})$ has been determined by Hall measurements with a sheet resistance of $108\,\Omega/\square$ and a charge density of $n_s = 7.2\,\mathrm{e}12\,/\mathrm{cm}^2$; the very high value for the charge density is related to the highly doped cap. Only few wafers of the metamorphic power epitaxy with double recess configuration have been available for evaluation. The wafer map of the sheet resistance of one representative sample is shown in the annex on page 140 with a mean value of $Rsh = 100.8\,\Omega/\square$, a range of $8\,\Omega/\square$ and a standard deviation of 2.5 %. Compared to the metamorphic low-noise material, the homogeneity of the double recess structure is significantly worse and had to be optimized to comply with production level requirements.

Epitaxy for single recess configuration metamorphic power devices: The strategy to improve the device breakdown voltage is to reduce the channel indium content for an increased bandgap and less impact ionization. The epitaxy layer sequence is shown in table 2.5. Similar to the double recess approach, the indium content of the step-back buffer is raised to 43 %. The indium concentration of the channel is constant corresponding to an even bandgap of $E_g = 0.85\,eV$.

layer	d [nm]	doping [$\mathrm{cm}^{-2(3)}$]	material [%]
cap	15	$> 6.0 \cdot 10^{18}$	$In_{35}Ga_{65}As$
cap	20		$In_{35}Al_{65}As$
barrier	14		$In_{35}Al_{65}As$
Si-pulse		$5.5 \cdot 10^{12}$	
spacer	4		$In_{35}Al_{65}As$
channel	16		$In_{43}Ga_{57}As$
spacer	4		$In_{43}Al_{57}As$
Si-pulse		$1.5 \cdot 10^{12}$	
barrier	300		$In_{43}Al_{57}As$
buffer	1000		$In_xAl_{1-x}As$ grad. step-back
substrate			GaAs

Table 2.5: Layer sequence of the metamorphic power epitaxy with single recess configuration.

The aluminium concentration of the barrier is 65 % and forms a pseudomorphic metamorphic channel as shown in the simulated band diagram in figure 2.38. With this, the conduction band discontinuity is increased by around $0.15\,eV$ to $\Delta E_c = 0.77\,eV$ compared to a strain-free lattice matched structure and is the highest of all epitaxy structures in this work. However, this strategy could be in conflict with the appearance of DX-centers mentioned before on page 40. Like for the double recess structure, charge supply of the channel is realized by double side δ-doping. To reduce the charge density next to the gate recess for improved device breakdown, the cap layer has been divided into a highly doped and un-doped part.

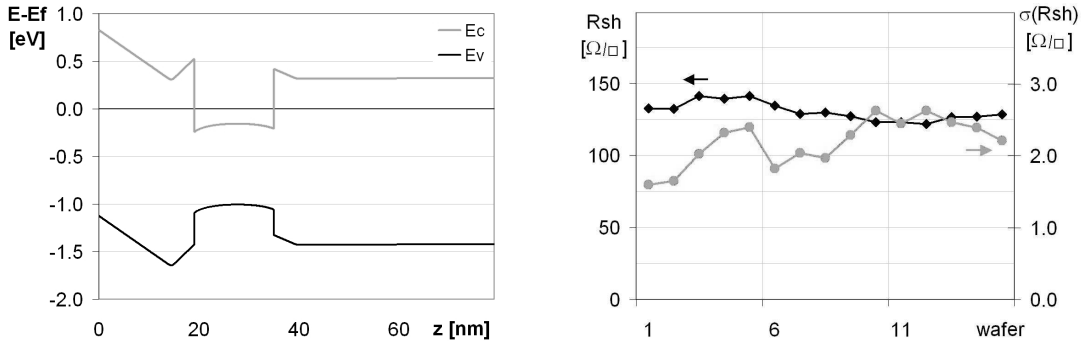


Figure 2.38: Simulated band diagram of the metamorphic single recess power epitaxy (l) and the trend of the sheet resistance R_{sh} (r).

Two growth runs at a commercial epitaxy supplier within five months have been performed. The trend of the sheet resistance in the right part of figure 2.38 shows a mean value of $R_{sh} = 138\,\Omega/\square$ for the first 5 wafers and $127\,\Omega/\square$ for the second epitaxy batch. The large difference of more than $10\,\Omega/\square$ indicates a non-satisfactory reproducibility between the growth runs. Integral Hall measurements including the highly doped cap result in a sheet charge density of $n_s = 6.8\,\mathrm{e}12\,/cm^2$ a mobility of $\mu = 8000\,\mathrm{cm}^2/(\mathrm{Vs})$ and a sheet resistance of $127\,\Omega/\square$. Results are close to the metamorphic epitaxy with double recess configuration but with a higher sheet resistance due to the partly un-doped cap. The sheet resistance has a mean value of $R_{sh} = 123\,\Omega_\square$, a range of $6.7\,\Omega_\square$ and a standard deviation of $5.4\,\%$. This is slightly better compared to the metamorphic epitaxy with double recess configuration but significantly worse compared to the metamorphic low-noise material. A mapping of the sheet resistance can be found in the annex on page 140.

3 Device fabrication

The description of device fabrication can be divided into three parts; the transistor as the active device, the passive elements like resistors, capacitors and inductors, and backside processing. This chapter will focus on the fabrication of the active pseudomorphic and metamorphic HEMTs. A short description about passive components and back side processing is found in the annex on page 153. Depending on the application like low noise or power, similarities and differences regarding processing are discussed for each fabrication level of the pseudomorphic and metamorphic HEMT technologies. Fabrication levels are, incoming control of the epitaxy, device isolation, ohmic contact formation, definition of the gate pofile, recess formation, gate metallization and device passivation.

3.1 Incoming control of epitaxy

Before starting device fabrication, a visual inspection of the epitaxy wafers is performed. Defective wafers having cracks likely break to pieces during fabrication and contaminate production tools. While the surface of pseudomorphic HEMT material is perfectly smooth, metamorphic wafers show significant surface roughness. This is linked to the ternary buffer required to overcome the lattice mismatch between the GaAs substrate and the active layers of the mHEMT. Too strong surface roughness may cause difficulties for the stepper alignment mark detection. The surface roughness of the metamorphic wafers has been quantified by atomic force microscopy (AFM) showing the typical crosshatch pattern in figure 3.1 with a lateral dimension in the order of 1 to 2 μm.

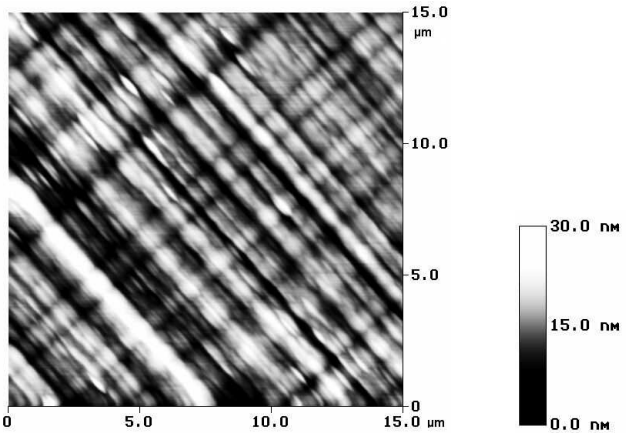


Figure 3.1: AFM-image of the metamorphic epitaxy surface based on the ternary $In_xAl_{1-x}As$-buffer with a channel indium content of 53 %.

Tendencies of the mean surface roughness are shown in figure 3.2 for several mHEMT epitaxy growth runs. For 3" and 4" wafer diameter, the surface roughness has been reduced to 2 nm by buffer growth optimizations. Since marker detection has been proven to work correctly on both ASML steppers for a surface roughness below 10 nm, the surface quality of the metamorphic epitaxy meets production requirements.

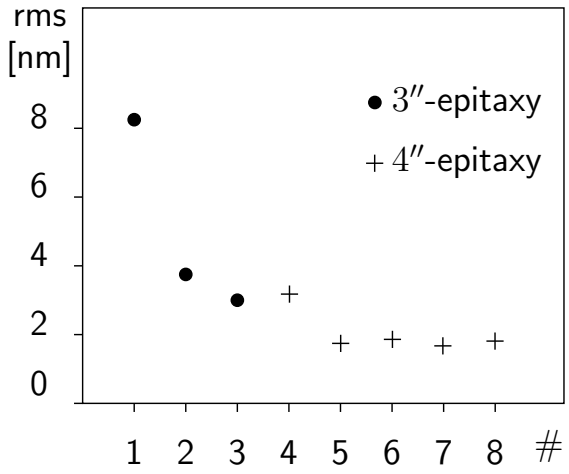


Figure 3.2: Trend of the rms-roughness of 3” and 4” epitaxy from several growth runs.

The different surface quality is already visible by optical microscopy as shown in figure 3.3 comparing wafers with a mean roughness of 8 and 2 nm. Therefore, characterizations of the surface roughness by AFM have been reduced to a sampling of representative wafers from an epitaxy batch.

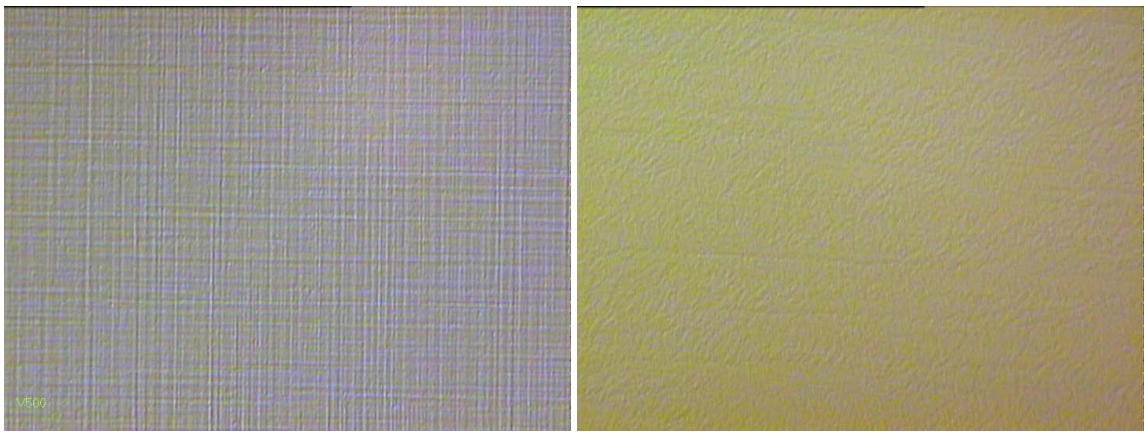


Figure 3.3: Comparison of the crosshatch structure on metamorphic 3” double recess and 4” single recess epitaxy wafers.

Besides surface roughness characterizations, a nano-indentation characterization has been performed at the Technical University of Wildau to compare the mechanical properties of a 1 μm thick $In_{53}Ga_{47}As$ layer grown lattice matched on InP on the one hand and growth on GaAs using a metamorphic buffer on the other hand. Similar properties have been found for both samples as described in the annex on page 155 confirming a good crystal quality for the metamorphic growth of the InGaAs layers. However, nano-indentation is not suited for epitaxy characterization since the layer thickness required is significantly higher than those in the metamorphic HEMT structures.

3.2 Device isolation

Two isolation techniques are common on III-V-semiconductors to define the active areas on epitaxy wafers; ion-implantation [105] and mesa isolation [106, 107]. In this work, boron implantation was used for the pHEMT and mesa etching for the low-noise and power metamorphic HEMT fabrication.

3.2.1 Implantation isolation

The isolation of the pseudomorphic wafers is performed by boron implantation using energy levels in the range of 30 to 250 kV. Figure 3.4 shows the trend of the isolation resistance R_i along a 1.8 mm long comb-structure of 4 μm electrode distance. Stable values above 100 MΩ and a spread in the order of $10\,\%$ reflect the high maturity of this planar isolation technique for the pHEMT technology on GaAs substrate.

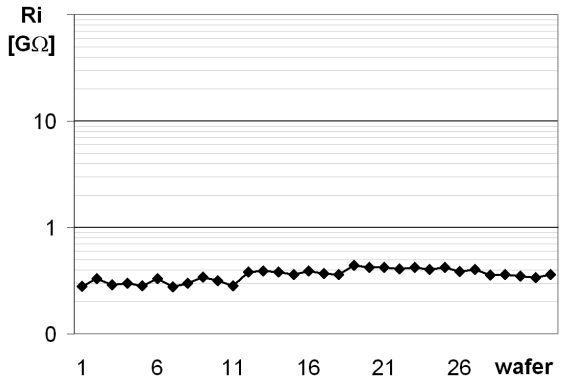


Figure 3.4: Trend of the pHEMT isolation resistance R_i realized by boron implantation.

On metamorphic HEMT-structures, boron implantation fails due to the low bandgap material. Experiments result in a 3 orders of magnitude worse isolation resistance for the low-noise metamorphic epitaxy compared to the pHEMT; this is not sufficient to suppress leakage currents outside the active device. Alternatively, a combination with oxygen implantation is proposed in literature [10]. Fe-implantation [105] especially reduces the conductivity of the highly doped InGaAs cap. Due to incompatibilities with the available implanter regarding above mentioned species, mesa isolation has been chosen for the metamorphic technologies.

3.2.2 Mesa isolation

Mesa isolation is performed in two steps. First, a non-selective wet chemical etch solution is used in an automatic spray etcher to remove the highly conductive active layers like the cap and the channel. In contrast to quaternary metamorphic buffers, the highly insulating $In_xAl_{1-x}As$ buffer does not have to be removed completely, and a depth of 150 nm is sufficient to guarantee a high isolation resistance between neighboring pads.

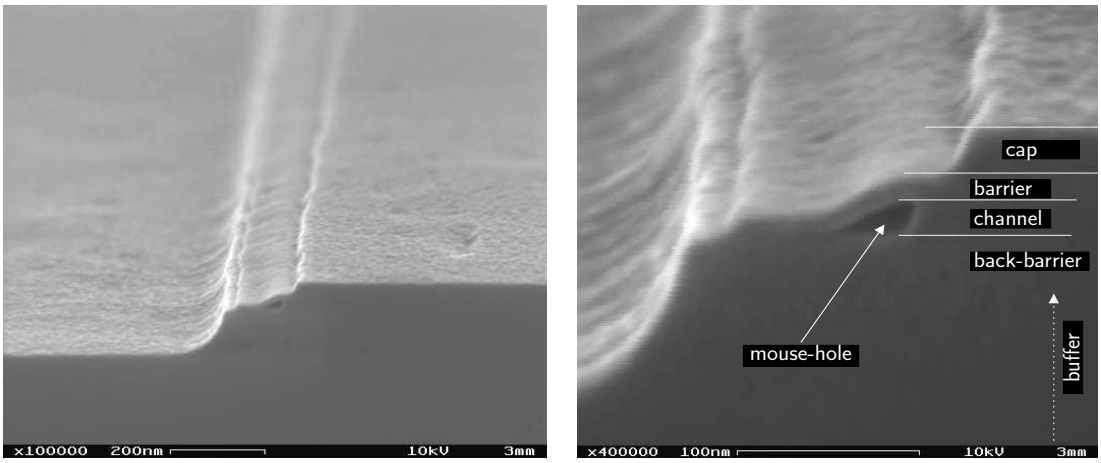


Figure 3.5: Cross section of the isolation mesa; the channel is laterally etched at the mesa edge and forms a mouse hole or micro air bridge (r).

To isolate the gate from the channel, the channel is laterally etched at the mesa edge as proposed by Bahl [106]. A selective etch solution based on succinic acid is used to form this undercut shown in figure 3.5. On the right picture, the upper $In_xAl_{1-x}As$ barrier layer is bent down to the lower barrier forming a mouse hole or micro air bridge.

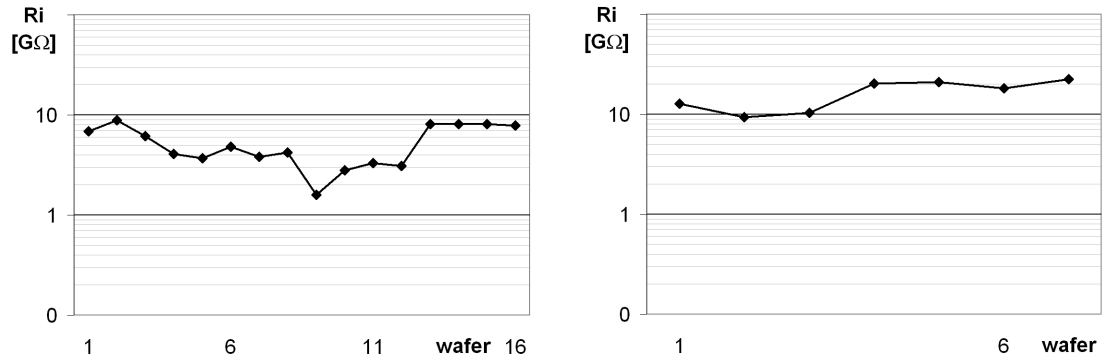


Figure 3.6: Isolation resistance for the metamorphic low-noise (l) and power HEMT (r).

Isolation of the gate towards the channel is needed for both metamorphic technologies independent from low-noise or power operation. For low-noise, a gate leakage at the mesa edge is an additional noise source. For the power technology, gate leakage currents increase with the higher operation voltage. Despite a lower power added efficiency linked to DC-losses at the input, leakage currents at the mesa edge may cause electro migration of the gate metal and may become a reliability issue. Besides this impact on RF-properties or reliability, the breakdown voltage of the device is significantly reduced, especially for a short gate width multi finger device. While isolation between neighboring contact pads can be easily verified by IV-measurements, the proper functionality of the channel undercut cannot be checked before the end of active device fabrication. The gate recess selectivity, gate metal adhesion and the thermal budget during device passivation combined with different thermal expansion coefficients may destroy the micro air bridge structure causing excessive gate leakage currents. The trends of the isolation resistance

R_i are shown in figure 3.6 for the metamorphic low-noise and power technology. An isolation resistance above 1 GΩ is obtained for the metamorphic low-noise material. The higher value above 10 GΩ for the metamorphic power device wafers is linked to the higher aluminium concentration in the buffer. Fluctuations and spreads around 18 % are related to the depth of the mesa.

3.3 Ohmic contact formation

Ohmic contacts have to assure a sufficiently low specific contact resistance to the intrinsic device to comply with high frequency requirements. Furthermore, they have to provide a certain level of reliability regarding thermal stress related to self heating during device operation. To realize ohmic contacts on n-typed III-V materials, several metallization schemes are proposed by literature based on alloyed and non-alloyed types:

- Alloyed: AuGeNi [108, 109, 110, 111, 112], PtGeAu [113, 114], MoGeInW & NiGeAuAg [115, 116]
- Non-alloyed: TiPtAu [117, 118], WSi [119]

In this work, alloyed ohmic contacts based on AuGeNi are used for the pseudomorphic and metamorphic HEMT technologies. The ohmic contact areas are defined by image reversal lithography and using the lift off technique. The minimum feature size is limited to 1 μm due to undercut requirements for the resist profile. Smallest structures found in the active device have a source to drain distance of 1.5 μm. Non-alloyed ohmic contacts based on refractory metals have also been investigated for the metamorphic low-noise technology and are discussed later in section 3.3.2 on page 58.

3.3.1 Alloyed ohmic contacts

After the definition of the ohmic contact areas, the AuGeNi-based metal stack is alloyed into the semiconductor by rapid thermal annealing [108, 109, 110]. Nickel reacts with the native oxides of the semiconductor surface providing good surface wetting and high uniformity across the contact area. Furthermore, it diffuses out of the NiGe-phase to form NiAs and Ni_2GeAs nano crystals. Germanium atoms substituting Ga sites help to create high n-type doping at the Ni_2GeAs/GaAs interface responsible for a low contact resistance due to a local degradation of the Schottky barrier height. Gold, mainly used for contact reinforcement reacts with out-diffusing gallium and form grains of Au_xGa. The interface between GaAs and the ohmic metalization gets irregular during the inter diffusion process. To obtain a minimized ohmic contact resistance, parameters of rapid thermal annealing like the temperature and time have to be adapted to maximize the Ni_2GeAs/GaAs interface area.
Supplementary thermal budgets during wafer processing or device operation supports the ohmic metal diffusion processes further [108, 120]. Mainly Au diffuses into the GaAs, replacing parts of the low resistive Ni_2GeAs/GaAs interface area. The high Schottky barrier height of the Au/GaAs-phase leads to an increased ohmic contact resistance.

Pseudomorphic HEMT

The ohmic contact metal is diffused into the highly n-doped GaAs cap by rapid thermal annealing at temperatures above 400 °C [109]. Due to the low conduction band discontinuity of 0.2 eV at the cap to barrier interface of the pHEMT, direct contacting of the channel is not mandatory; there is efficient electron transfer by tunneling. A mapping of the contact resistance over the 4" pHEMT wafer and a trend chart are shown in figure 3.7. After optimization of the annealing programm for reduced temperature overshoot, the contact resistance is stabilized at a low ohmic contact resistance R_{co} of around 0.12 Ωmm with a spread below 7 %. The annealed ohmic contact provides a good on-wafer homogeneity and a high reproducibility for the pseudomorphic HEMT.

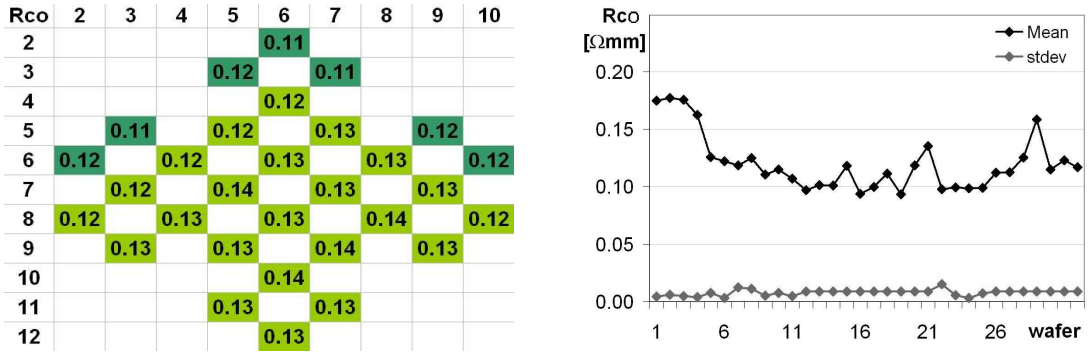


Figure 3.7: Mapping and trend of the ohmic contact resistance R_{co} characterized on pseudomorphic HEMT wafers.

Metamorphic HEMT

The same metal composition has been used to realize ohmic contacts on the metamorphic low-noise and power epitaxy wafers. Due to less experience with the metamorphic material compared to the pHEMT, alloying has been carried out at varied temperatures as shown in figure 3.8. For the metamorphic low-noise epitaxy the optimum annealing temperature is 320 °C. A low contact resistance of $R_{co} = 0.09\,\Omega$mm with low spread is obtained. Due to the low bandgap of the n-type $In_xGa_{1-x}As$ cap and its low surface barrier of around 0.25 eV [121], ohmic anneal temperatures are significantly lower for the metamorphic than for the pseudomorphic HEMT technology.

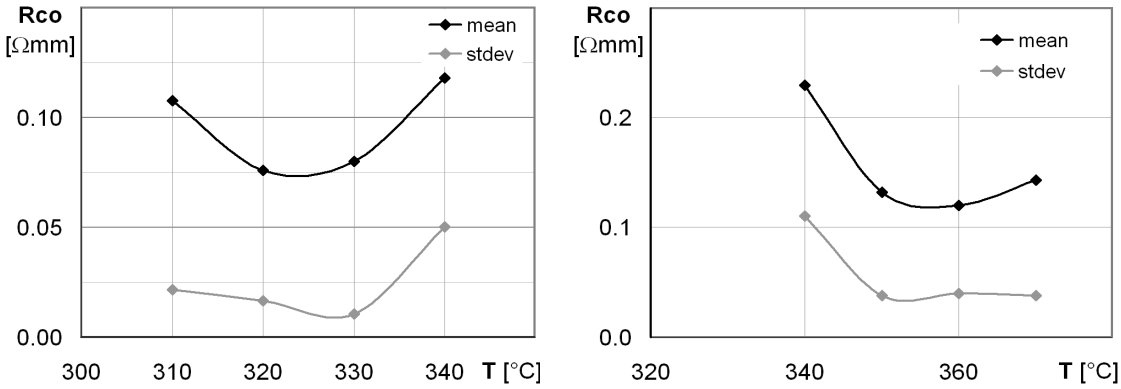


Figure 3.8: Contact resistance R_{co} over annealing temperature T for the metamorphic low-noise (l) and power (r) epitaxy.

With the lower indium concentration of the metamorphic power epitaxy material, the optimum annealing temperature of 360 °C is in between that of the metamorphic low-noise and the pseudomorphic HEMT process; the ohmic contact resistance is 0.12 Ωmm. Mappings of the contact resistance can be found in the annex (Fig B.1 on page 143) showing good on-wafer homogeneities for the metamorphic low-noise and power technology. Trend charts of the ohmic contact resistance are given in figure 3.9. While the metamorphic power epitaxy configuration annealed at 360 °C shows a quite regular trend, the low-noise version annealed at 320 °C shows a group of doubled contact resistance. A clear relation with temperature overshoots during the anneal process was identified as cause of this irregularity and was corrected by slower temperature ramps.

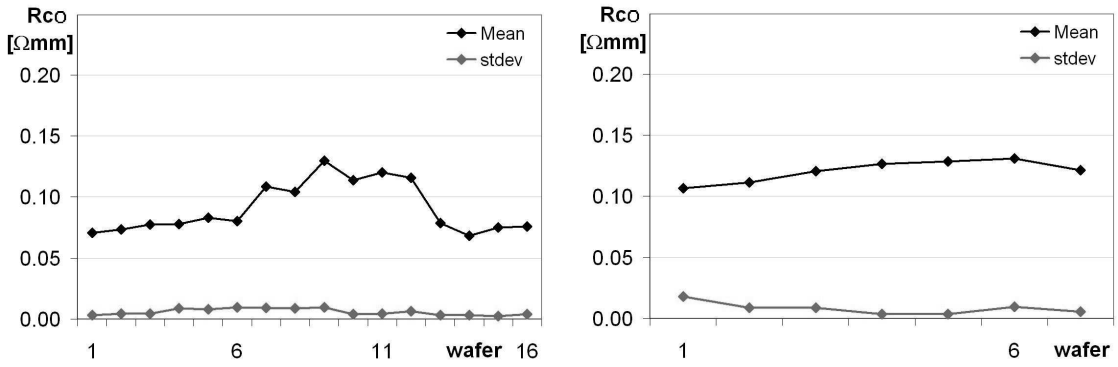


Figure 3.9: Trend of the ohmic contact resistance R_{co} on metamorphic low-noise (l) and power (r) epitaxy wafers.

For optimized annealing parameters, the alloyed ohmic contact based on AuGeNi provides a low and reproducible contact resistance with a low on-wafer spread on both metamorphic HEMT technologies.

3.3.1.1 Thermal stability of alloyed ohmic contacts and Schottky contact

The highest risk concerning reliability of the ohmic contact is expected for the metamorphic low-noise technology linked to the lowest annealing temperature of 320 °C. To evaluate the thermal stability, temperature storage tests in nitrogen atmosphere have been performed on the pseudomorphic and both metamorphic technologies.

Pseudomorphic HEMT

Temperature storage of pseudomorphic HEMT devices has been performed at 275 °C using a completely fabricated (passivated) wafer. The ohmic contact resistance has been extracted from a (non-recessed) TLM structure. Single finger 100 μm test transistors have been characterized regarding key DC-parameters like the maximum transconductance, pinch-off voltage or access resistance. The evolutions of the ohmic contact resistance R_{co} obtained from TLM and the access resistance $R_s + R_d$ of the active device are shown in figure 3.10 over a period of 800 h.

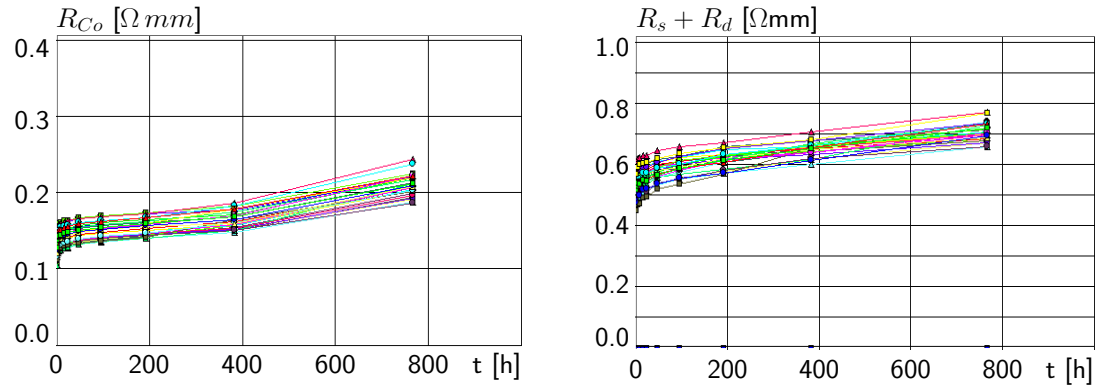


Figure 3.10: Evolution of the ohmic contact resistance R_{co} (l) and access resistance $R_s + R_d$ (r) of a pseudomorphic 100 μm-HEMT during temperature storage at $T = 275\,°C$.

The median value of the contact resistance R_{co} increases by 0.09 Ωmm from 0.11 to 0.21 Ωmm. Being a part of the access resistance, similar degradation is observed for $R_s + R_d$. In fact, the median change $\Delta(R_s + R_d) = 0.177\,\Omega$mm fits well with twice the change of the ohmic contact resistance. Thanks to the SiN_x passivation of the semiconductor surface, there is no significant contribution coming from surface degradation, especially from the gate recess area. A mean time of failure of 680 h is extracted for a failure criterion of $R_{co} = 0.2\,\Omega$mm. Based on a log-normal distribution and an activation energy of $Ea = 1.5\,eV$ obtained from a similar single recess pHEMT production technology [93], a mean time of failure of 93 years has been extrapolated for a temperature of 175 °C. This exceeds the common requirement of 20 years for a power pHEMT-technology. The alloyed ohmic contact based on AuGeNi provides a sufficient level of reliability.
During temperature storage, drift of further transistor parameters has been observed which is not related to ohmic contact degradation but to lowering of the Schottky barrier height. In figure 3.11, the barrier height Φ_b is reduced from 0.67 eV to 0.62 eV.

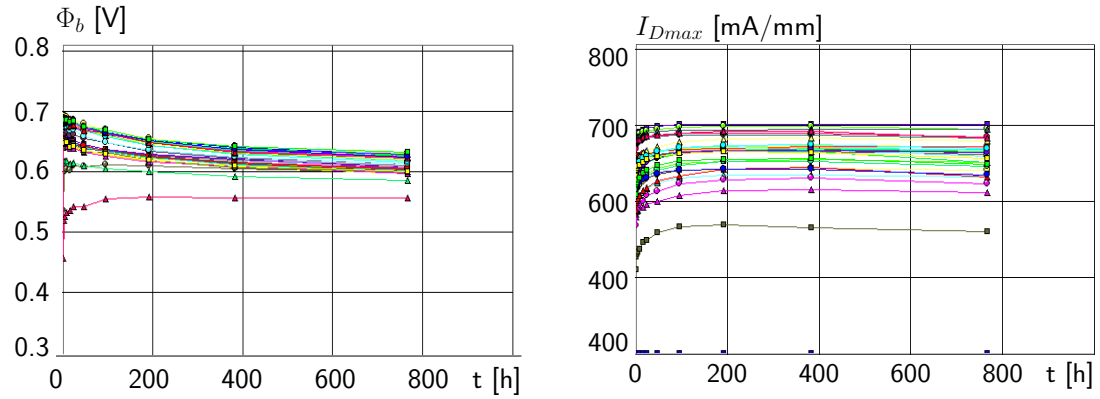


Figure 3.11: Evolution of the Schottky barrier height Φ_b and the maximum saturation current ID_{max} obtained at $V_{DS} = 2$ V and $V_{GS} = 0.7$ V for the pseudomorphic 100 μm test device during temperature storage at $T = 275\,°C$.

This is explained by the TiAl based gate metalization. At first, the Schottky-contact is formed by the Ti/AlGaAs-interface. During temperature storage, Ti reacts with Al to an eutectic ratio of Al_3Ti having a lower barrier height [122]. If storage was continued to a very long time of several thousand hours, the barrier height recovered, again, when titanium completely diffused into the gate metal, and the Schottky-contact is formed by

the Al/AlGaAs-interface. Device parameters linked to the drift of the barrier height are the maximum saturation current ID_{max}, partly the maximum transconductance G_m and the device breakdown voltage V_{bDS}. The effect on the maximum saturation current and transconductance is explained by a slight drift of the pinch-off voltage V_{G100} from -0.51 V to -0.52 V. The device breakdown voltage V_{bDS} is limited by the reverse Schottky characteristic depending on the barrier height.

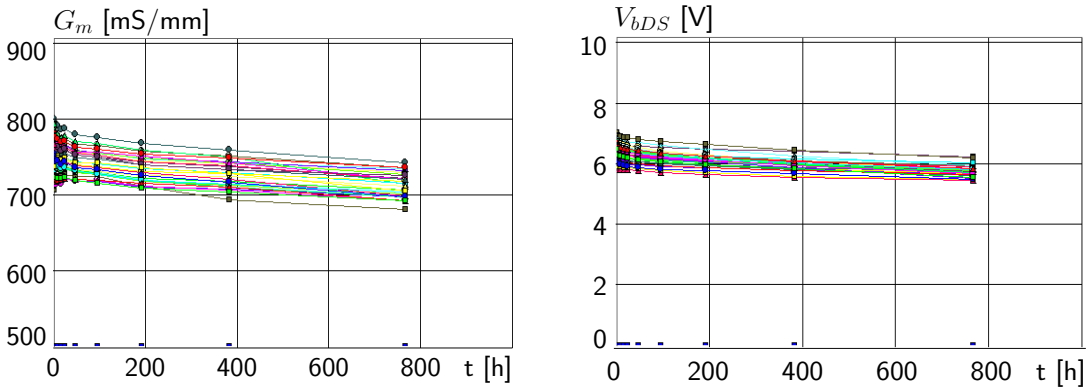


Figure 3.12: Evolution of the maximum transconductance G_m and device breakdown V_{bDS} of the pseudomorphic 100 μm test device during temperature storage at $T = 275\,^{\circ}\mathrm{C}$.

Metamorphic low-noise HEMT

Compared to pseudomorphic HEMT technologies, there is less information about the thermal stability of the ohmic contacts for the metamorphic technology. Therefore, activation energies for ohmic contact degradation have been calculated from storage tests at different temperatures. With the lowest annealing temperature, the metamorphic low-noise devices are to be the most sensitive for ohmic contact degradation. Temperature storage tests have been performed at several temperatures between 200 °C and 275 °C on non-passivated parts of a low-noise mHEMT wafer. For the highest temperature, gold diffusion was observed by microscope as shown in figure 3.13. The initially smooth surface of the annealed ohmic contact is balled-up after 40 hours of temperature storage.

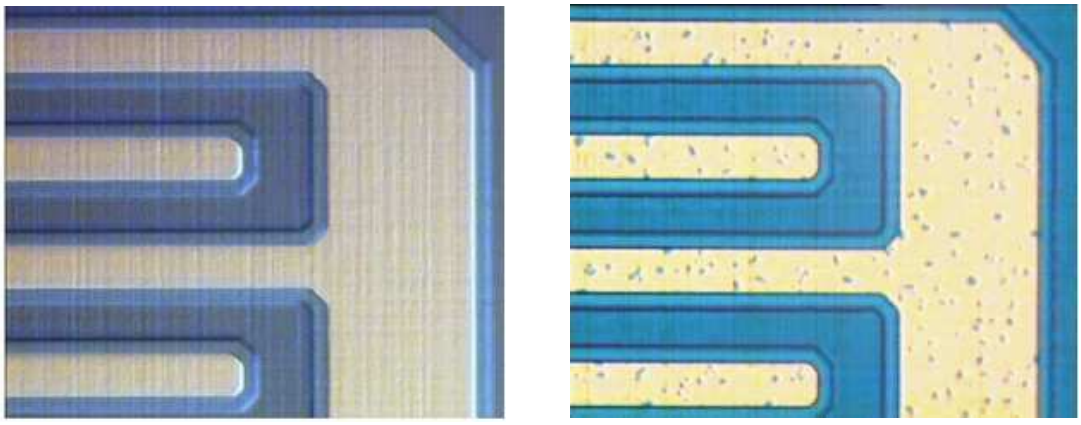


Figure 3.13: Ohmic contact on an isolation test structure of a metamorphic low-noise wafer: annealed at 320 °C for 60 s (l) and after 40 hours of temperature storage at $T = 275\,^{\circ}\mathrm{C}$ (r).

To minimize surface oxidation during thermal stress, a nitrogen atmosphere is provided in the storage oven. Oxidation, however, can not be prevented during unloading the oven when the hot wafer is exposed to air. The evolution of the sheet resistance and the ohmic contact resistance has been extracted from TLM measurements. The sheet resistance remained stable at a value of $98 \pm 2\,\Omega/\square$ and indicates that surface oxidation of the highly doped cap has no significant impact on device degradation. The evolution of the ohmic contact resistance R_{co} is shown in figure 3.14 for the highest temperature of $T = 275\,°C$. Starting at a mean value of $0.085\,\Omega$mm, there is rapid degradation over time. In order to assess the impact of the ohmic contact degradation on the DC-performance of the active device, interim measurements of non-passivated $100\,\mu$m test devices have been performed after each storage cycle. The effect of ohmic contact degradation on the device performance is evident in the transfer characteristic depicted in the right part of figure 3.14. The maximum transconductance and the drain current are significantly reduced after 40 hours of temperature storage at 275 °C.

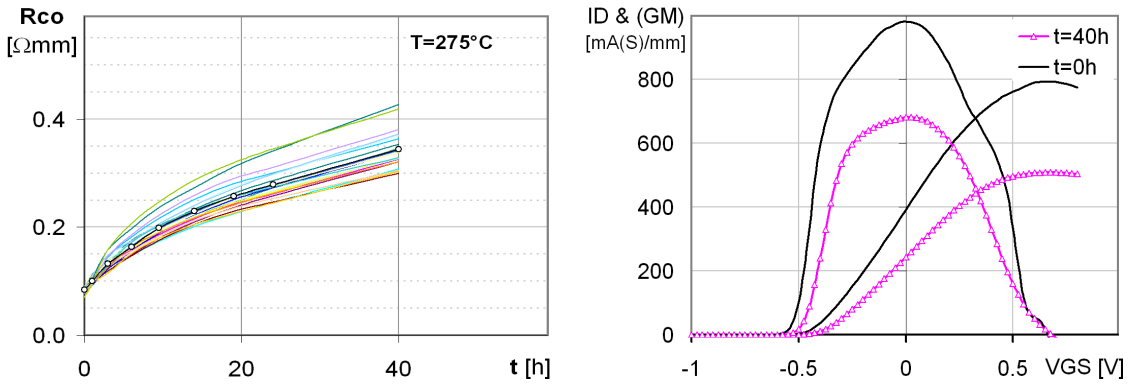


Figure 3.14: Evolution of the ohmic contact resistance R_{co} (l) on a metamorphic low-noise wafer during storage at $T = 275\,°C$ and impact on the transfer characteristic (r) of a 1x100 μm device.

The reduction of the transconductance and the current density are directly linked to the increased device access resistance. In figure 3.15 the trend of the change of the maximum transconductance is presented over the absolute change of the access resistance.

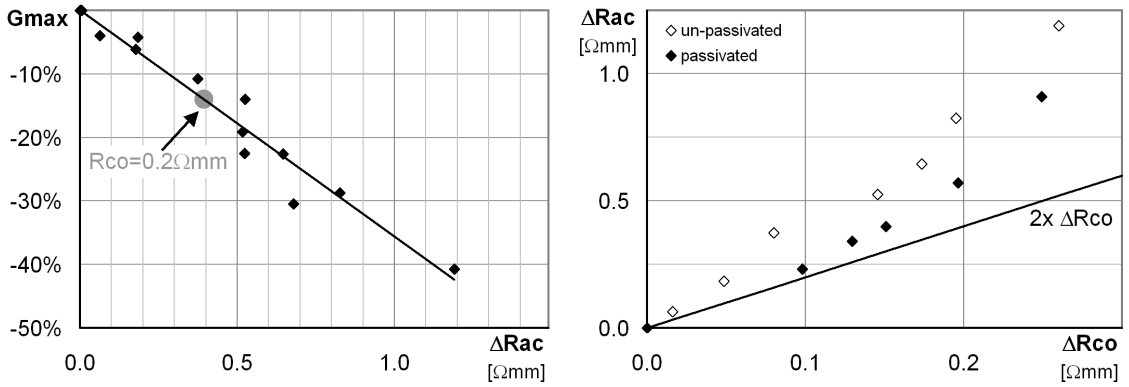


Figure 3.15: Relation between the maximum transconductance G_{max} and the increase of the access resistance ΔR_{ac}(l). Absolute change of the access resistance ΔR_{ac} over the absolute change of the ohmic contact resistance ΔR_{co} (r).

A failure criterion of 15 % for G_{max}-degradation corresponds to an ohmic contact resistance just below 0.2 Ωmm. Since the access resistance is a series of twice the ohmic contact resistance and the contribution of the sheet resistance between drain and source, degradation of the access resistance may not be related to the ohmic contact alone. The absolute changes of the access resistance over the ohmic contact resistance is shown in the right part of figure 3.15. If degradation of the access resistance R_{ac} was only caused by ohmic contact degradation, the absolute change of the access resistance ΔR_{ac} had to be in line with twice the absolute change of the ohmic contact ΔR_{co}. However, the access resistance degrades more than the ohmic contact resistance and may be related to:

- Surface oxidation of the non-passivated gate recess area.
- Change of the effective ohmic contact dimension due to lateral metal diffusion causing errors in the calculation of the contact resistance from TLM characterizations.

To identify the impact of surface oxidation especially in the gate recess area, storage at 275 °C has been performed once again for SiN_x passivated devices. While similar degradation of the ohmic contact resistance was observed, the access resistance degrades less compared to the non-passivated device as shown in the left part of figure 3.15. This indicates that a significant part of the access resistance degradation for the non-passivated device is due to surface oxidation of the gate recess causing a stronger surface depletion. However, degradation of the passivated device still cannot be explained by the change of the ohmic contact resistance alone. SEM inspections of the degraded ohmic contact in figure 3.16 confirm a significant vertical and lateral diffusion of the ohmic metal.

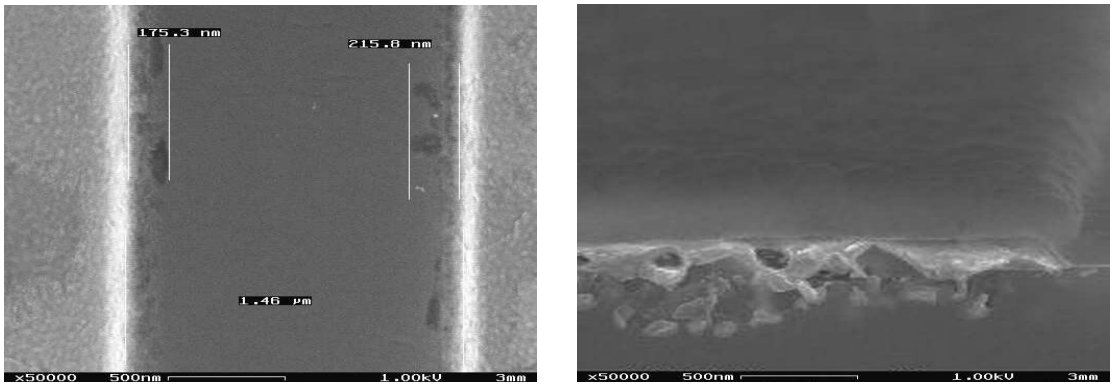


Figure 3.16: Lateral (l) and vertical diffusion of the ohmic contact metal observed on a metamorphic low-noise wafer after 40 hours of thermal storage at $T = 275$ °C.

After 40 hours of storage at 275 °C the effective distance between neighboring ohmic areas is reduced by around 0.4 μm. Taking this into account for the last point of the passivated device, the contact resistance is increased further by 0.2 Ωmm. With this, there is good agreement between the absolute change of the ohmic contact resistance of 0.45 Ωmm and the absolute change of the access resistance of 0.91 Ωmm; there is only a minor impact on degradation related to the gate recess for the passivated device. Based on a failure criterion of 0.2 Ωmm for the ohmic contact resistance a worst case activation energy of $Ea = 1.3\,eV$ has been extracted from different storage temperatures and extrapolation

from semi-log plots. A mean time to failure of 39 years is calculated for a temperature of $T = 125\,°C$. This meets the requirement of 20 years for space applications [123].
To improve the thermal stability of the alloyed ohmic contact, an alternative metal composition has been evaluated for the metamorphic low-noise technology. In contrast to GaAs pHEMTs [113, 114] replacement of Ni by Pt results in the same optimum annealing temperature and shows similar degradation compared to the AuGeNi-stack. Thus, annealed AuGePt-contacts do not improve the thermal stability of the ohmic contacts of the metamorphic low noise technology.

Metamorphic power HEMT
The ohmic contact resistance of the metamorphic power technology is similar to that of the pseudomorphic HEMT. Therefore, the same storage conditions and failure criteria have been used to evaluate the thermal stability of the ohmic contacts. The evolution of the ohmic contact resistance for the un-passivated TLM structure is shown in figure 3.17 stressed at 275 °C and 300 °C. Like for the low-noise mHEMT structure, the sheet resistance remained stable.

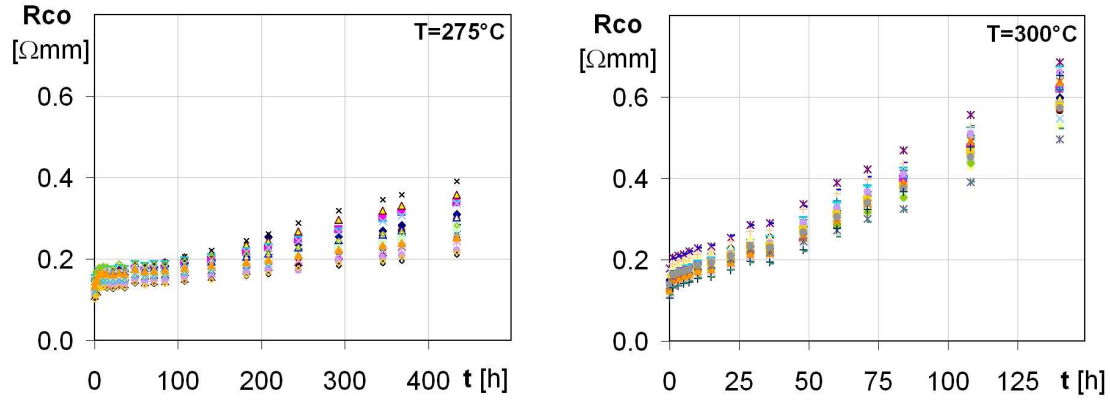


Figure 3.17: Evolution of the ohmic contact resistance R_{co} on a metamorphic power epitaxy wafer during storage at $T = 275\,°C$ and $T = 300\,°C$.

For a failure criterion of $R_{co} = 0.2\,\Omega mm$, extracted mean time to failures are 152.8 and 19.8 hours for 275 and 300 °C, respectively. The calculated activation energy of $E_a = 2.2\,eV$ is rather high. This corresponds to an extrapolated lifetime of 605 years at a temperature of $T = 175\,°C$. Although a better thermal stability was expected for the metamorphic power technology related to the lower indium content, this result seems to be quite optimistic. Based on the 275 °C-result and a worst case assumption for the activation energy of $E_a = 1.5\,eV$, the extrapolated life time is reduced to 21 years.

3.3.2 Refractory ohmic contact for low-noise metamorphic HEMT

In contrast to the GaAs based cap of the pseudomorphic HEMT, $In_xGa_{1-x}As$ used for the metamorphic epitaxy structures shows no or merely weak Fermi level pinning at the interface to air [87]. This can be used to realize non-alloyed ohmic contacts. The successful implementation of non-alloyed contacting has been reported for InAlAs/InGaAs-HEMT

on InP substrates [117, 118]. To evaluate this option for the metamorphic low-noise technology TiWSi has been selected as contact material. Figure 3.18 shows a cross-sectional view of the refractory ohmic contact in a sketch and the electron microscopic picture. Compared to the lift off technique used to define alloyed ohmic contacts, the definition of the refractory contact area is more complex.

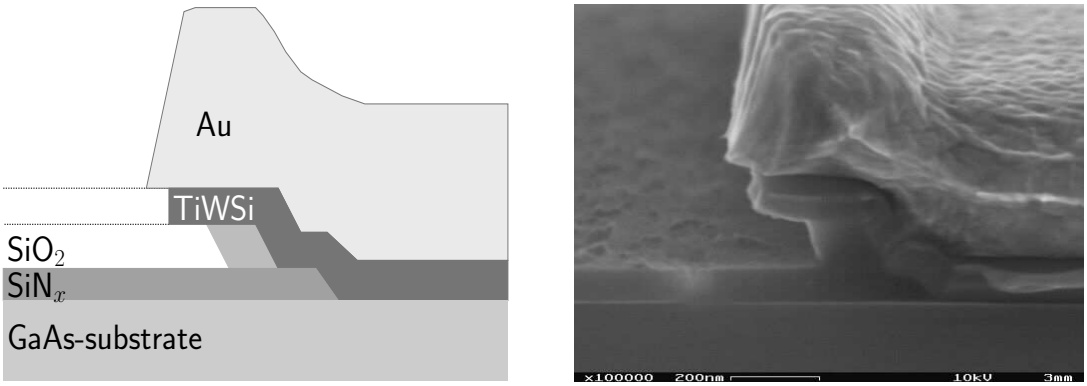


Figure 3.18: Sketch of the refractory contact (l) and SEM-cross section (r).

Due to typically high melting points of silicides, TiWSi has to be deposited by sputtering. However, patterning by the lift off technique results in a poor edge definition because of side coverage of the resist profile. Therefore, back etching of the sputtered material is used. First, a dielectric stack of silicon nitride and silicon oxide is deposited on the whole wafer. At the contact areas, the dielectric film is opened to the highly doped cap by dry plasma etching. TiWSi is sputtered on the whole wafer. The contact area is reinforced by evaporated and lifted gold which is also used as an etch mask for RIE-etching. The silicon oxide layer acts as a sacrificial layer. The etch selectivity between silicon nitride and silicon oxide allows to remove the oxide layer by buffered oxide etch. The remaining nitride layer is used for the dielectric assisted gate technology described later in this chapter.

The refractory metallization shows a significantly higher contact resistance R_{co} of $0.2\,\Omega$mm on the metamorphic low-noise material compared to the alloyed contact version. A good on-wafer homogeneity is confirmed by mapping in the left part of figure 3.19. On the right part, the evolution of the contact resistance during temperature storage at $T = 300\,^{\circ}$C is shown. The ohmic contact resistance of the refractory contact material even improves over 5000 hours.

Rco	1	2	3	4	5	6
1				0.19		
2	0.20	0.20	0.19	0.19	0.18	0.19
3	0.20	0.19	0.20	0.19	0.18	0.17
4	0.19	0.22	0.20	0.19	0.19	0.17
5			0.18			

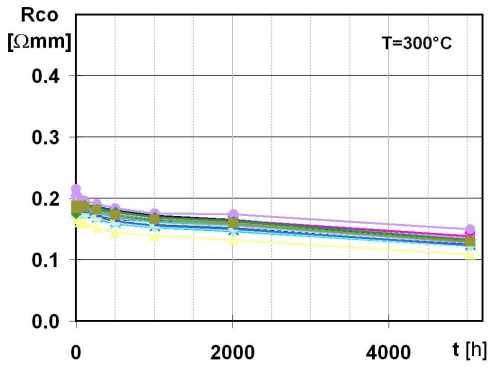


Figure 3.19: Refractory ohmic contact resistance R_{co} (l) and thermal stability at $T = 300\,^{\circ}$C.

The surface of the refractory contact after aging is shown in the left part of figure 3.20. Besides some discoloring indicating recrystallization of the refractory metal material, no metal sinking is observed related to temperature storage.

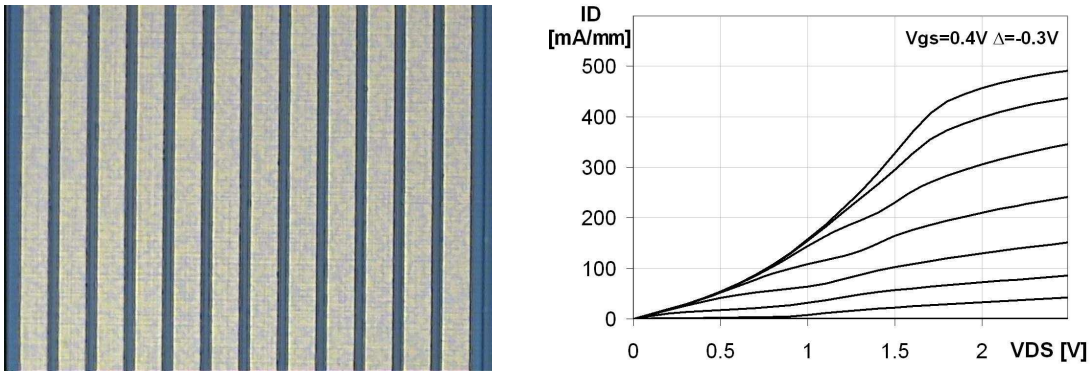


Figure 3.20: The refractory ohmic contact after 5000 h of temperature storage (l) at $T = 300\,^{\circ}\mathrm{C}$. DC-characteristic (r) of a low-noise mHEMT with refractory ohmic contacts.

At a first glance, the refractory approach seems to be very promising on low-noise metamorphic HEMT-structures, however, the channel cannot be connected directly like with the alloyed contact version. Due to a large conduction band offset of 0.52 eV between the highly doped $In_{53}Ga_{47}As$ cap and the $In_{53}Al_{47}As$ barrier layer, there is a significant barrier in the current path which electrons have to overcome by tunneling connected with an exponential IV-characteristic. This is confirmed in the output characteristic of the device in the right part of figure 3.20 showing a diode-like access behavior. A simple (non-recessed) implementation of the non-alloyed ohmic contact results therefore in a non-linear device access resistance. A comparison of the electron current density is given in figure 3.21 by MINIMOS-NT simulations of the non-alloyed and alloyed ohmic contact.

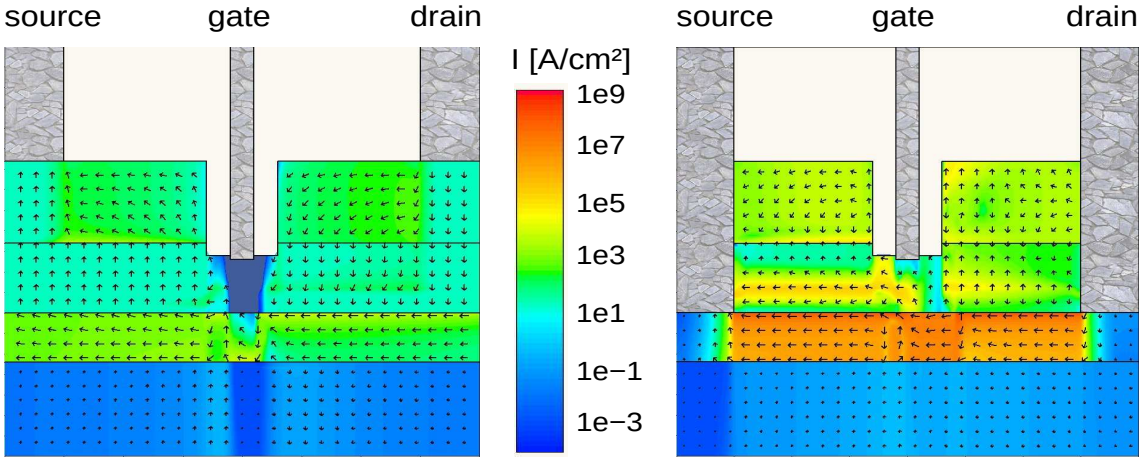


Figure 3.21: Simulated electron current density at $V_{DS} = 2.5$ V and $V_{GS} = 0.4$ V for indirect (l) and direct (r) contacting of the channel for a metamorphic low-noise HEMT structure.

For the same drain voltage of $V_{DS} = 2.5$ V and gate voltage of $V_{GS} = 0.4$ V, there is a much lower current density in the channel in the order of 10^5 A/cm^2 for the refractory contact;

electrons are blocked by barriers formed by the high conduction band offset at the cap to barrier interface. On the right, the channel is contacted directly representing the alloyed ohmic contact. The channel electron current density of 10^7 A/cm^2 is two orders of magnitude higher compared to the non-alloyed contact.
To overcome the high barriers in the current path, high doping of the upper part of the barrier layer combined with InP-etch stop layers are proposed by literature [117]. However, this was not compatible with the supplier of the epitaxy material due to the lack of a phosphorous MBE-source. An alternative solution for direct contacting of the channel is sketched in the right part of figure 3.22 where direct contacting is realized by a recess structure.

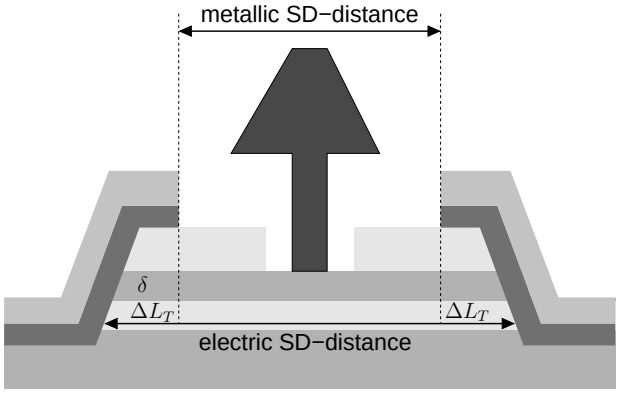


Figure 3.22: Direct contacting of the channel by a recessed structure. Compared to an alloyed ohmic contact the transfer length between drain and source is increased by two times ΔL_T.

Compared to a device with an alloyed ohmic contact, the device with the recessed refractory ohmic contact has a larger transfer length; this is equivalent to an increased drain to source distance. The enlargement in the order of 1 μm depends on the overlay capability of optical steppers and some technological margin. Due to the highly doped $In_xGa_{1-x}As$ cap, the impact on the device access resistance and RF-performance is expected to be lower than 20 %. The recessed refractory ohmic contact might be a temperature stable alternative for the low-noise metamorphic HEMT.

3.4 Gate definition

The gate is commonly defined by electron beam lithography for gate lengths below 500 nm. T-shaped gates help to reduce the gate resistance which is important for high frequency applications. There are two main techniques for T-gate definition by ebeam-lithography as sketched in figure 3.23:

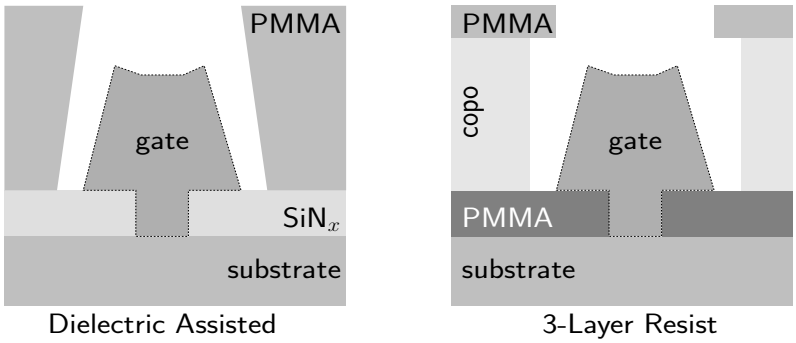


Figure 3.23: Gate definition by the dielectric assisted (l) and the 3-layer resist (r) gate technology.

1) Dielectric assisted technology [124, 125]: Two independent single resist ebeam-exposure steps are required to define the gate foot and gate head separately. The gate foot print is transferred into a dielectric film by RIE etching. To define the gate head, the profile of the second resist has to provide sufficient undercut with respect to the gate metal lift off.

2) Multi-layer resist technology [126, 127, 13, 11]: A resist stack of at least two resist types e.g. PMMA / PMMA-MA is exposed at once, forming the gate foot in the lower less sensitive resist, and the gate head within the top resist of higher sensitivity. To improve the lift off quality, a third resist of medium sensitivity might be used as top resist layer resulting in a box-shaped undercut profile.
In this work, both gate technologies are realized with Leica EBPG systems, where the dielectric assisted technology has been optimized for the needs of the pseudomorphic power HEMTs. A production worthy 3-layer resist technology has been developed to fabricate the metamorphic devices.

3.4.1 Dielectric assisted gate technology

The dielectric assisted technology allows a separate optimization of the gate foot and gate head; alternative shapes like gamma-gates for reduced input capacitance or field plates to improve the breakdown on non-recessed devices can be easily realized. On recessed devices, however, the dielectric film has to be removed after gate lift off for proper surface passivation. Due to the separate lithography steps there are overlay errors between the gate foot and the gate head that may cause an increased device parameter spread over the wafer. A 50 kV single PMMA resist exposure is used for a highly reproducible definition of the gate foot. The resist pattern is transferred into a silicon nitride layer by low ion energy dry etching based on CF_4. The roughly 1 μm thick gate head resist is structured by 20 kV exposure. The negative resist profile required for the lift off technique is realized by

enhanced forward scattering of the electron beam related to the low acceleration voltage. A cross section of the resist profile and its simulation are shown in figure 3.24. There is good agreement between the Monte Carlo simulation performed at XLith (Ulm, Germany) [128] and the shape of the resist profile.

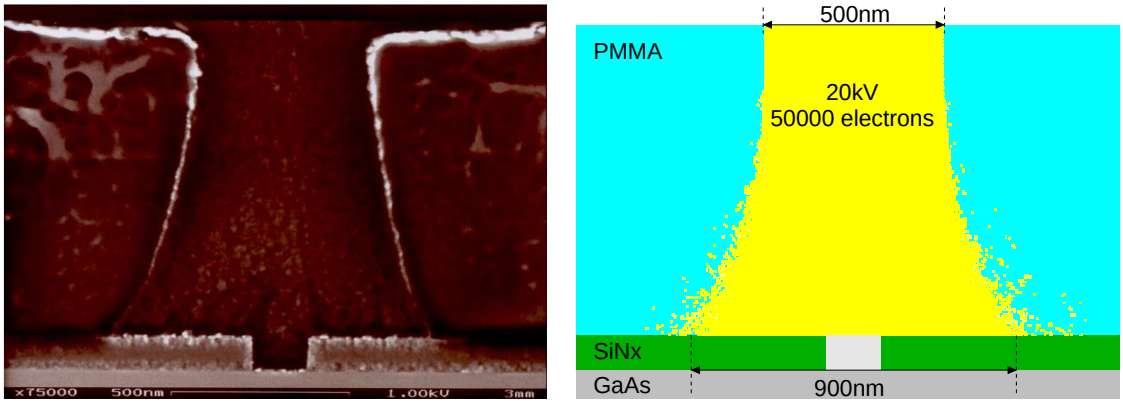


Figure 3.24: Cross section of the gate head resist profile (l) due to forward scattering of the electron beam at 20 kV as calculated by Monte Carlo simulation (r) [128].

While the gate head exposure parameters are similar to existing pHEMT production technologies, the gate foot exposure had to be modified as described below. Both, the nitride opening representing the gate length and the gate head can be checked separately by electron microscopy as shown in figure 3.25. This non-destructive method is very helpful to identify process deviations and to maintain a stable gate technology.

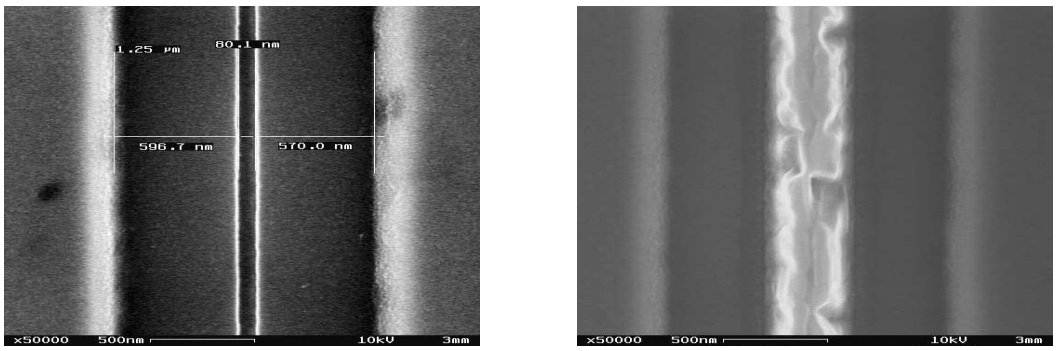


Figure 3.25: Separate, non-destructive SEM-control of the foot opening and the gate head size.

Thanks to little forward scattering in the thin PMMA film, small foot structures in the order of 30 nm can be realized with 50 kV acceleration voltage. However, the aspect ratio of the dielectric film thickness and the gate length should not exceed a factor of around one. A too small gate length will cause improper metalization showing detachments between the gate foot metal and the gate head. On the other hand, the thickness of the dielectric film cannot be reduced to any level, since a minimum gap between the semiconductor surface and gate head is required to ensure proper device passivation after stripping the dielectric film. Therefore, a target gate length between 80 to 90 nm has been chosen for the pseudomorphic power HEMT technology. Several exposure strategies with distinction in dose and resolution have been characterized for process optimization.

The exposure area (main field) which can be covered by the ebeam without wafer holder movement is limited by deflection errors of the electron beam and the resolution depth of the AD-converters of the deflection unit. If not limited by beam distortion, a beam step size or pixel size of 25 nm shows a 6.25 times larger main field area compared to a beam step size of 10 nm. This situation is sketched in figure 3.26 for a virtual 3-bit AD-converter; an unusual spot size smaller than the beam step size is drawn to illustrate the beam distortion as a function of deflection vector.

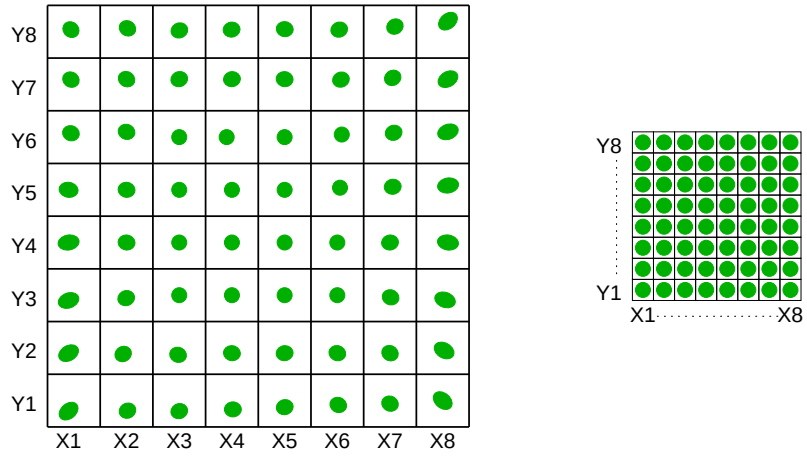


Figure 3.26: Exemplary beam shape distribution as a function of the main deflection field size.

Typically, the spot size is at least twice the beam step size to obtain a clear overlap between neighboring exposed pixels resulting in a regularly defined line in the case of a straight pixel chain. Exposure of a complete wafer requires more time for the small beam step size due to the raised number of table movement steps compared to a 25 nm beam step size. However, a beam step size of 25 nm requires a single line exposure strategy (1x25) to hit the targeted gate length. Although the distribution of the gate length is well centered around a mean value of (90 ± 10) nm in figure 3.28, this fast exposure strategy is most sensitive to deflection errors related to the main field. On some devices, the exposure of the gate line is divided up into two main fields. This is critical if a highly homogeneous resist opening is required. Irregularities like patching errors as shown in figure 3.27 may occur. They depend on the boundary conditions at the main field border which are the placement accuracy of the moving table and the beam shape distortion as a function of the deflection vector.

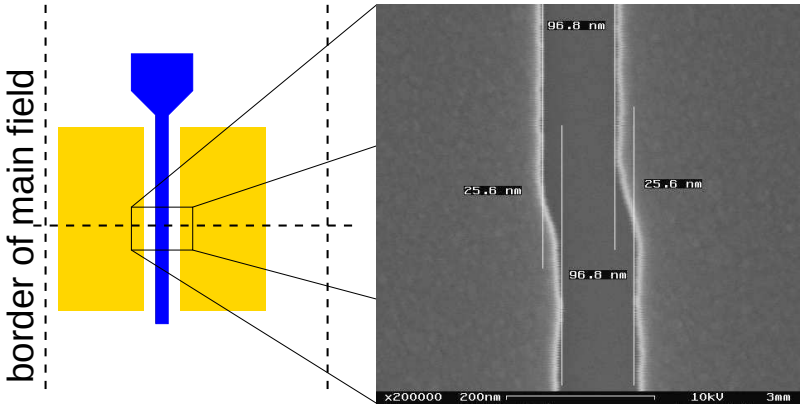


Figure 3.27: Patching error at the border of two main fields.

An interruption of the gate foot opening has to be considered as the worst case for main field patching. However, this was never observed for properly working ebeam tools. For the target gate length of 80 to 90 nm, the best compromise with respect to main field distortion and dose selection is observed for a triple line strategy and 10 nm beam step size.

Compared to optical lithography, ebeam lithography is slower, and production processes have to run on several ebeam tools in parallel to fulfill throughput requirements. Therefore, exposure parameters and specifications have to be sufficiently robust to tolerate fluctuations and drift between several tools. A comparison of gate length distribution in the right part of figure 3.28 obtained from wafers exposed with similar parameters on four different but tightly controlled and maintained Leica EBPG-systems show very similar results which are well centered within a fabrication window between 70 and 100 nm.

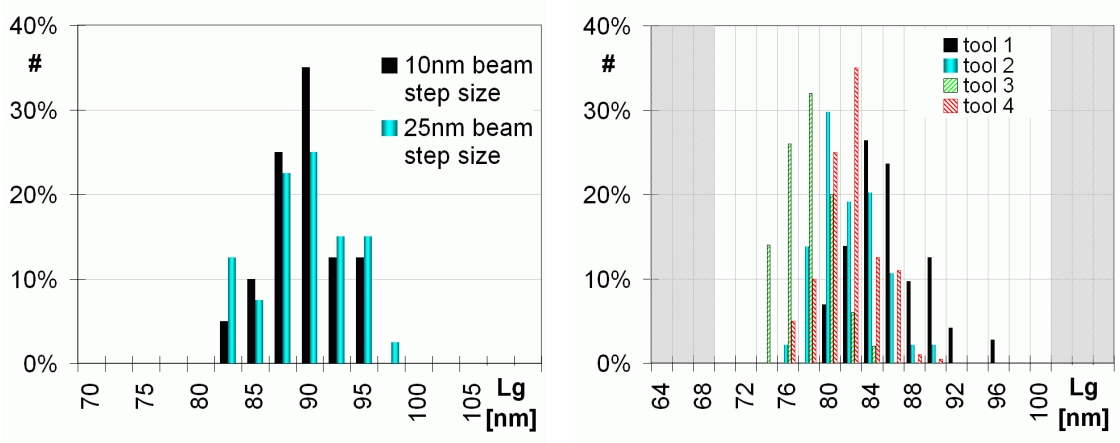


Figure 3.28: Distribution of the gate length for 10 and 25 nm of beam step size (l) and 10 nm beam step size similarly exposed on four different ebeam tools (r).

Together with the trend charts for the gate length and the gate head size in figure 3.29, a high reproducibility is confirmed after switching to the triple line 10 nm pixel size exposure strategy with mean gate length of 84 nm and overall range within 20 nm.

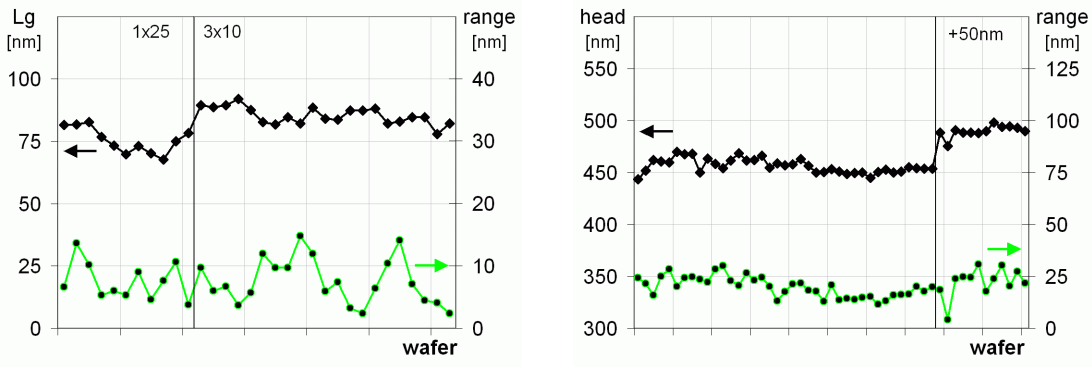


Figure 3.29: Trend charts for the gate length Lg (l) and size of the gate head (r).

Gate yields are evaluated by automatic on-wafer characterizations at the end of wafer fabrication. Therefore, the gate resistance is measured on at least twenty 100 μm and 1500 μm test devices distributed over the whole wafer.

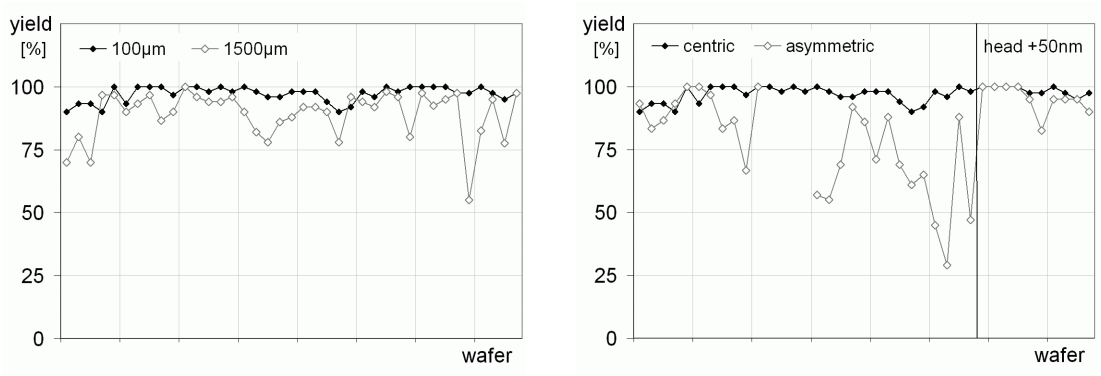


Figure 3.30: Yield of test modules with 100 μm and 1500 μm gate width for symmetric (l) and asymmetric (r) gate configuration.

While the gate yield of both test devices is above 70 % for the standard configuration having a centered gate position between drain and source, poor yields are observed for the asymmetric gate configuration, where gates are moved towards the source contact for a low source resistance. After the gate lift off, gate interruptions have been identified especially on the 1500 μm test device; the yield for the asymmetric gate configuration has been significantly improved by gate head enlargement. The 50 nm larger gate head provides a higher mechanical stability at the cost of slightly increased feedback capacities. With a range of 12 nm for the mean value, an overall range of 19 nm and a typical standard deviation of 3 nm the triple lines 10 nm exposure strategy developed in this work is well suited to realize a gate length of 80 to 90 nm with high yield.

3.4.1.1 Dielectric assisted gate technology on metamorphic devices

The dielectric assisted gate technology was also applied on metamorphic wafers. To prevent degradation of the ohmic contacts, the temperature for the gate nitride deposition has been lowered to 275 °C. After the gate metalization and lift off the dielectric film has been removed by reactive ion etching based on CF_4/O_2 as sketched in the left part of figure 3.31. Strong kinks are formed during gate nitride stripping in the output characteristic of the mHEMT device. The maximum saturation current and the transconductance are reduced by 50 % as shown in the right part of 3.31.

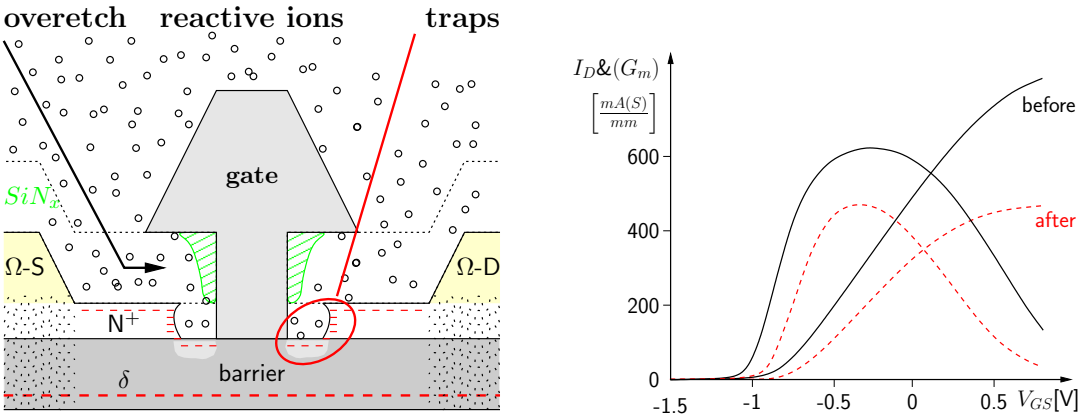


Figure 3.31: Formation of traps on the surface during plasma-based gate nitride removal and its effect on the transfer characteristic of a metamorphic low-noise device.

Due to oxidation of the InAlAs gate recess surface, surface depletion is enhanced reducing charge densities. Some improvement due to less oxidation has been realized with an ICP etch process which allows chemical nitride etching at a lower temperature. However, the result remained unsatisfactory. In contrast to GaAs, the removal of arsenic oxides by water rinse does not change the surface potential of the oxidized InAlAs barrier. The dielectric assisted gate technology is not suited for the metamorphic low-noise technology but might be further optimized for the power HEMT technology since the situation improves with increasing barrier thickness.

3.4.2 3-layer resist gate technology

A multi layer resist technology exposed by direct ebeam writing allows to fabricate T-shaped gates without any plasma related damage or oxidation of the semiconductor surface. Since the gate foot and head are defined simultaneously, the multi layer resist technology provides perfect overlay between the gate head and gate foot. Besides lithography preparation, no advantage concerning process time is obtained compared to the dielectric assisted technology. The gate length and gate head size can be varied separately only in a very limited range. Furthermore, the high thickness of the resist stack limits the minimum gate length due to forward scattering of the electron beam. Intermixing layers found at the resist interfaces result in a more difficult resist development procedure and gate metal lift off.
As mentioned before, there are two common schemes of resist stacks shown in the cross sections of the resist profile in figure 3.32. Both start with the most unsensitive resist which is based on PMMA-950K for gate foot definition. Either a very sensitive PMMA/MA co-polymer resist on the left or PMGI on the right picture are used as second layer. On top, there is PMMA-50K of medium sensitivity in order to define the size of the gate head and to provide the undercut profile required for gate lift off. Compared to the dielectric assisted gate technology described in previous section, the multi layer resist gate technology allows no in-line control of the gate dimensions during device fabrication. Failures or process drift might be identified very late within the production chain. The co-polymer version allows common resist development of all layers at once. However, common development requests a compromise for the gate dimensions and undercut profile. Furthermore, the co-polymer resist shows a short durability, and dose levels have to be readjusted regularly.

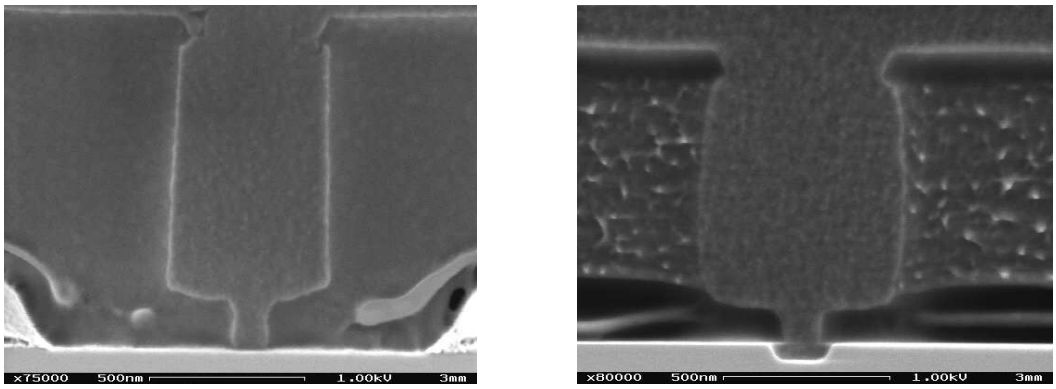


Figure 3.32: Resist profiles: PMMA co-polymer (l) and PMMA/PMGI (r) system.

The PMMA/PMGI/PMMA stack requires a more complex separate development step of each resist layer allowing independent optimization for the head size and gate length. Due to the high selectivity of AZ-based developers towards PMMA, the undercut profile can be well controlled and adjusted by the development time. Although being more complex and with some risk of resist intermixing appearing, the process has been optimized in this work for the metamorphic devices with
- a high degree of controllability,
- excellent long term stability of all resist types,

- and the compatibility to an automatic resist coating system providing a highly reproducible resist stack.

3.4.2.1 Adhesion of resist

To assure a homogeneous start of the gate recess etch process, the opening of the bottom PMMA has to provide a hydrophilic semiconductor surface. An excellent adhesion of the bottom resist is required to form a precise undercut of the gate recess. However, resist adhesion of PMMA on GaAs strongly depends on the surface preparation and environmental conditions like air humidity before and during resist coating. It was found that the same coating procedure on similar epitaxy material resulted in extremely different resist adhesion, if coating was performed in different clean rooms - in most case, insufficient PMMA adhesion was observed causing irregular gate recess formation as shown in the left part of figure 3.33.

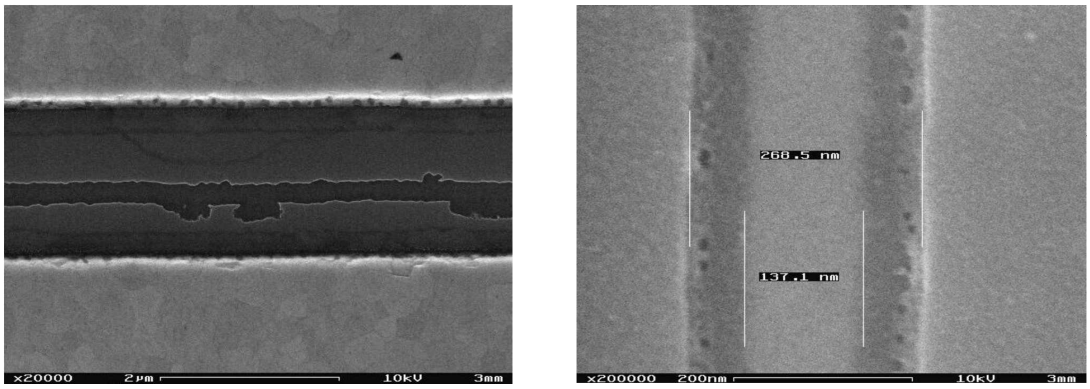


Figure 3.33: Example for poor resist adhesion during the gate recess (l) and residues of adhesion promoter (r) at the edges of the well defined recess groove.

Several adhesion promoters like HMDS, AP1000-3000, OmniCoat and Ti-Prime, deoxidation steps, pre-bake and solvent rinse have been tested without success. Merely a very thin AZ-resist film deposited before PMMA coating helped to improve the adhesion to a reliable degree. However, AZ-resist is hardened by temperatures above 150 °C typically used for the PMMA bake. In the right part of figure 3.33, the hardened and not removed adhesion promoter has a thickness of around 10 nm and prevents proper passivation of the recess area. The adhesion promoter has been thinned down to a thickness of around 1 nm for improved removability.

3.4.2.2 Limitation of the gate length due to forward scattering

Electrons penetrating the ebeam resist show inelastic scattering and loose kinetic energy by cracking polymer chains in the resist; elastic electron scattering results only in a change of the electron paths. Projections of 3D Monte Carlo simulations [128] for single isolated line electron injection and an acceleration voltage from 2 to 10 kV are depicted in figure 3.34, where 100 electrons are injected in 900 nm thick PMMA resist on GaAs substrate. For an electron energy of 2 kV spreading of the beam is observed to a penetration depth of 150 nm. With increased electron energy, the penetration depth increases to around 600 nm

for 5 kV and reaches the GaAs substrate for 10 kV. The shape of the scatter profile within the PMMA changes from circular to conical due to an increased ratio between forward and back scattering.

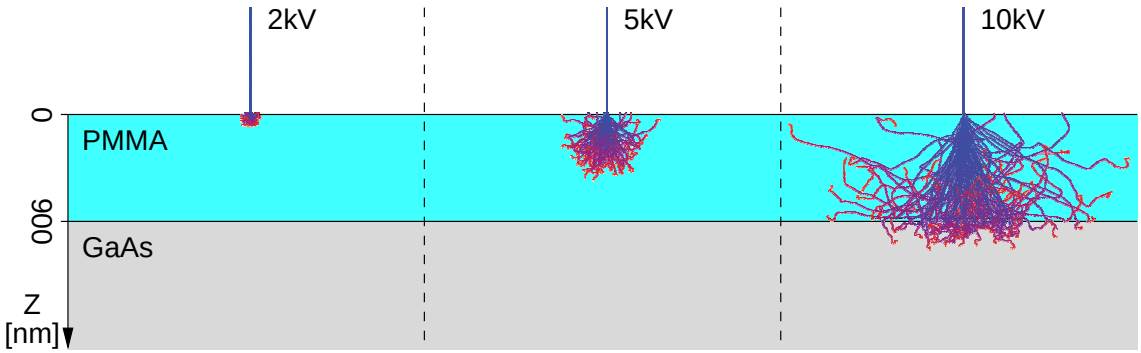


Figure 3.34: Monte-Carlo simulations of forward scattered electrons: $V_{acc} = 2$ to 10 kV [128].

Beam broadening related to forward scattering within the ebeam resist provides the opportunity to realize a negative resist profile as required for the lift off technique. Therefore, the gate head lithography of the dielectric assisted gate technology is performed with an acceleration voltage of 20 kV.

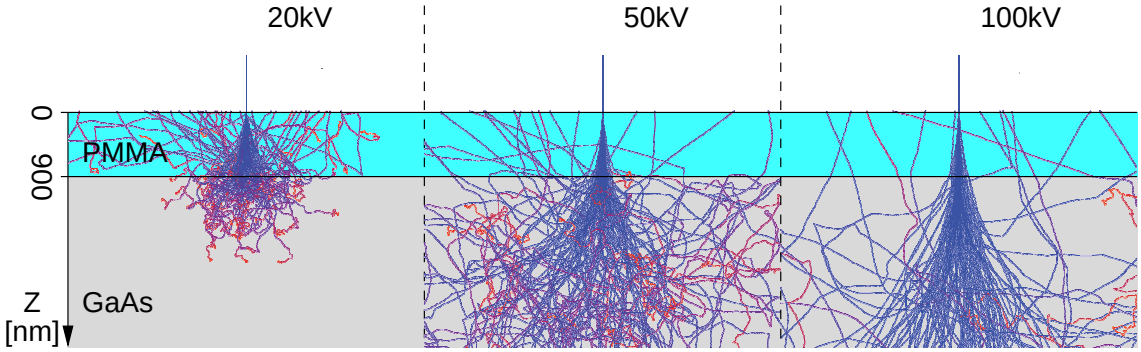


Figure 3.35: Monte-Carlo simulations of forward scattered electrons: $V_{acc} = 20$ to 100 kV [128].

Beam broadening, however, gives some limitation for the minimum achievable gate length in the multi layer-resist gate technology. As depicted by Monte Carlo simulations for acceleration voltages of 10 kV, 50 kV and 100 kV in figure 3.35 for delta injection and figure 3.36 for 100 nm beam diameter, beam broadening within the PMMA resist is lowered for an increased acceleration voltage and is transferred into the GaAs substrate. A fit of the lateral energy density calculated from Monte Carlo simulations over the penetration depth z gives [129]

$$\Delta(z) = k \cdot z^3, \tag{3.1}$$

with the constant k strongly depending on the electron injection energy. For a resist thickness of 900 nm, beam broadening is calculated to 372 nm, 51 nm and 14 nm for acceleration voltage of 20 kV, 50 kV and 100 kV, respectively.

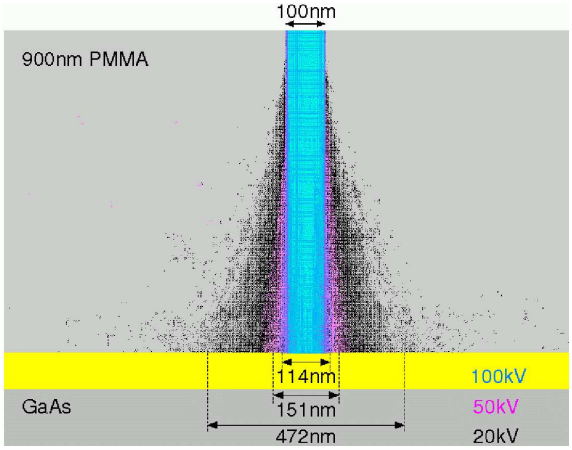


Figure 3.36: Simulation of forward scattering as a function of the acceleration voltage for 100 nm beam diameter and 900 nm thick ebeam resist. Beam widths are defined as full width at half maximum of the Gaussian beam (FWHM).

For a Gaussian electron beam of 50 nm spot diameter, the minimum achievable gate length is estimated to around 420 nm for the 20 kV-exposure, disqualifying low electron energies for the multi layer resist gate technology. Table 3.1 summarizes beam broadening and the minimum achievable gate length Lg for a PMMA thickness of 900 nm and 600 nm.

V_{acc}	$\Delta_{900\,nm}$	$Lg_{\,900\,nm}$	$\Delta_{600\,nm}$	$Lg_{\,600\,nm}$
20kV	372 nm	422 nm	110	160 nm
50kV	51 nm	101 nm	15	65 nm
100kV	14 nm	64 nm	8	58 nm

Table 3.1: Broadening of the lateral electron density Δ and the minimum gate length Lg for 50 nm beam size and 900 nm and 600 nm resist thickness.

To minimize forward scattering, the ebeam exposure might be performed at a higher acceleration voltage. Another optimization parameter is the resist thickness. For instance, the minimum gate length reduces from 101 nm for 50 kV and 900 nm resist thickness to 58 nm for 600 nm of resist exposed at 100 kV. Switching the acceleration voltage requires long stabilization times for the ebeam tool equivalent to a loss of production. Therefore, the acceleration voltage is fixed to 50 kV. A reduction of the resist thickness is automatically linked with a thinner gate metal and a higher gate resistance. Depending on the gate metal composition, like for TiPtAu, this can be accepted without a significant loss in RF-performance. In this work, the gate metalization is based on aluminum, showing a 20 % higher specific resistance than TiPtAu; a reduction of the resist thickness results in a significant drop of the device performance. Due to compatibility reasons with existing pHEMT production processes neither an increased acceleration voltage nor the reduction of the resist thickness were an option limiting the gate length to 120 nm for the metamorphic devices.

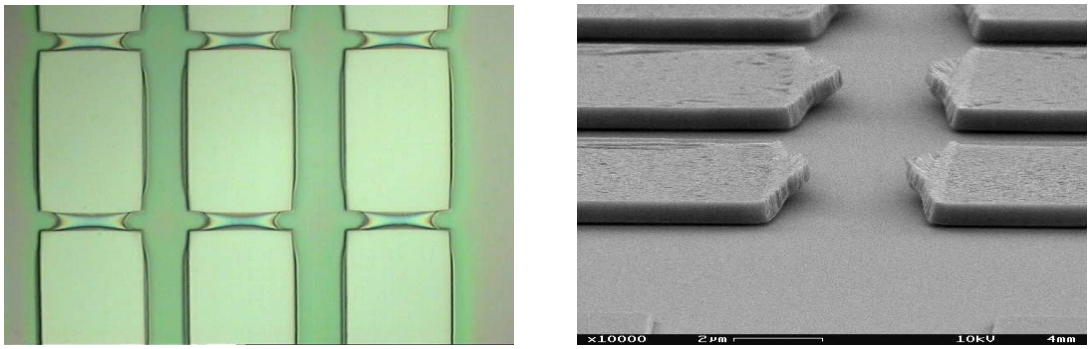
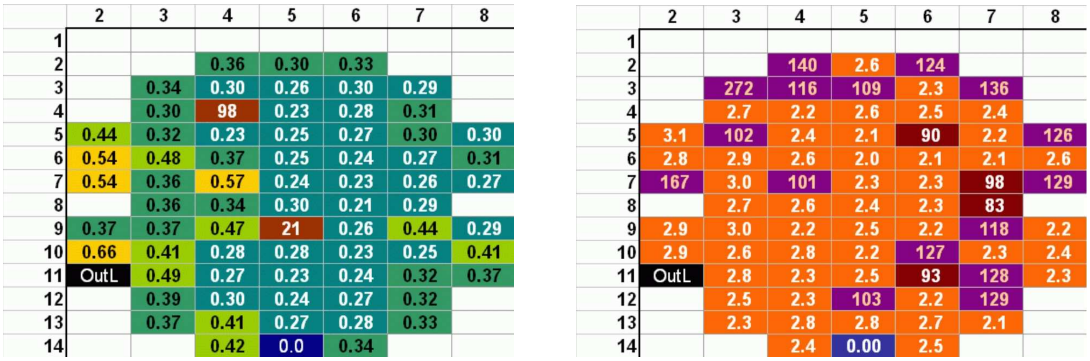


Figure 3.37: Proximity effect on large gate structures: Due to the high electron dose required for the bottom resist and significant back scattering in a 10 μm-area, the more sensitive upper resist is overexposed. Neighboring structures located too close together are not resolved properly (l) and cause a poor definition of the metal structures (r).

The optimization of the multi layer resist technology is often focused on the T-gate structure. Since a high dose is required for the bottom resist, over-exposure is observed on large structures for the more sensitive middle and top resist due to back-scattered electrons spreading up to 10 μm at 50 kV acceleration voltage. Especially the top resist is thinned making it more difficult to provide a good undercut profile. In the case of large openings located closely spaced, as shown in figure 3.37, structures deviate strongly from their ideal form. To prevent such proximity effects, minimum distances have to be defined and taken into consideration for circuit designs. Alternatively, a two step exposure and development techniques has been investigated to reduce proximity effects on large structures but also to reduce the gate length. The two step RIE-free gate module is discussed in the annex on page 159. Since this strategy was not successful regarding gate length reduction, it was not used for the metamorphic device fabrication.

3.4.3 Gate yield: dielectric assisted versus 3-layer resist technology

Fabrication of HEMTs on production level requires a high reproducibility and stability of all processing steps. Since the target gate length differs between the two technologies used in this work, a principle comparison between the dielectric assisted and the 3-layer resist gate technology has been investigated for similar gate length. Well known pseudomorphic HEMT epitaxy from pHEMT production has been used for an increased gate length of 200 nm that provides sufficient margin to the minimum gate length of the 3-layer resist gate module. Since the probability of gate defects is expected to be proportional to the total gate width of the device, a large test device of 2.6 mm total gate width has been selected for the gate yield evaluation; the drain leakage current under pinch-off condition is used as a parameter for the gate yield.



	2	3	4	5	6	7	8
1							
2			0.36	0.30	0.33		
3		0.34	0.30	0.26	0.30	0.29	
4		0.30	98	0.23	0.28	0.31	
5	0.44	0.32	0.23	0.25	0.27	0.30	0.30
6	0.54	0.48	0.37	0.25	0.24	0.27	0.31
7	0.54	0.36	0.57	0.24	0.23	0.26	0.27
8		0.36	0.34	0.30	0.21	0.29	
9	0.37	0.37	0.47	21	0.26	0.44	0.29
10	0.66	0.41	0.28	0.28	0.23	0.25	0.41
11	OutL	0.49	0.27	0.23	0.24	0.32	0.37
12		0.39	0.30	0.24	0.27	0.32	
13		0.37	0.41	0.27	0.28	0.33	
14			0.42	0.0	0.34		

	2	3	4	5	6	7	8
1							
2			140	2.6	124		
3		272	116	109	2.3	136	
4		2.7	2.2	2.6	2.5	2.4	
5	3.1	102	2.4	2.1	90	2.2	126
6	2.8	2.9	2.6	2.0	2.1	2.1	2.6
7	167	3.0	101	2.3	2.3	98	129
8		2.7	2.6	2.4	2.3	83	
9	2.9	3.0	2.2	2.5	2.2	118	2.2
10	2.9	2.6	2.8	2.2	127	2.3	2.4
11	OutL	2.8	2.3	2.5	93	128	2.3
12		2.5	2.3	103	2.2	129	
13		2.3	2.8	2.8	2.7	2.1	
14			2.4	0.00	2.5		

Figure 3.38: Comparison of the sub-threshold leakage current [μA/mm] between the dielectric assisted gate technology (l) and the 3-layer resist gate technology (r). Leakage currents are obtained at V_{DS} = 2.5 V and V_{GS} = -2 V from a 2.6 mm test device on pseudomorphic HEMT wafers with a gate length of 200 nm. Both technologies show homogeneous leakage currents, however many devices of the 3-layer resist technology show excessive leakage and fail. The lower values for the dielectric assisted technology are linked to the gate nitride stripping process supporting surface depletion.

As depicted in figure 3.38, the mappings of the drain leakage current of a 2.6 mm pHEMT test device with a gate length of 200 nm shows significant differences between the dielectric assisted and the 3-layer resist gate technology. At 2.5 V drain voltage and -2 V at the gate, both wafers show a homogeneous distribution of the leakage current. The lower values for the dielectric assisted gate technology are linked to a stronger surface depletion due to the nitride stripping process and should not be considered as a quality parameter of the gate itself. The crucial difference is found in the number of abnormal devices - while the dielectric assisted technology shows only four not properly working devices with exceeding leakage, there are 22 or 20 % more faulty devices for the 3-layer resist gate. Local pinch-off problems have been identified by electro luminescence characterization under device breakdown conditions. Affected devices show bright emission spots indicating local current pathes related to a non-uniform definition of the gate foot. Due to the separate control of the gate length and gate head size, the dielectric assisted gate technology offers high flexibility combined with superior gate yield. If not suitable by the epitaxy material, the dielectric assisted gate technology is recommended for a high yield gate definition.

3.5 Gate recess

As discussed before on page 29, the recess configuration has significant impact on the device performance. In this section, the focus is set on the technological realization of the recess structure for the metamorphic and pseudomorphic HEMT technologies. Recess etching can be performed by dry plasma processes or wet chemical etching. In contrast to dry etching techniques, wet etching offers a high simplicity for low-cost, and introduces minimal damage to the etched surface. Since the size of the gate recess is linked to the device performance like the off-state breakdown [130], lateral etching of the cap layer has to be well controlled. In this work, wet chemical etching has been used for the gate recess on both, pseudomorphic and metamorphic HEMT technologies.

Generally, wet chemical etching of III-V-compounds relies heavily on oxidation and reduction reactions. To obtain a high vertical control and homogeneity of the recess, slow, diffusion limited etching is preferred. Diffusion limitation can be realized by formation of thick oxide layers (oxide buildup) and slow dissolution of the oxidized product into the etch solvent. Oxidation strongly depends on the bond strength of the semiconductor surface, and anodic oxidation has to be used for high band-gap materials like SiC [131] and GaN [132]. Oxidation of GaAs and $In_xGa_{1-x}As$, however, is realized by oxidizers like peroxide or nitric acid. All types of arsenic oxides are easily dissolved in water and will not contribute to diffusion limitation; dissolution of group III-oxides, however, requires the presence of acids or bases partly supported by complex forming agents like ammonium-hydroxide, sulfuric or citric acid. Diffusion limited etch rates are realized by a slow removal of the group III-oxides.

3.5.1 Recess on metamorphic wafers

The gate recess process on metamorphic epitaxial structures on GaAs substrates is similar to that of InP-based HEMTs. Succinic acid hydrogen peroxide solutions are preferably used due to a higher selectivity towards the $In_xAl_{1-x}As$ barrier compared to citric acid [133]. With acid dissociation constants as defined in equation 3.2 of $pK_{S1} = 4.21$ and $pK_{S2} = 5.64$ [134], the etch solution is buffered to a pH value between 4.5 an 5.5 by ammonia titration; c(H_3O^+), c(HA) and c(A^-) are the concentrations of the hydronium ion (H_3O^+) dissociated from the generic acid (HA) and the conjugate base (A^-) in aqueous solution. There is to note that peroxisuccinic acid, oxosuccinic acid, or malonic acid may be formed by parasitic oxidation with hydrogen peroxide [135].

$$pK_s = -\log K_s = -\log \frac{c(\mathrm{H_3O^+}) \cdot c(\mathrm{A^-})}{c(\mathrm{HA})} \tag{3.2}$$

The $In_xGa_{1-x}As$ layer of the mHEMT cap is oxidized by the aqueous hydrogen peroxide solution and its $OH^{\cdot}$ radicals. All arsenic oxides are dissolved in water. Since, group-III oxides cannot be dissolved in water directly, complexes are formed with $C_4H_5O_4^-$ ions of the once dissociated succinic acid molecule that are water soluble, again. As shown later by variation of the etch solution, the etch mechanism is reaction limited by the oxidation process. Lateral etching of the gate recess is proportional to the recess time and allows a simple optimization for the metamorphic low-noise and power technology. Furthermore, the etch rate shows only minor dependence on the structure size. To provide homogeneous etch results, a good adhesion of the PMMA foot resist and a hydrophilic semiconductor surface have to be guaranteed at the bottom of the gate foot resist opening. Especially adhesion promoters may not be removed properly by resist development and can cause an irregular gate recess. Irregular recess etching is shown in the left part of figure 3.39. This picture is taken from an experimental wafer without any surface preparation before the gate recess; ebeam exposure can be excluded as a cause, since lithography for this wafer has been simplified to a single resist exposure based on reliable pHEMT production parameters.

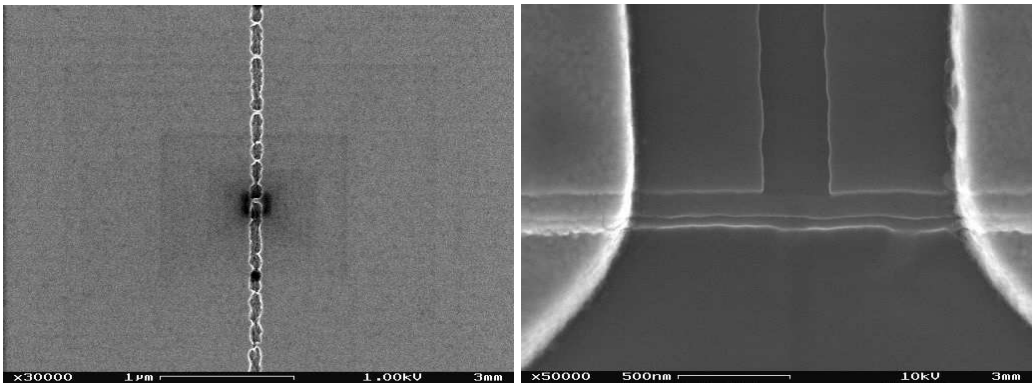


Figure 3.39: Irregular recess (l) due to a hydrophobic semiconductor surface and poor wetting behavior of the etch solution. Top view on the mesa edge (r) of the properly defined gate recess.

The importance of the etch selectivity between the $In_xGa_{1-x}As$ cap and $In_xAl_{1-x}As$ barrier is obvious at the edge of the mesa as shown in the right part of figure 3.39, where the gate passes from the active to the isolated part of the device. For gate to channel isolation as described before in section 3.2.2, a mouse hole is formed by selective sidewall etching of the channel creating a free standing $Al_xGa_{1-x}As$ fin of 10 to 20 nm thickness.

3.5.1.1 Double recess on metamorphic wafers

Before the gate lithography step, a single resist ebeam lithography and selective wet chemical etching are used to define the wide recess for the double recess metamorphic power HEMT. The etch solution is based on succinic acid and hydrogen peroxide. Like for the gate recess, good adhesion of the resist mask and a clean and hydrophilic semiconductor surface at the bottom of the resist opening are required for a proper etch result. The definition of the wide recess is sketched in the left part of figure 3.40.

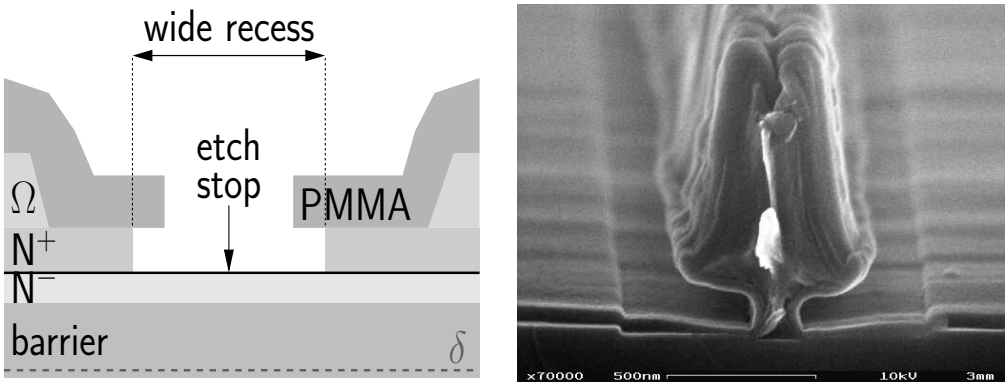


Figure 3.40: Sketch of the wide recess formation by single resist ebeam lithography (l) and selective wet chemical etching of the N^+ cap. Cross-sectional view of a double recessed metamorphic device (r).

Since both, the highly doped $In_xGa_{1-x}As$ cap and the slightly doped charge screen layer consist of the same material composition, they are separated by a thin $In_xAl_{1-x}As$ layer. This thin layer provides an etch stop due to its high resistance against the recess etch

solution. After wide recess formation, device fabrication continues with the gate module like for the single recess technology but deviates for the gate recess. In advance of the gate recess, the thin etch stop on top of the charge screen layer has to be removed by a dip in a non-selective etch solution, containing sulfuric acid and hydrogen peroxide. With respect to the non-selective removal of the etch stop layer, the minimum charge screening layer thickness is limited to around 10 nm. A cross sectional view of a double recess metamorphic device is shown in the right part of figure 3.40 with a symmetric wide recess configuration of 1 μm size and a gate length of 150 nm.

3.5.1.2 Maturity of the mHEMT wet chemical recess solution

Gate recess formation is one of the key elements during active device fabrication and has to be well controlled. To prove the production capability of the metamorphic recess etch solution based on succinic acid and hydrogen peroxide, variations have been performed on metamorphic low-noise material regarding reproducibility, temperature and composition. Thanks to the high process stability of the dielectric assisted gate technology very reproducible gate nitride openings of 100$\pm$6 nm have been realized on the low-noise mHEMT material. Since recess properties were proven to be independent from the on-wafer position and the presence of the gate head resist profile in preceding experiments, recess variations have been carried out without the gate head resist profile on parts of the wafer with a size of around 1x1 cm^2. Samples were etched in the slightly stirred etch solution. The etch process is interrupted by water rinsing. Nominal parameters for the low-noise mHEMT gate recess are 60$\pm$1 seconds at a temperature of 21$\pm$0.2 °C and a pH-value of 5.3$\pm$0.1. The dielectric assisted gate technology offers to control the recess geometries by electron microscopy directly after recess etching; for a high acceleration voltage above 10 kV the undercut is visible through the 100 nm thick nitride layer as shown in figure 3.41. For higher accuracy the Si_3N_x (gate nitride) has been removed by CF_4 reactive ion etching.

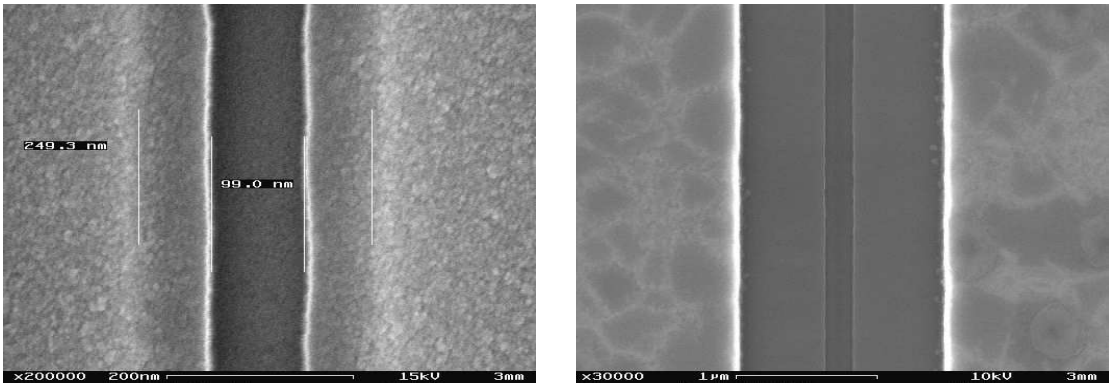


Figure 3.41: SEM-inspection of the recess size through the gate nitride layer (l) and after nitride removal (r).

Variations of the etch time are shown in the left part of figure 3.42. There is a linear relationship between the recess size and the etch time up to 135 s, typical for a reaction limited etch process. Linear regression, however, does not meet the origin of the coordinate system because of a delayed etch start through the initial oxide. Due to reaction

limitation, a high selectivity towards the barrier layer is required; even for the longest process time, no defect was found related to insufficient etch stop properties. With a lateral etch rate of 1 nm/s, the recess undercut can be easily controlled by time. For the low-noise metamorphic mHEMT, the target undercut of 45±5 nm can be realized with a comfortable fabrication window of 60±5 seconds. For the power metamorphic HEMT, the gate recess etch time is increased by 30 s, equivalent to an undercut of 75 nm.

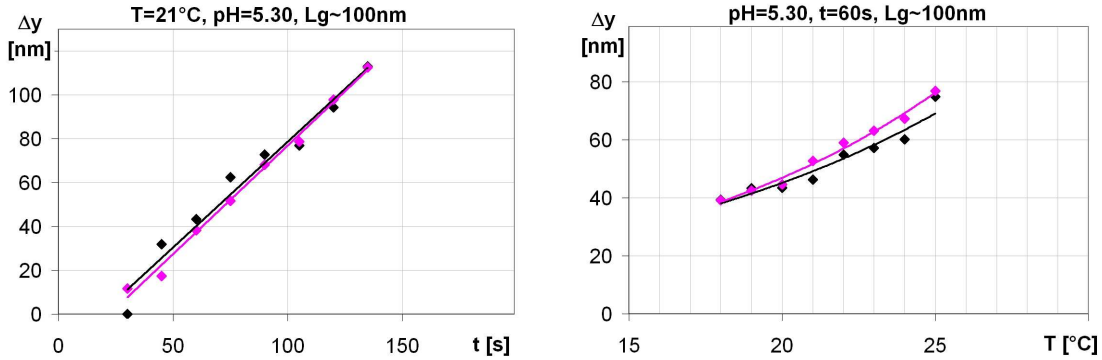


Figure 3.42: Dependence of the metamorphic recess dimension from the etch time (l) and temperature (r). The less accurate dark points are obtained from SEM-inspections at 15 kV through the 100 nm thick gate nitride. The light points are taken from the gate recess after nitride removal.

The right part of figure 3.42 shows the dependence of the metamorphic recess dimension for a bath temperature between 18 to 25±0.2 °C; the etch time of 60 s and the pH-value of 5.3 are kept constant. The temperature dependence of the undercut follows the exponential relationship of the Arrhenius law. An activation energy of 16.7 kcal/mole or 0.73 eV can be calculated for the InGaAs etch process that is slightly higher than for GaAs etched by citric acid [136, 137]. A temperature variation within ±1 °C changes the recess size by ±5 nm. This is acceptable since the temperature can be well controlled even within a smaller process window.
To evaluate the impact of the etch solution composition, the ratio of ingredients such as succinic acid and hydrogen peroxide have been investigated. The variation of the succinic acid content by ±20 % shows no impact on the recess size in figure 3.43. This fits with the reaction limitation caused by the oxidation process. Variation of the hydrogen peroxide content by ±20 % in the right part of figure 3.43, however, shows a clear linear dependence between the undercut and the amount of hydrogen peroxide. To control the etch rate of the mHEMT gate recess, the hydrogen peroxide concentration has to be well adjusted in the recess solution. Since hydrogen peroxide decomposes over time, especially when mixed to non-pure aqueous solutions, there are two requirements for the mHEMT gate recess.

- Fresh (non-expired) hydrogen peroxide has to be used to prepare the gate recess etch solution.
- Gate recessing has to be performed in time after preparation of the gate recess solution.

For a variation of ±5 nm concerning the recess undercut the amount of hydrogen peroxide may fluctuate by more than 10 %; this is no issue for the recess solution preparation. The decomposition of hydrogen peroxide has been evaluated for the highest concentration. After 64 hours the etch rate reduced to a value equivalent to 80 % of peroxide concentration. Assuming a linear decomposition over time, the gate recess should be performed within 10 hours after preparation of the gate recess solution.

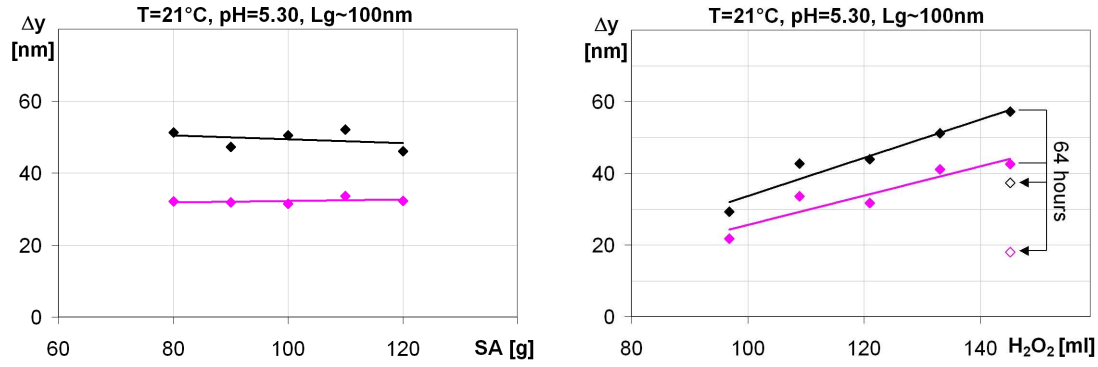


Figure 3.43: Dependence of the metamorphic recess size from the amount of succinic acid SA (l) and hydrogen peroxide (r). The less accurate dark points are obtained from SEM-inspections at 15 kV through the 100 nm thick gate nitride. The light points are taken from the gate recess after nitride removal.

A variation of the pH-value has been carried out in a wide range between 4.6 and 6.0. The maximum lateral etch rate in the left part of figure 3.44 is observed slightly below the nominal value of pH = 5.3. The recess undercut over the pH-value implies that dissolution of the group-III oxides is linked to complexes formed by the once dissociated succinic acid molecule; the maximum concentration of $C_4H_5O_4^-$-ions is reached between the two dissociation numbers of succinic acid of $pK_{S1} = 4.21$ and $pK_{S2} = 5.64$ [134]. Accepting a 10 % tolerance for the etch rate, there is a very large fabrication window for the pH-value from pH = 4.8 to 5.6. Adjustment of the pH-value is no issue for the metamorphic gate recess.

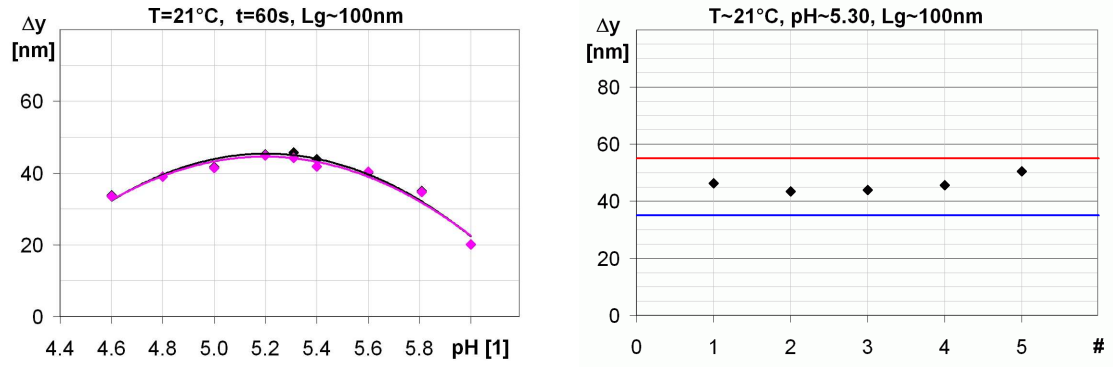


Figure 3.44: Dependence of the metamorphic recess size from the pH-value (l) and reproducibility of the etch rate for several etch solutions (r). The less accurate dark points are obtained from SEM-inspections at 15 kV through the 100 nm thick gate nitride. The light points are taken from the gate recess after nitride removal.

Besides the impact of fluctuations caused by a single parameter as discussed above, the preparation of the nominal recess solution has to be reproducible for device fabrication on a production level. Here, fluctuations of compositions, the temperature and pH-value may occur simultaneously. The reproducibility has been proven over five independent preparations of the recess etch solution. For nominal etching parameters, fluctuations of the recess undercut are in a small range of 7 nm, acceptable for device fabrication.
The mHEMT recess solution based on succinic acid and hydrogen peroxide provides reaction rate limited etching of the highly doped $In_xGa_{1-x}As$ layers with high selectivity towards the $In_xAl_{1-x}As$ barrier. Processing windows are comfortable for device fabrication. A good reproducibility of the etch solution preparation confirms its high maturity for metamorphic HEMT fabrication.

3.5.2 Recess on pseudomorphic wafers

The highly doped cap layer of the pseudomorphic HEMT structure is based on GaAs and cannot be etched by aqueous acid or alkaline solutions [138] that do not contain an oxidizing agent. Therefore, wet etching of GaAs requires two steps - oxidation and dissolution of oxidized components. While all arsenic oxides can be dissolved in water [139], oxides and hydroxides of gallium have amphoteric character and can be dissolved in alkaline or acid media [139].
The etch properties of the hydrogen peroxide based etch solution change with the pH-value. For a strong acid or alkaline hydrogen peroxide solution there is equivalent etching of GaAs and $Al_xGa_{1-x}As$ [109]. Figure 3.45 shows the etch profiles obtained from a one minute peroxide based recess etching step on N^+-GaAs at a pH-value of 4 and 8. At the moderately low pH-value, the little depth of the etch profile indicates to a diffusion limited removal of the gallium oxides. With the higher pH-value, a significantly deeper isotropic profile, typical for reaction limitation, is observed.

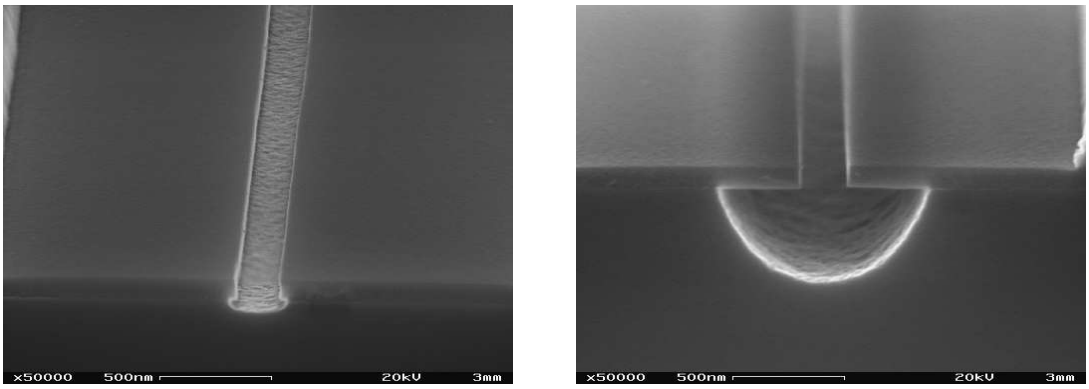


Figure 3.45: Etch profile depending on the pH-value; acid pH = 4 (l) and alkaline pH = 8 (r).

For $6 < pH < 7.1$ [140] the hydrogen peroxide etch solution provides a smooth etch surface and sufficient selectivity towards the $Al_xGa_{1-x}As$ barrier. In this small window, the etch rate increases for higher pH-values independent from pH-adjustment by ammonia or trimethylammonium hydroxide. This indicates that dissolution of Ga-oxides is linked to the OH^- concentration in the recess solution. A cross section of the gate recess performed

with a hydrogen peroxide solution at pH $\approx$ 6.8 is shown in figure 3.46; the etch solution stopped on the $Al_{25}Ga_{75}As$ barrier and shows a smooth surface.

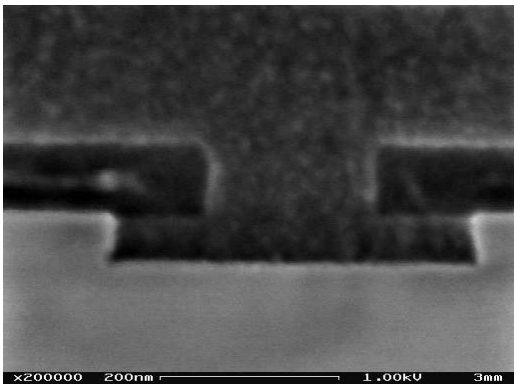


Figure 3.46: The highly doped GaAs cap is etched by a hydrogen peroxide solution at pH $\approx$ 6.8 without any selectivity to the AlAs etch stop layer; the planar profile of the recess bottom is a results from strong reduction of the vertical etch rate on the $Al_{25}Ga_{75}As$ barrier.

It is difficult to realize Schottky contacts of good quality on the oxidized $Al_xGa_{1-x}As$ barrier layer. Therefore, a thin GaAs Schottky layer and an atomic scale AlAs etch stop are used on top of the $Al_xGa_{1-x}As$ barrier to suppress the formation of Al-oxides. The selectivity of the hydrogen peroxide etch solution, however, is too low and does not stop on the thin AlAs layer. Adding some citric acid helps to reach the required selectivity. At neutral pH-value, most of the citric acid dissolved in water is completely dissociated to $C_6H_5O_7^{3-}$ and forms a negatively charged surface complex with the oxidized AlAs stop layer [141, 142]. Further removal of group-III oxides is suppressed by repelling forces between the OH^- and the negatively charged citric acid complex.
In this work, the gate recess of the pseudomorphic HEMT has been carried out with an optimized citric acid, hydrogen peroxide based etch solution. Strict control of the pH-value adjusted by ammonia titration slightly below 7 is required to control the etch rate and selectivity toward the AlAs etch stop. The etch mechanism is diffusion limited concerning Ga-oxide removal and provides a slow but regular attack of the GaAs layer. Diffusion limitation however causes a high sensitivity of the etch rate to the structure size.

3.6 Gate metallization, lift off and device passivation

The gate metalization is performed directly after recessing to avoid surface oxidation. Metalization stacks of TiPtAu [143, 13] or TiAl [122] are commonly used, where titanium provides a good adhesion on the semiconductor surface. Both metalization types offer advantages. While TiPtAu-gates benefit from the low specific resistance of gold, simplifying a small gate length for multi layer resist ebeam lithography, platinum is required as diffusion barrier to prevent gate sinking during long term device operation not observed on aluminium based gates. However, TiAl based Schottky contacts tend to show barrier height lowering at high temperature storage, as mentioned before on page 54. Due to compatibility reasons with existing production steps and the more critical metal adhesion for a small gate length, TiAl was selected in this work for the gate metalization.

Depending on the gate technology, the recess area next to the gate foot has to be protected by a passivation layer directly after gate metal lift off or gate nitride removal, respectively. Silicon nitride passivation is well established in the GaAs semiconductor industry and works well on pseudomorphic and metamorphic epitaxy material. However, the thermal budget has to be kept low for the metamorphic devices since the high indium content requests low ohmic contact anneal temperatures. Further heat treatment may degrade the ohmic contact quality.

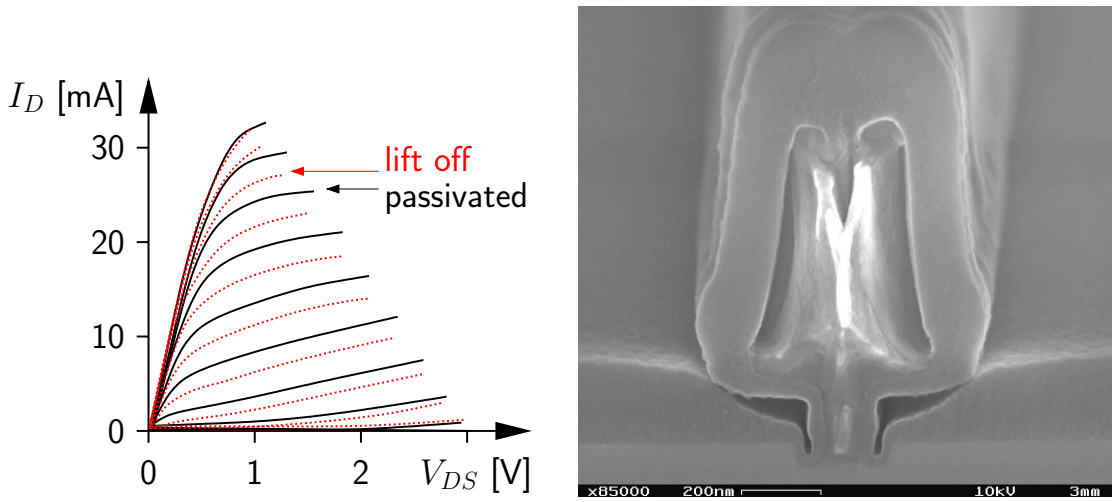


Figure 3.47: Output characteristic before and after device passivation for the metamorphic low-noise technology (l). Cross-sectional view of the passivated gate area (r).

With respect to the ohmic contacts, the deposition temperature has been reduced to 275 °C. No increase of the access resistance is observed in figure 3.47 comparing the output characteristic of a metamorphic low-noise device before and after silicon nitride passivation. Saturation currents slightly reduce but do not change e.g. due to three-terminal breakdown characterizations. This hints to a stabilized semiconductor-SiN_x interface at the gate recess. A cross sectional view of a 200 nm silicon nitride passivated 3-layer resist gate on metamorphic low-noise epitaxy layers is shown in the right part of figure 3.47; next to the gate foot, a passivation layer thickness of 10 nm is sufficient for surface stabilization. The mouse holes underneath the gate head are closed for a sufficiently thick overall passivation layer and help to reduce parasitic capacitances - in contrast, mouse holes which are not formed properly have some connection to the wafer surface and are filled up by photo resist during succeeding lithography steps. Affected device show large spreads and increased values on the feedback capacitance.

4 Low-noise properties

The technology development regarding low-noise devices mainly focused on the metamorphic single recess HEMT due to advantages coming from the high indium content of the channel. Based on DC, small signal and noise parameter characterizations, a precise noise model has been extracted for transistor base cells used in several low noise amplifier demonstrators. Although not developed for low-noise, some LNA-demonstrators have also been fabricated with the pseudomorphic single recess power technology.

4.1 Metamorphic low-noise HEMT

The fabrication of the metamorphic devices is based on the epitaxial sequence given in chapter 2.5.4. As described in previous chapter, the ohmic contacts are realized by AuGeNi and 60 s rapid thermal annealing at 320 °C. The 3-layer resist gate technology is used for T-gate definition of 120 nm gate length followed by wet chemical recess etching based on succinic acid and hydrogen peroxide. The recess size is controlled by the etch time and is targeted for 45 nm lateral extension to comply with a device breakdown above 4 V. The evaporated gate metalization consists of TiAl and is structured by the lift off technique. For device protection, a 200 nm thick SiN_x-passivation is deposited at 250 °C with respect to the low ohmic anneal temperature. Furthermore, passive devices like thin film resistors, capacitors, inductors and lines have been realized for the demonstrator circuits.

In this section, DC, small signal and RF-noise properties of the metamorphic low-noise HEMT technology are presented. Noise characterizations of two device geometries allowed to set up a noise equivalent circuit required for the low noise amplifier design.

4.1.1 DC-performance

The output and transfer characteristic of a 100 μm single finger test device are presented in figure 4.1. The slight kink in the output characteristic around 0.4 V drain voltage is related to negatively charged surface states located at the gate recess; with increasing drain voltage, these surface states are compensated by holes generated by impact ionization. The low damage 3-layer resist gate technology and proper device passivation helps to reduce this kink-effect. However, the kink does not disappear completely. The high channel indium content of the metamorphic low-noise device is reflected in a high extrinsic transconductance with a peak value around 1000 mS/mm at 1.5 V drain voltage. A maximum saturation current of $I_{DS^+} = 800$ mA/mm is reached for a gate voltage of $V_{GS} = 0.5$ V. The pinch-off voltage $V_{G100} = -0.45$ V is obtained for a drain current of 1 % of I_{DSS}.

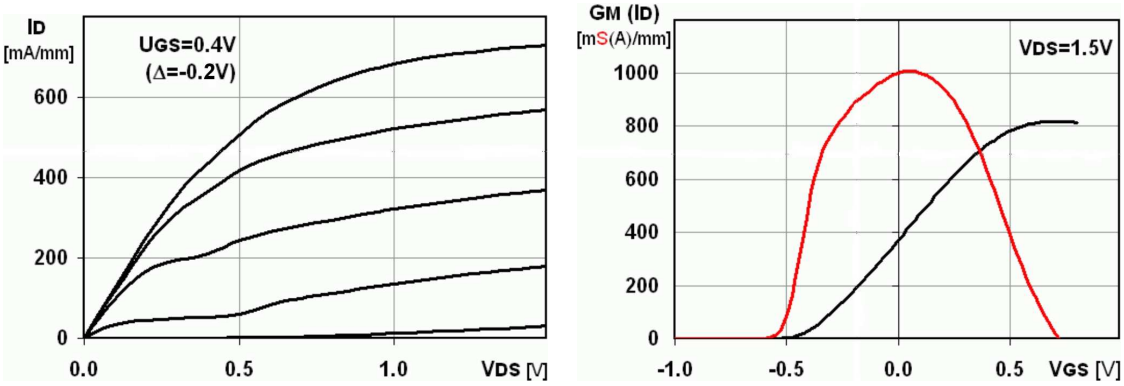


Figure 4.1: Output characteristic (l) and transfer characteristic (r) of the metamorphic 1x100 μm low-noise test device.

The diode characteristic is shown in figure 4.2 in linear and semi logarithmic scale. The two terminal breakdown voltage defined for a reverse current density of 1 mA/mm is close to -5 V and is symmetrical for the gate-source and gate-drain diode. A barrier height of 0.51 V has been extracted from the forward diode characteristic which fits well to the $In_{53}Al_{47}As$ barrier and the mean indium content of 60% for the channel.

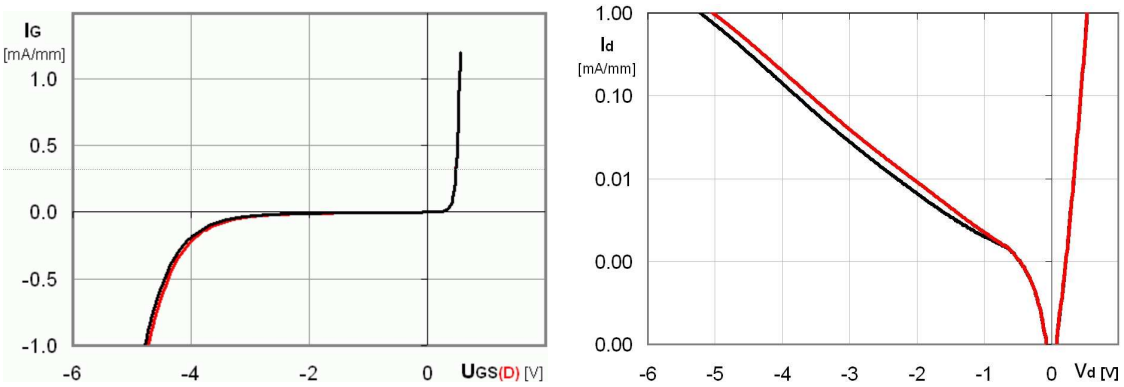


Figure 4.2: Diode characteristic in linear (l) and logarithmic scale (r) for the metamorphic 1x100 μm low-noise test device.

For industrial process control, automatic measurements are used to characterize the on-wafer homogeneity of electrical key parameters. Therefore, test devices are distributed over the whole wafer. Mappings of the maximum saturation current I_{DS^+}, the peak transconductance G_{max}, the pinch-off voltage V_{G100} and device breakdown V_{bDS} are found in the annex on page 144. Representatively, the mapping of the maximum transconductance G_{max} is shown in figure 4.3 for the 100 μm single finger test device. The peak transconductance G_{max} of 1120 mS/mm at 1 V drain voltage is homogeneously distributed over the whole wafer. The higher values observed at the end of the front side fabrication compared to in-line measurements are related to the more accurate 4-pole probing technique of the automatic measurement setup and contact resistance correction. Two test devices failed due to high leakage currents. This failure is linked to the yield of the 3-layer resist gate technology.

Flat at bottom		Param.	Gmax__FET		Lot	K17014/ASTROLAN_02A			
		Unit	mS/mm		Wafer	2/R004			
Average	1122		2	3	4	5	6	7	8
σ	14	1							
% s	1.2%	2							
Range	55	3	1117		1107	1129	>>>		1156
% Range	4.9%	4		1127		1118		1121	
Min	1102	5	1118		1114		1131		1135
Max	1156	6		1124		1121		1140	
Median	1121	7	1104		1123	1102	>>>		1108

Figure 4.3: Mapping of the max. transconductance G_{max} for the 1x100 μm low-noise test device.

The mean maximum saturation current I_{DS+} is 702 mA/mm with a small spread of $\sigma = 2\,\%$. At 1 % of I_{DSS}, the pinch off voltage V_{G100} of -0.43 V with a small standard deviation of 2 % confirms good gate recess etch stop properties for the $In_{53}Al_{47}As$ barrier. The three terminal breakdown voltage V_{bDS} is obtained from a gate voltage sweep for a fixed drain current of 1% of I_{DSS}. The mean device breakdown V_{bDS} of 4.9 V fulfills the requirement of 4 V with a spread of $\sigma \leq 4\,\%$; this confirms the correct gate recess size.

4.1.2 Small signal RF-performance and model

As for the DC-characterization, small signal measurements have been performed on a 2x75 μm test module for a drain voltage of 1 V and a gate voltage of 0 V which is close to the bias point of maximum gain. RF-key elements like the input or feedback capacitance are extracted from a simple small signal equivalent circuit [93] described in the annex on page 161. Mappings of the input and feedback capacitance, the output resistance and RF-transconductance are found on annex page 145. Representatively, the mapping of the input capacitance c_{in} is shown in figure 4.4 to demonstrate the on-wafer homogeneity.

Flat at bottom		Param.	cin						
		Unit	fF						
Average	184.8		2	3	4	5	6	7	8
σ	250.1	1							
% s	135.4%	2							
Range	1127.8	3	123		155	128	129		1247
% Range	610.4%	4		129		129		126	
Min	119.3	5	127		126		126		126
Max	1247.1	6		132		131		128	
Median	128.2	7	129		130	130	119		124

Figure 4.4: Mapping of the input capacitance c_{in}(2x75 μm at $V_{DS} = 1$ V and $V_{GS} = 0$ V).

One of twenty PCM-modules failed in the automatic RF-test due to high leakage currents and was not considered for spread calculation. The input capacitance c_{in} of 128 fF represents a gate length of 120 nm and shows an acceptable spread of $\sigma \leq 6\,\%$. Similarly, for the feedback capacitance c_f of 29.8 fF which is linked to the gate head size and passivation thickness. The output resistance r_{out} of 97.5 Ω is correlated with the input capacitance c_{in} as a function of the gate length; the correlation coefficient is 94 %. The smallest spread of $\sigma \leq 3\,\%$ is observed for the RF-transconductance g_{me} of 166.2 mS which represents the distance between the Schottky contact and the channel.

A deeper analysis of the small signal performance of the low-noise metamorphic HEMTs has been performed up to 65 GHz on Agilent systems. Extracted parameters like the

transit frequency f_T and the maximum oscillation frequency f_{max} are shown in figure 4.6 for a 2x50 μm device biased at V_{DS} = 1.25 V. The highest transit frequency f_T is found at V_{GS} = 0 V. While f_{Tcgs} = 240 GHz is calculated from the RF-transconductance and input capacitance, the more conservative parameter f_{Tc} = 193 GHz includes also the feedback capacitance c_{gd}. The extrapolation from $|h_{21}|^2$ at 40 GHz results in an extrinsic transit frequency of f_{Tex} = 202 GHz. The maximum oscillation frequency f_{max} extrapolated from the unilateral gain is close to 300 GHz.

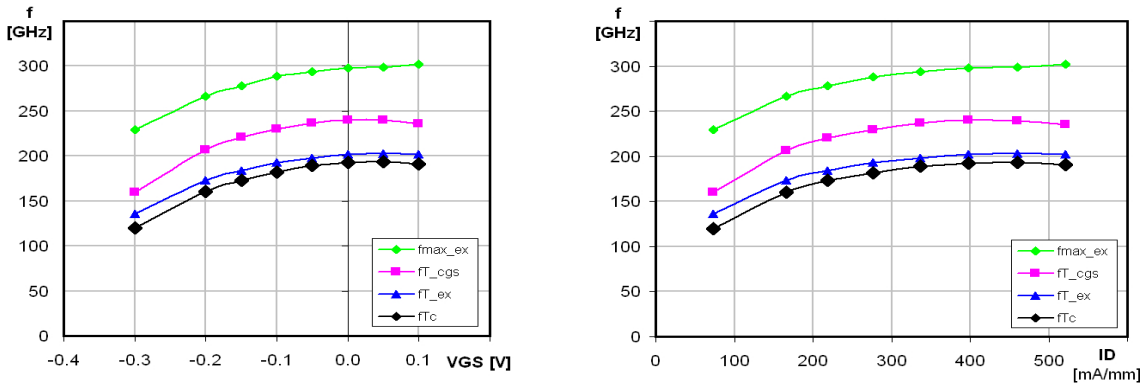


Figure 4.5: Transit and maximum oscillation frequency f_T and f_{max} as a function of V_{GS} (l) and the drain current I_D (r); Extrapolations at 40 GHz from a 2x50 μm device operated at V_{DS} = 1.25 V.

The evolution of the small signal transconductance g_{me}, the input c_{in} and feedback capacitance c_f versus the current density is shown in the left part of figure 4.6.

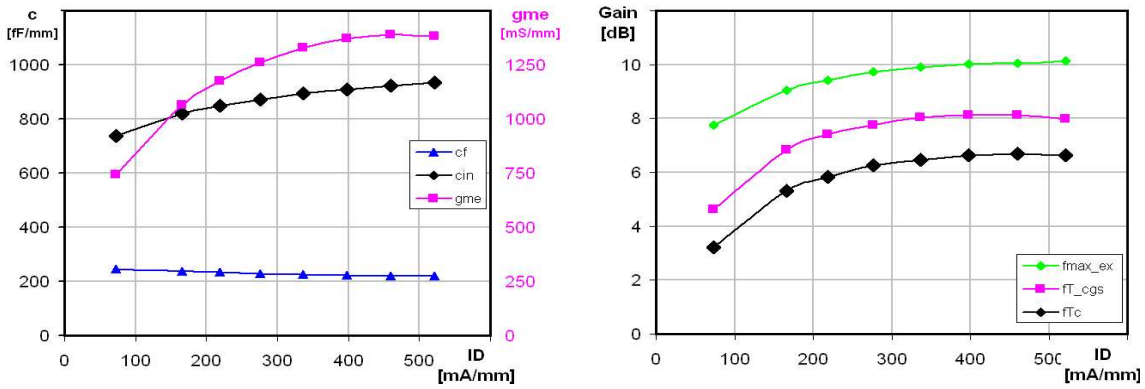


Figure 4.6: Input c_{in} and feedback c_f capacitance and RF-transconductance g_{me} (l) at 4 GHz. The estimated gain (r) at 94 GHz is based on extrapolations from f_T and f_{max}.

Based on the extracted transit frequency f_T and the maximum oscillation frequency f_{max}, the maximum available gain and current gain are calculated for 94 GHz. From these data, a small signal gain between 6 and 8 dB per transistor stage can be expected for a LNA-design. To improve the accuracy of the small signal equivalent circuit elements for W-band, S-parameter measurements have been performed up to 110 GHz on an Anritsu setup. In figure 4.7 the previous results are confirmed including some spread analysis

with the minimum and maximum values from 15 samples distributed over the wafer. The current gain $|h21|^2$ at 94 GHz ranges from 7.9 to 8.7 dB. A range of 3.1 dB is observed for the maximum available gain MAG due to a peak of 8.0 dB and a minimum value of 4.9 dB. Below and above 94 GHz, the range is less than 2 dB.

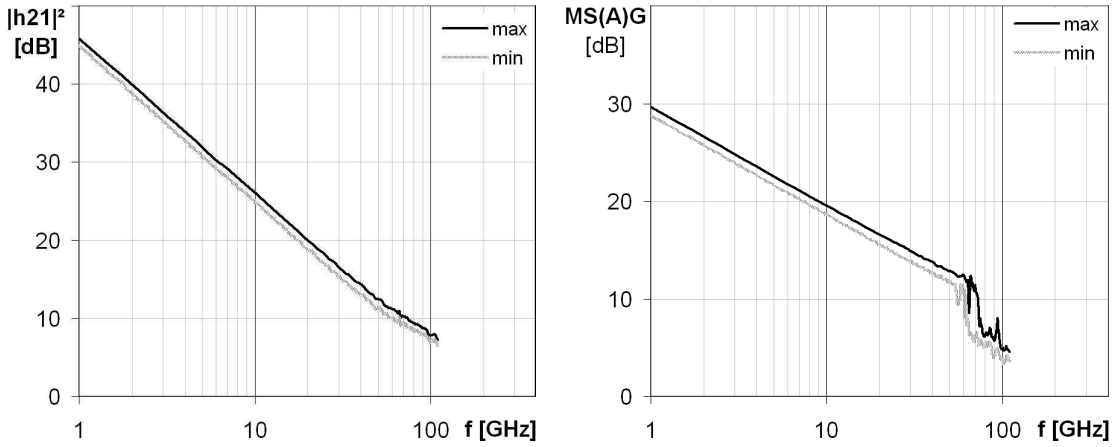


Figure 4.7: Minimum and maximum short circuit current gain $|h_{21}|^2$ (l) and maximum available (stable) gain M(S)AG (r) obtained from small signal parameter measurements at $V_{DS} = 1$ V and $V_{GS} = 0$ V of fifteen 2x50 μm devices normalized to a 50 Ω reference plane.

The unilateral gain MUG in figure 4.8 also shows little spread from 8.4 dB to 9.4 dB at 94 GHz. The minimum and maximum stability factor k are 1.02 and 1.34, respectively.

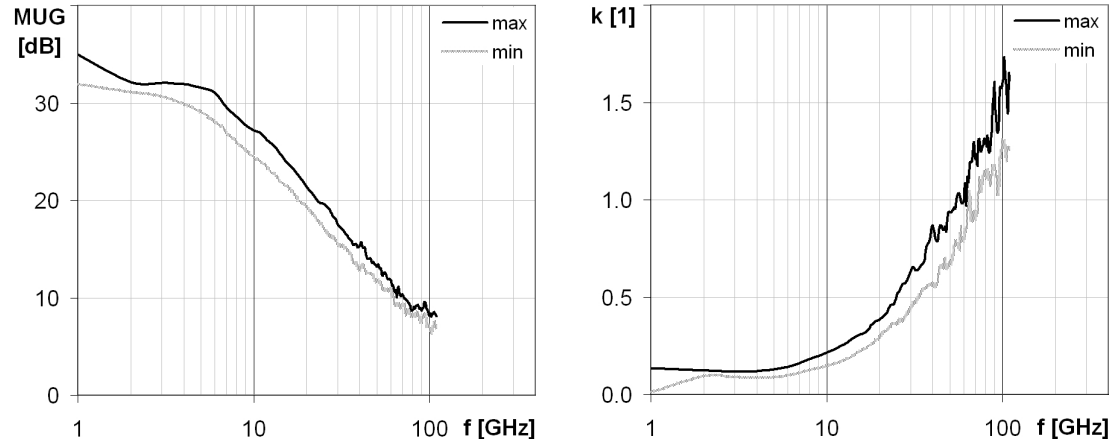


Figure 4.8: Minimum and maximum of unilateral power gain MUG (l) and stability factor k (r) obtained from small signal parameter measurements at $V_{DS} = 1$ V and $V_{GS} = 0$ V of fifteen 2x50 μm devices normalized to a 50 Ω reference plane.

For similar drain and gate biasing, the elements of the small signal equivalent circuit are expressed by empiric functions of the gate width W_G and number of fingers N as summarized in table 4.1. The metamorphic low-noise HEMT technology based on 60 % of mean channel indium content and a gate length of 120 nm provides typical transit frequencies around 200 GHz and a maximum oscillation frequency around 300 GHz. Parameter spreads over the wafer are low. With respect to the 450 nm thick SiN_x passivation, the

observed cut-off frequencies are in agreement with publications of institutes working on comparable material systems regarding indium composition and gate length [19, 20, 21].

Element	Fit-function	2x50 μm device
L_G [pH]	$\frac{0.311}{N^{0.797}} \cdot W_G - 3.56 \cdot N + 17.57$	19.4
L_S [pH]	$\frac{42.147}{N^{1.411}} - \frac{80.1 \cdot ln(W_G)}{N^{4.58}}$	2.8
L_D [pH]	$\frac{0.706 \cdot W_G}{N^{0.524}}$	24.5
c_{gm_0} [fF]	6.2	6.2
c_{gs} [fF]	$1.15 \cdot N \cdot W_G$	115
c_{gd} [fF]	$0.232 \cdot N \cdot W_G - 0.22 \cdot W_G + 0.676 \cdot N + 6.943$	20.5
c_{ds} [fF]	$0.2 \cdot W_G \cdot N + 2.9 \cdot N$	25.8
R_S [Ω]	$\frac{250}{N \cdot W_G}$	2.5
R_D [Ω]	$\frac{250}{N \cdot W_G}$	2.5
R_G [Ω]	$\frac{0.0932}{N} \cdot W_G$	2.3
r_{ds} [Ω]	$\frac{1}{1.5\ 10^{-4} \cdot N \cdot W_G} - 3.5\ 10^{-4} \cdot N + 1.2\ 10^{-4}$	64.5
r_i [Ω]	$\frac{893.24}{N \cdot W_G} - \frac{76.25}{W_G}$	7.4
g_m [mS]	$2.1 \cdot N \cdot W_G$	210
τ [pS]	$\frac{0.0026}{N} \cdot W_G + 0.588$	0.653

Table 4.1: Scaled elements of the small signal equivalent circuit at V_{DS} = 1 V and V_{GS} = 0 V for the metamorphic low-noise devices of 60 % mean channel indium content. The fit is performed over the gate-width W_G(μm) and number of gate fingers N. Calculated values are given for a 2x50 μm device.

4.1.3 RF-noise performance

The RF-noise properties of the low-noise metamorphic devices have been characterized at MilliLab (Espoo, Finland) in V- and W-band. Since the noise figure F of a linear two-port varies as a function of the source reflection coefficient, several input reflection coefficients have been set by tuners [78] in order to extract following noise parameters: Minimum noise figure N_F, the normalized noise resistance R_n and the optimum reflection coefficient Γ_{opt} in magnitude and phase. The minimum noise figures N_F for a 2x20 μm and a 4x20 μm device operated at V_{DS} = 1 V and three different current densities, corresponding to I_{DSS}, $I_{DSS}/2$ and $I_{DSS}/5$ are shown in figure 4.9 from 50 to 100 GHz. The noise figure correlates with the current density and is in good agreement between the V- and W-band measurement overlapping at 75 GHz. At 94 GHz, the minimum noise figure is below 2.5 dB for the 2x20 μm device and below 3 dB for the 4x20 μm device.

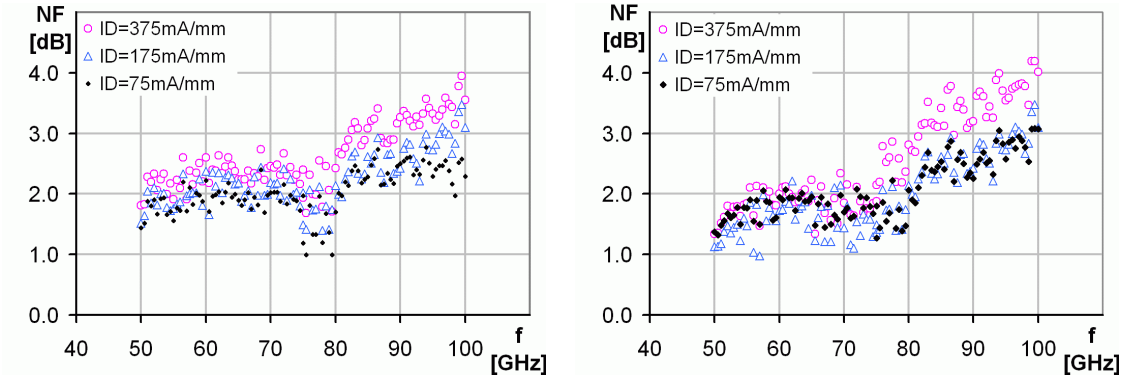


Figure 4.9: Minimum noise figure N_F within V- and W-band obtained from a 2x20 μm (l) and 4x20 μm device (r) at 1 V drain voltage and current densities of 75, 175 and 375 mA/mm.

The equivalent noise resistance R_n in figure 4.10 scales well with the device geometry with a slight different frequency response in W-band.

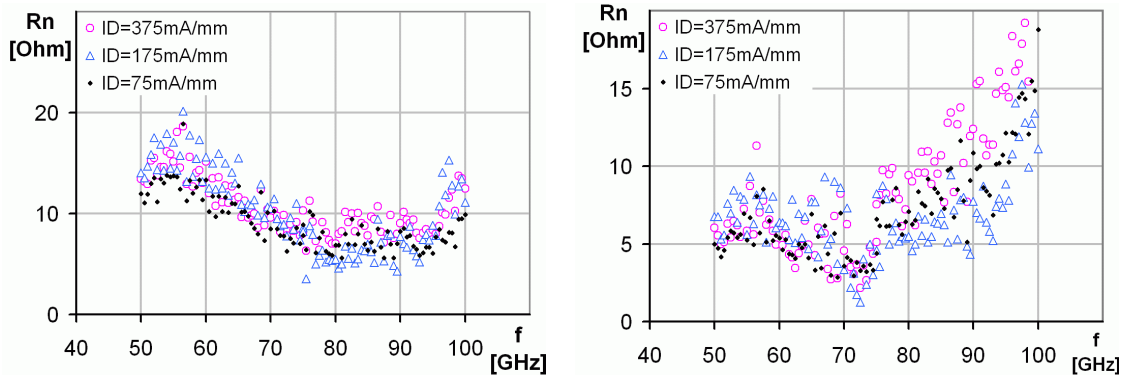


Figure 4.10: Equivalent noise figure Rn within V- and W-band obtained from a 2x20 μm (l) and 4x20 μm device (r) at 1 V drain voltage and current densities of 75, 175 and 375 mA/mm.

The magnitude of the optimum input reflection coefficient Γ_{opt} in figure 4.11 is stable over the whole frequency band for both devices.

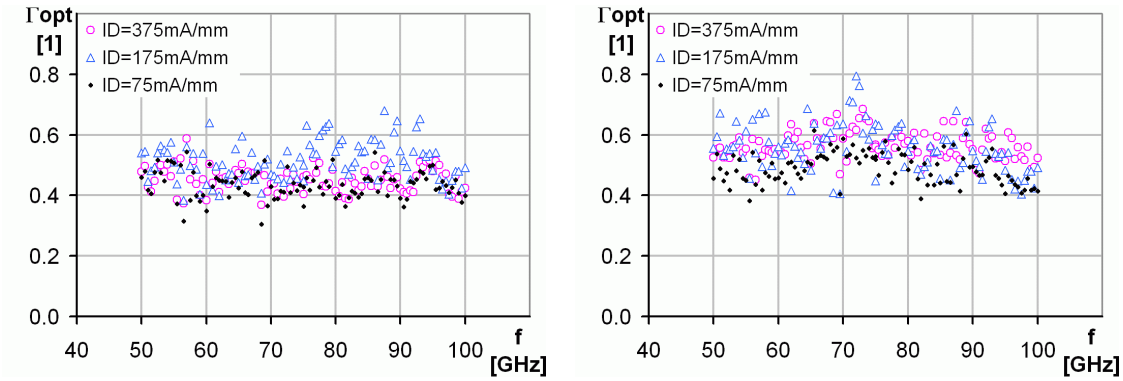


Figure 4.11: Magnitude of Γ_{opt} within V- and W-band obtained from a 2x20 μm (l) and 4x20 μm device (r) at 1 V drain voltage and current densities of 75, 175 and 375 mA/mm.

While the phase of the optimum input reflection coefficient Φ_{opt} increases steadily for all current densities of the 4x20 μm device, a phase shift is observed for the 2x20 μm device at 175 mA/mm current density. This unsteadiness at the cross-over frequency from V-band to W-band measurement is explained by calibration introducing a systematic phase shift of around 60 °.

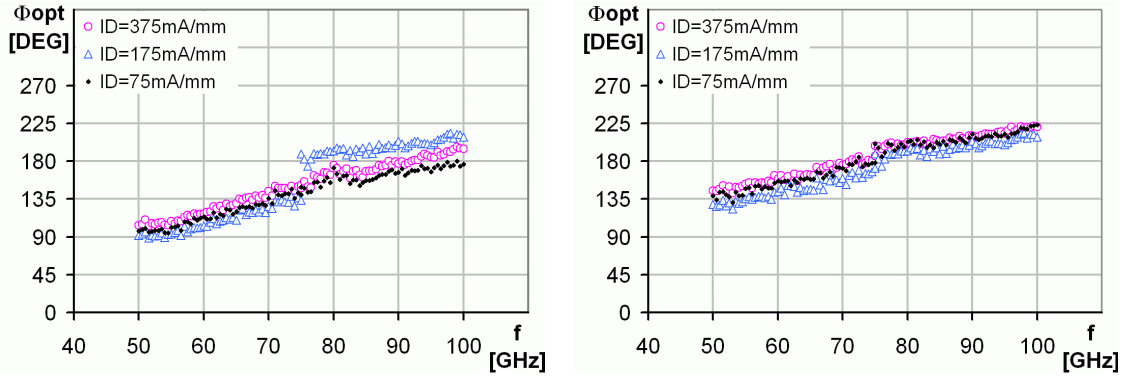


Figure 4.12: Optimum phase of input reflection coefficient Φ_{opt} within V- and W-band obtained from a 2x20 μm (l) and 4x20 μm device (r). (V_{DS} = 1 V, I_D = 75, 175 and 375 mA/mm)

Based on the RF-noise measurements, a model as shown in figure 4.13 has been established in the electronic design software ADS for the 2x20 μm and 4x20 μm devices. The model is optimized for the LNA-demonstrator design with a tradeoff between the noise figure and associated gain; operating conditions are set to a drain voltage of 1 V and a drain current density of 220 mA/mm. The model considers noise sources related to a non-perfect Schottky contact I_{ng}, the channel noise source I_{nd} and impact ionization source I_{im}. The frequency behavior of impact ionization is described by a low pass RC-network consisting of c_{im} and the noiseless resistor r_{im}. A summary of the small signal noise equivalent circuits elements is given in the annex on page 162.

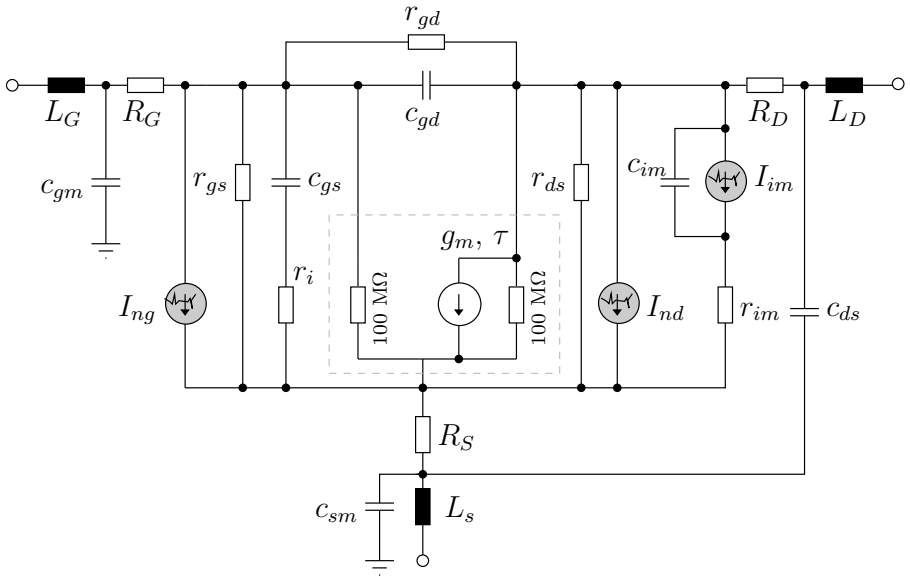


Figure 4.13: Small signal noise equivalent circuit implemented in the electronic design software Advanced Device System (ADS).

A fit of the associated gain G_{ass} for the 2x20 μm device biased at V_{DS} = 1 V and a current density of I_D = 220 mA/mm is given in the left part of figure 4.14. From 60 to 100 GHz the associated gain reduces from 10 dB to 5 dB. Besides measurement values, a fit of the noise figure is shown in the right part of 4.14 resulting in a noise figure increasing from 2 dB to 4 dB from 60 to 100 GHz. The noise figure has been calculated using Friis formula [144] in equation 4.1 for a three stage ($n = 3$) and infinity-chain amplifier (equation 4.2).

$$F_n = F_1 + \sum_{k=2}^{n} \frac{F_k - 1}{\prod_{l=1}^{k-1} G_l} \qquad (4.1)$$

$$F_\infty = \frac{F - 1}{1 - 1/G_a} + 1 \qquad (4.2)$$

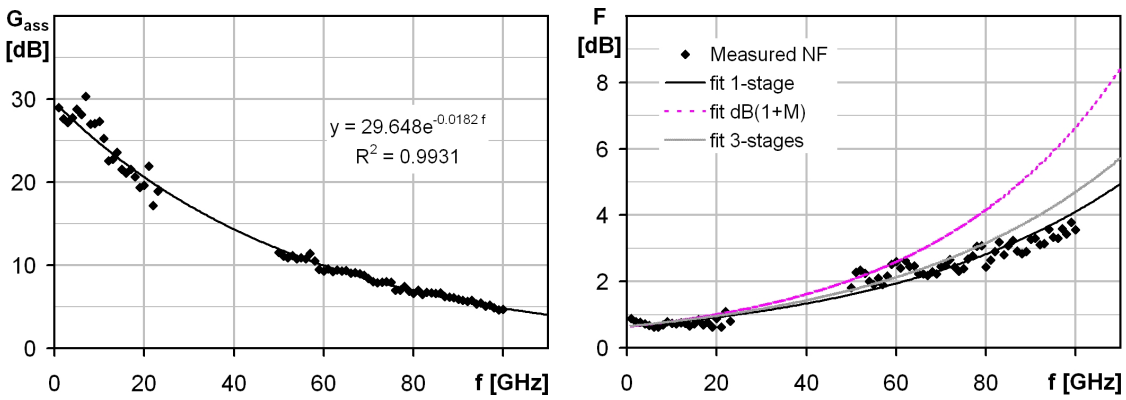


Figure 4.14: Associated gain G_{ass} (l) for a 2x20 μm low-noise metamorphic device operated at V_{DS} = 1 V and I_D = 220 mA/mm; Noise figures (r) are calculated by Friis formula for a 3-stage and infinity-chain of similar amplifier.

With this, a gain above 16 dB at 94 GHz combined with a noise figure around 4 dB can be achieved with a three stage common source LNA-design based on the metamorphic low-noise HEMT technology.

4.1.4 Low frequency noise performance

As already discussed on page 22, there is a large variety of parameters affecting the low frequency noise or flicker noise performance [145] of an electronic device. Elementary events causing noise show a characteristic time constant τ. For a period of $T = 1/f$ given by the frequency f, a statement concerning the frequency response of the noise event can be given as follows:

1. For $\tau \ll T$, the noise spectrum is white with a noise power density of $W(f) \propto f^0$.
2. For $\tau \gg T$, the noise spectrum decreases strongly over frequency with a typical power density of $W(f) \propto f^{-2}$.
3. For $\tau \simeq T$, the spectral power density is proportional to f^{-1}. In the case that all elementary noise events have the same characteristic duration, the frequency range showing $W(f) \propto f^{-1}$ is very small. A broadband $1/f$-behavior is observed for a wide distribution of time constants as described by McWorther's model [146].

An important source of $1/f$-noise for a planar active device like a HEMT is found at the interfaces between the epitaxy and passivation layers. Besides the interface and surface roughness linked to the metamorphic buffer, the high indium concentration in the channel may also affect the low frequency noise performance due to impact ionization and electron-hole-pair recombination. To evaluate the $1/f$-performance of the low-noise metamorphic devices, measurements have been performed at IRCOM laboratories (Limoges, France). The output characteristic and the corresponding gate current I_G of the test sample are shown in figure 4.15 for a 4x20 μm device. In enhancement mode, the gate current is dominated by the forward Schottky diode. Over a wide range for the gate voltage there is a negative gate current above a threshold of $V_{DS} \approx 0.9$ V. This negative (hole) current is related to impact ionization appearing in the low bandgap material of the channel. Under deep pinch-off conditions, the impact ionization current disappears due to the lack of channel electrons in the high field area.

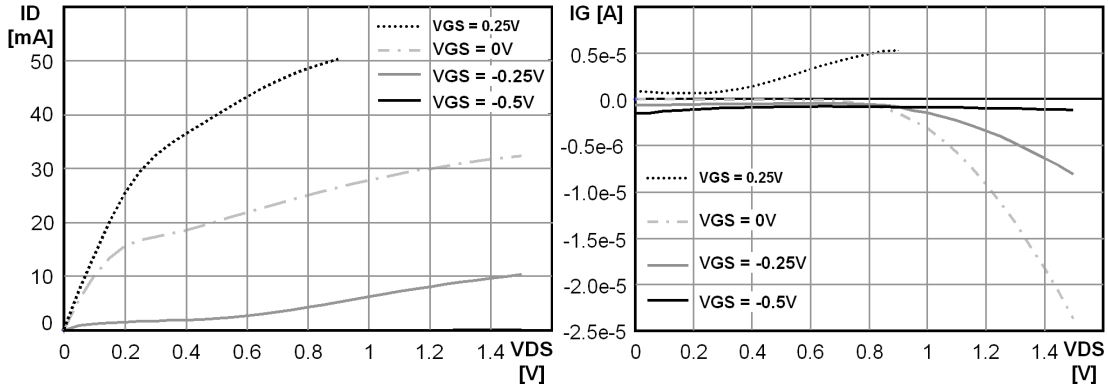


Figure 4.15: DC-output characteristic (l) and corresponding gate current I_G (r) of a 4x20 μm metamorphic low-noise device showing impact ionization above a drain voltage of 0.9 V.

The low frequency noise power density S_{ID} has been characterized in a frequency range from 100 Hz to 1 MHz. Results for a drain voltage between 0.5 V and 1.5 V and different gate bias are shown in figure 4.16. For a low drain voltage of 0.5 V there is no impact ionization; the low frequency noise response is proportional to $1/f$ and the value is related to the drain current.

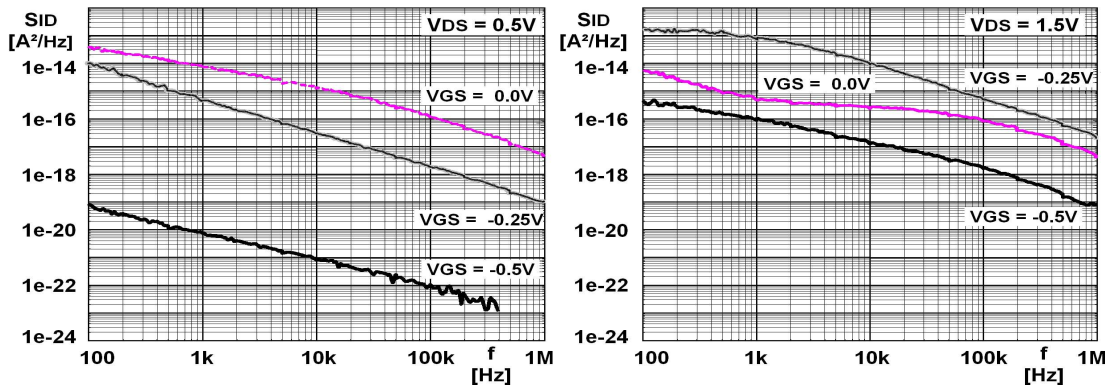


Figure 4.16: Low-frequency noise current density S_{ID} of a 4x20 μm metamorphic low-noise device at $V_{DS} = 0.5$ V (l) and $V_{DS} = 1.5$ V (r).

At open channel, there is a broadband recombination-generation center that hints towards traps located at the passivation interface in the gate recess area. For a drain voltage of 1.5 V in the right part of 4.16, there is more pronounced gate to drain leakage for the pinched device enhancing the noise power density. In contrast to a relationship with the drain current, the open channel condition shows less noise compared to device operation in moderate depletion. However, there is still a significant recombination-generation center around 100 kHz. This behavior is related to impact ionization; surface states with a slow time constant are recharged by holes and suppress recombination-generation events in the low frequency range.

To compare the low frequency noise properties of the metamorphic HEMT with the pseudomorphic one, $1/f$-measurements have been performed on pHEMT devices of similar topology. For approximately the same current density of 140 mA/mm at V_{DS} = 1.5 V, the metamorphic device shows a significantly higher noise current density in figure 4.17 than the pseudomorphic HEMT with a recombination-generation center around 3kHz. At a low drain voltage of 0.5 V, the noise is in the same order of magnitude for both technologies.

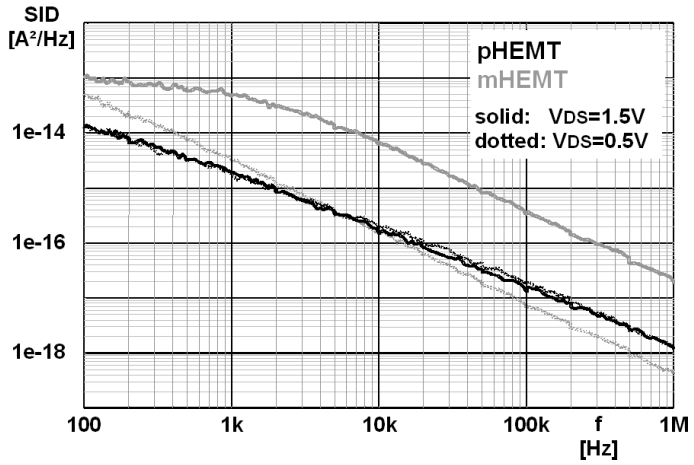


Figure 4.17: Low-frequency noise current density S_{ID} of a 4x20 μm pseudomorphic and metamorphic device operated at V_{DS} = 0.5 V and V_{DS} = 1.5 V.

Below the impact ionization threshold, the metamorphic low-noise device shows similar low frequency noise current densities compared to the pseudomorphic HEMT. However, surface traps related to a broadband recombination-generation center around 100 kHz are more pronounced. At high drain voltage, impact ionization effects become a disadvantage regarding $1/f$-noise for the metamorphic low-noise HEMT. Since $1/f$-noise plays an important role in mixer and oscillator circuits the choice of the metamorphic low-noise technology might be restricted to low noise amplifiers.

5 Power properties

Power devices have to provide a high current and voltage swing as discussed in chapter 2.3.4. While the pseudomorphic HEMT technology fulfills these requirements, the high indium concentration and low bandgap in the channel of the metamorphic structures limit the device breakdown voltage due to impact ionization. In this chapter, performances of two metamorphic HEMT technologies and a pseudomorphic HEMT technology are presented with respect to power suitability. Furthermore, the design of transistor cells and different gate configurations are discussed for optimized RF-gain and heat management.

5.1 Metamorphic power HEMT

Since device breakdown is the most limiting factor for the metamorphic devices, two strategies have been investigated for improvement:

1) Double recess configuration for a high average indium content of 50 %.

2) Single recess configuration for a reduced indium content of 43 %.

5.1.1 Double recess configuration mHEMT

The idea behind the double recess configuration is to increase the off-state breakdown voltage without the need of a large gate recess which is sensitive to surface states causing time dispersion. Charge densities below and besides the gate recess have to be adjusted in a way that the depletion zone can enter the wide recess area before reaching critical electric fields as discussed in chapter 2.4. This strategy is commonly used for pseudomorphic power HEMT technologies [103, 147] addressing for X-band applications.
The fabrication of the metamorphic double recess HEMT is based on the epitaxial structure given on page 43. As described in the technology chapter, the ohmic contacts are realized by AuGeNi and 60 s rapid thermal annealing at 360 °C. The wide recess has been defined by single resist ebeam lithography with an etched dimension of 1 μm. The 3-layer resist gate technology was used for the 150 nm T-gate definition. After the selective gate recess, the gate metal based on TiAl has been evaporated and lifted off. Before device passivation, electrical parameters have been characterized on few test structures; these devices showed a low off-state breakdown voltage around 5 V. The breakdown voltage has been determined by the small gate recess without a significant contribution from the wide recess area. The presence of the wide recess is only reflected in a high access resistance of 1.5 Ω/mm compared to the low-noise metamorphic structure of similar indium content. A dry etching step based on CF_4/ O_2 has been performed to increase the off-state breakdown to 9.5 V. The maximum saturation current at 2 V and V_{GS} = 0.4 V dropped by around 40 mA/mm to 550 mA/mm. There are two effects reducing the charge density by above mentioned post treatment. Besides enhanced surface depletion related to surface oxidation, surface states of the wide recess are located closer to the channel due to thinning of the screening layer by around 2 nm. Pulsed DC-characterization with 100 ns

pulses and 1 ms separation show acceptable time dispersion when pulsed from pinch-off conditions of V_{DS} = 2 V and V_{GS} = -1.4 V; compared to the pulse measurement from zero bias, the drain current at V_{DS} = 1 V and V_{GS} = 0.4 V drops by 12 %. The high off-state breakdown is also reflected in pulsed measurements of the 2x60 μm device shown in figure 5.1; at a current density of 200 mA/mm, an on-state breakdown of 7 V is reached with a DC-power limit of 1.6 W/mm [148]. The transfer characteristic of the metamorphic double recess device is given in the right part of figure 5.1 with a maximum transconductance of 500 mS/mm.

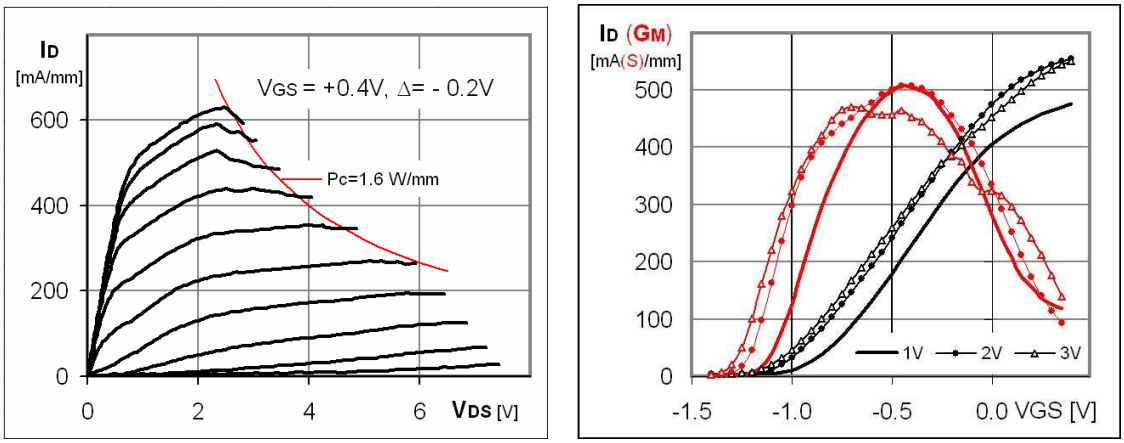


Figure 5.1: Pulsed output characteristic from bias-free separation (l) using 100 ns pulse and 1ms separation time. Static transfer characteristic (r) of a metamorphic double recess device with 50 % mean channel indium content for varied drain voltage V_{DS}.

The RF-performance has been measured on passivated 2x60 μm devices up to 50 GHz for small signal and at 10 GHz regarding power. Due to the double recess configuration the extrinsic transit frequency f_T extrapolated from $|h21|^2$ at V_{DS} = 2 V in the left part of figure 5.2 is rather low with around 100 GHz compared to 160 to 200 GHz for a single recess device of similar indium content. The maximum oscillation frequency f_{max} strongly depends on the biasing conditions and is extrapolated to approximately 200 GHz.

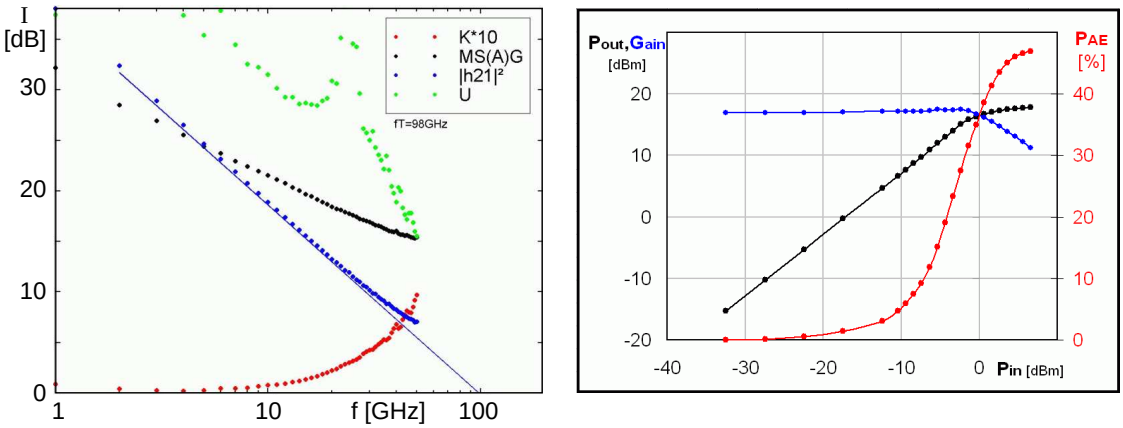


Figure 5.2: Small signal gain (l) of the double recess 2x60 μm device up to 50 GHz. The power performance (r) is measured at 10 GHz for class A-biasing at V_{DS} =4.5 V and I_D =225 mA/mm.

Load pull power measurements on the same device have been carried out for maximum gain and power as summarized in table 5.1. At 10 GHz, the maximum output power density of 500 mW/mm has been achieved with a power added efficiency of 46.9 % as shown in the right part of figure 5.2; biasing is class-A for a drain voltage of V_{DS} = 4.5 V and a current density of 225 mA/mm. Together with a linear gain of 17.5 dB, this is more or less the same result as obtained from single recess devices with a lower indium content of 43 % operated at 4 V [149]. No power characterization was possible above a drain voltage of 4.5 V due to sudden burn-out of the device.

V_{DS} [V]	V_{GS} [V]	I_D [mA/mm]	Gt [dB]	P_{1dB} [mW/mm]	P_o [mW/mm]	PAE [%]
3.0	-0.6	233	18.9	185	315	47.6
3.5	-0.6	225	18,8	227	363	46.3
4.0	-0.7	194	17.0	377	482	47.5
4.0	-0.6	221	18.8	231	367	41.8
4.5	-0.7	190	17.2	335	495	45.7
4.5	-0.6	225	17.5	392	503	46.9

Table 5.1: Power performance of the 2x60 μm double recess mHEMT for several bias conditions.

Although the off-state breakdown has been significantly improved by the double recess there is still significant impact ionization above a drain voltage of 2 V. This is obvious by the humps in the absolute gate current obtained during the measurement of the transfer characteristic in figure 5.3. Holes generated by impact ionization in the high field zone move towards the source and the recess surface. They are partly drawn towards the gate and contribute to additional gate current with a maximum value of (-)28 μA/mm at V_{DS} = 2 V, V_{GS} = -0.5 V and a drain current of 257 mA/mm. The maximum operation area which has been determined by destructive curve-tracer measurements of several devices using a different power compliance is roughly sketched in the output characteristic in the right part of figure 5.3 .

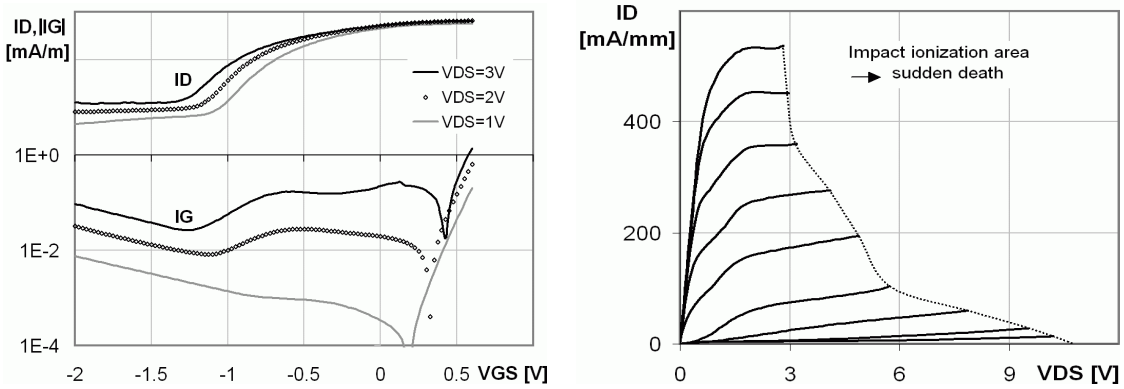


Figure 5.3: Transfer characteristic and absolute gate current (l) in logarithmic scale and output characteristic (r) for the metamorphic double recess device of 53 % mean channel indium content.

The double recess strategy helps to improve the off-state breakdown of a metamorphic device with high channel indium content. Surface oxidation after device lift off was necessary to lower charge densities below the wide recess and indicates the need for epitaxy

optimization regarding doping levels. The small signal characterization and power measurements at 10 GHz showed similar results compared to a metamorphic single recess device with 43 % indium content fabricated by the Daimler-Research group [149]. This has been confirmed by IEMN according to oral communication with D. Théron; no relevant benefit regarding power suitability has been observed for double recess metamorphic HEMTs fabricated at IEMN compared to their single recess devices. The double recess mHEMT strategy seems not to be a promising candidate for a metamorphic power HEMT technology.

5.1.2 Single recess configuration mHEMT

Thanks to the metamorphic buffer, there is no strain limitation for the indium content of the channel. A moderate indium content between the pseudomorphic and the metamorphic low-noise approach might be a compromise for a metamorphic structure which still benefits from superior transport properties but also provides sufficiently high breakdown. The fabrication of the metamorphic single recess power HEMTs is based on the epitaxy sequence given on page 44. As described in the technology chapter, AuGeNi-based ohmic contacts are annealed at 360 °C for 60 s. The 3-layer resist technology has been used to define T-gates with a gate length of 120 nm. With respect to device breakdown, the etch time for the single recess is increased by 30 s. After gate metalization (TiAl) and lift off, the devices are protected by a SiN_x passivation. Further nitride layers have been applied during the fabrication of passive devices and lines. The output characteristic in the left part of figure 5.4 indicates a quite similar envelope area for device operation compared to the double recess metamorphic HEMT. The presence of significant impact ionization even at a low drain voltage of 1 V is proven by the gate current shown in the right part of figure 5.4.

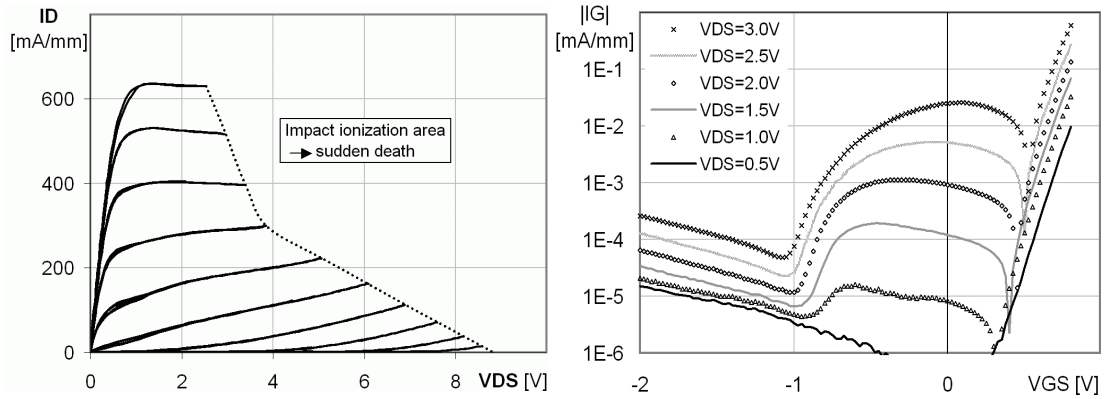


Figure 5.4: Output characteristic indicating the "safe" area of operation (l) and the gate currents caused by impact ionization (r) for varied drain voltage.

Compared to the double recess mHEMT technology, gate currents are around one order of magnitude lower with a maximum value of (-)1.1 μA/mm at V_{DS} = 2 V, V_{GS} = -0.32 V and a drain current of 375 mA/mm. This is related to the lower channel indium concentration and less impact ionization of the structure. Due to the single recess technology, the devices show a lower access resistance of 0.9 Ωmm, a higher maximum saturation

current of $I_{DS+} \sim 650$ mA/mm and a higher peak transconductance around 600 mS/mm at $V_{DS} = 2$ V. The pinch-off voltage V_{G100} is -1.0 V. A closer view on the transfer characteristic is given in figure 5.5 comparing the symmetric and asymmetric gate configuration in normal and inverse operation, where drain and source contacts are exchanged each other. Similar curves are obtained for the symmetric device with a gate to drain or gate to source spacing of 750 nm. Due to the lower source resistance, the asymmetric device with a gate to source distance of 500 nm and gate to drain distance of 1500 nm shows a slightly better maximum transconductance compared to the symmetric device. In inverse mode operation, the gate asymmetry is clearly reflected in a significant reduction of current and transconductance. This clear dependence on the source resistance is related to the split cap design.

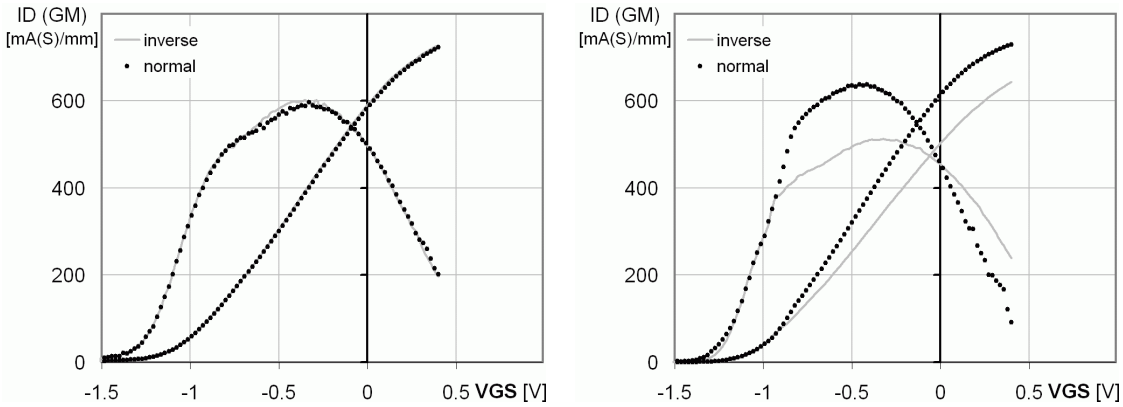


Figure 5.5: Transfer-characteristic for the symmetric (l) and asymmetric (r) gate configuration; normal (black) and inverse operation (grey), $V_{DS} = 2$ V.

The two terminal reverse diode characteristic and the three terminal device breakdown sweep for a drain leakage current of 3 mA/mm are shown in figure 5.6.

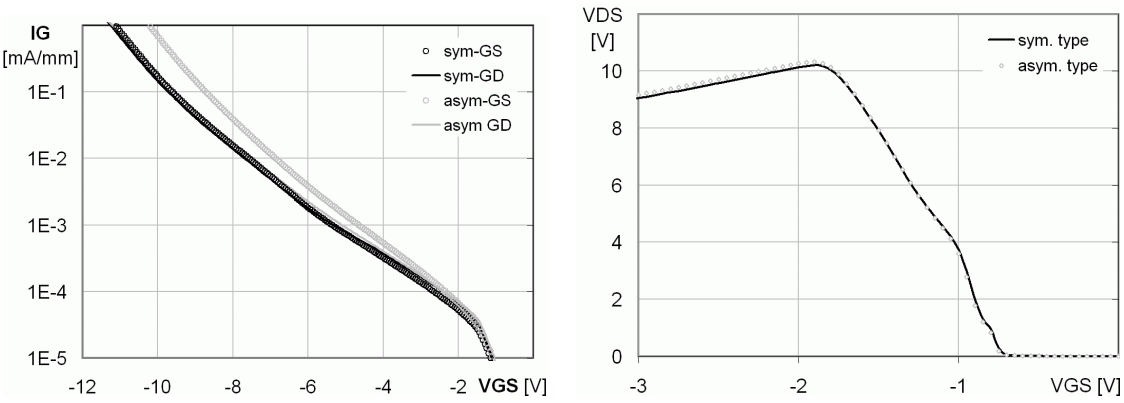


Figure 5.6: Diode reverse characteristic (l) and device breakdown performance at $I_D = 3$ mA/mm (r) for the symmetric and asymmetric gate configuration.

The gate to source breakdown voltage (at 1 mA/mm) of the asymmetric device is reduced by around 1 V due to the close ohmic contact. However, the device breakdown is dominated by the gate to drain diode, and no disadvantage can be observed for the asymmetric

device. A high device breakdown between 8.5 and 10 V is reached for the metamorphic single recess technology with 43 % channel indium content. A summary of key DC-parameters based on a statistical evaluation of the symmetric and asymmetric test devices is shown in table 5.2.

parameter	symmetric	asymmetric		$\frac{\text{asym.}}{\text{sym.}}$	$\frac{\text{asym(inverse)}}{\text{asym(normal)}}$
	normal	normal	inverse		
I_{DS+} [mA/mm]	708	730	661	+3%	-9%
I_{DSS} [mA/mm]	547	558	501	+2%	-10%
G_{max} [mS/mm]	688	715	635	+4%	-11%
R_s+R_d [Ω mm]	0.68	0.75	0.75	+10%	—
Rs [Ω mm]	0.38	0.34	0.50	-10%	+47%
V_{G100} [V]	-1.00	-0.99	-0.97	-1%	-2%
V_{bDS} [V]	9.0	8.8	8.9	-1%	-1%

Table 5.2: Comparison of key DC-parameters obtained from a statistical evaluation of symmetric and asymmetric test devices operated at V_{DS} = 2 V.

The on-wafer uniformity is demonstrated in figure 5.7 represented by the mapping of the device breakdown voltage V_{bDS}. Further mappings of the maximum saturation current I_{DS+}, the maximum transconductance G_M and the pinch-off voltage (V_{G100}) are found in the annex on page 146. While only one device located at the border of the wafer fails during the pinch-off determination, several devices burn out during the device breakdown measurement. Although a high device breakdown above 9 V is reached, devices are very sensitive towards high field operation.

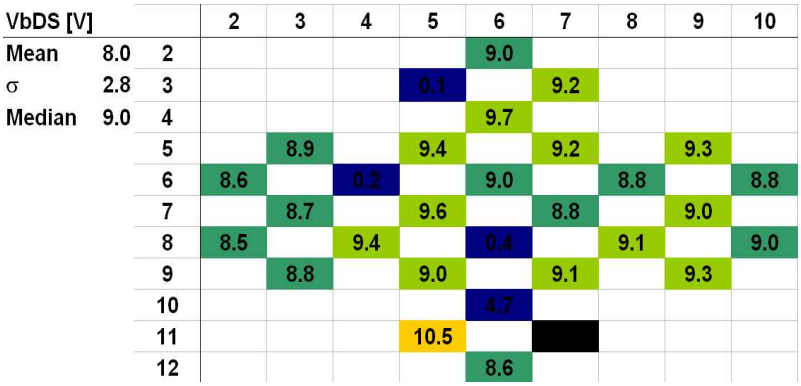


Figure 5.7: Wafer mapping of the device breakdown voltage V_{bDS} at 1 % of I_{DSS}.

To evaluate time dispersion effects, pulsed DC-measurements have been performed on symmetric and asymmetric devices with 100 ns pulses and a separation time of 1 ms. There are clear lagging effects at open channel in figure 5.8 in the case of the symmetric device; at a drain voltage of 1 V, the drain current drops by around 14 % when pulsed from the pinch-off condition of V_{DS} = 2 V and V_{GS} = -1.4 V, compared to the pulsed measurement from zero bias. No differences have been observed between the two gate configurations. This indicates that surface states on the cap layer do not contribute to time dispersion. There might be traps in the metamorphic buffer, below the Schottky contact

caused by Ar-milling before the gate metal evaporation or surface states in the gate recess. The identification of the buffer as main cause is quite difficult due to high costs for variations when relying on external epitaxy suppliers. Semiconductor damage due to the gate metalization is unlike since this had been excluded for production pHEMTs by variation of the Ar-milling. However, this is not proven for the metamorphic technology. Likely, surface states at the gate recess are responsible for the current dispersion as discussed before in chapter 2.4.

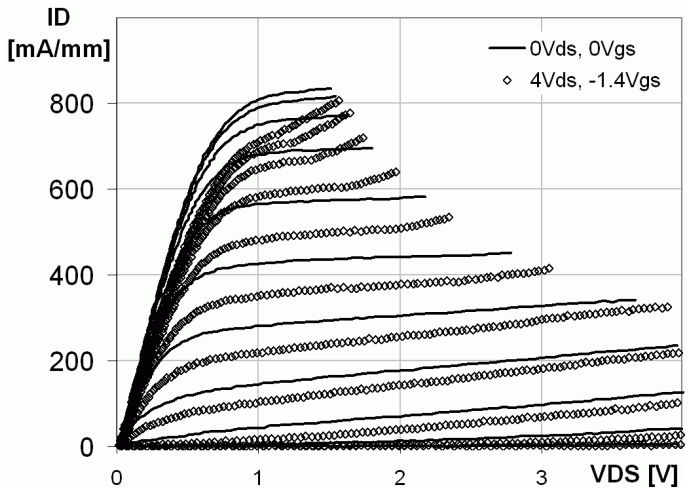


Figure 5.8: Pulsed (100ns / 1ms) DC-characteristic of the single recess power mHEMT.

5.1.3 Small signal performance

The small signal performance has been characterized up to 110 GHz for several transistor sizes and gate configurations. Bias scans for a drain voltage of 2 and 2.5 V are shown in figure 5.9 for a 2x40 μm and a 4x60 μm device.

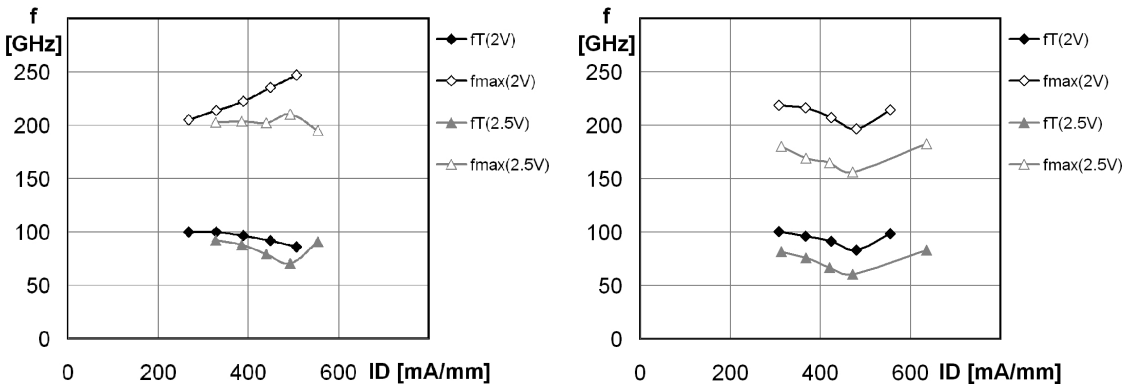


Figure 5.9: f_T and f_{max} for a 2x40 μm (l) and 6x40 μm (r) metamorphic power HEMT.

An extrinsic transit frequency around 100 GHz is reached for both device topologies at 2 V and a current density of 300 mA/mm. The maximum oscillation frequency f_{max} is above 200 GHz for a low drain voltage of 2 V and drops significantly for 2.5 V operation. Charts of the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral

gain MUG and the stability factor k are shown in the annex on page 150 to compare the symmetric and asymmetric gate configuration over the frequency. The smaller device becomes stable between 40 and 50 GHz. Due to the larger dimension of the 6x40 μm device, the parasitic elements cause earlier stabilization between 30 and 40 GHz. On both device topologies, there is slightly less gain for the asymmetric gate configuration. Table 5.3 gives a summary of the small signal equivalent circuit elements, extracted from S-parameters close to maximum gain at V_{DS} = 2.5 V and V_{GS} = -0.4 V.

parameter	2x40 μm		$\frac{\text{asym.}}{\text{sym.}}$	6x40 μm		$\frac{\text{asym.}}{\text{sym.}}$
	symmetric	asymmetric		symmetric	asymmetric	
I_{DSS} [mA/mm]	322	344	—	311	313	—
g_{me} [mS]	73.5	74.9	+2.0%	209.4	207.9	-0.7%
c_{gs} [fF]	115.9	125.2	+8.1%	339.6	371.4	+9.4%
c_{gd} [fF]	11.1	10.9	-2.1%	35.0	33.5	-4.4%
r_{ds} [Ω]	310.3	313.1	+0.9%	109.7	102.7	-6.4%
r_S [Ω]	4.75	4.62	-2.8%	1.49	1.44	-3.3%
$f_T(c_{gs})$ [GHz]	101	95	-6%	98	89	-9%
f_{Tc} [GHz]	92	88	-4%	89	82	-8%
f_{max} [GHz]	193	189	-2%	200	180	-10%

Table 5.3: Comparison of the small signal equivalent circuit elements for symmetric and asymmetric tests devices of 2x40 μm and 6x40 μm at V_{DS} = 2.5 V and V_{GS} = -0.4 V.

Unlike the static transconductance, the RF-transconductance g_{me} does not clearly benefit from the reduced source-resistance; yet the input capacitance c_{gs} increases by more than 8 % due to the reduced distance between gate and source. This lowers the transit frequency and the maximum oscillation frequency. Regarding small signal performance, the symmetric gate configuration shows slight advantages compared to the asymmetric gate configuration.

5.1.4 Power performance at 94 GHz

Power characterizations at 94 GHz have been carried out at IEMN on a load pull setup as sketched in figure 5.10. The power source is realized with an IMPATT diode which provides a maximum output power of 180 mW at 94 GHz. To protect the power source, an isolator is used to block reflected waves. The input power is varied with an attenuator. The injected and reflected part of the input power is monitored via a coupler and two bolometers. Manual tuners are used at the input and the output of the device to adjust for optimum power matching. The output signal is divided by a coupler for output power detection with a bolometer and the 50 Ω termination load.

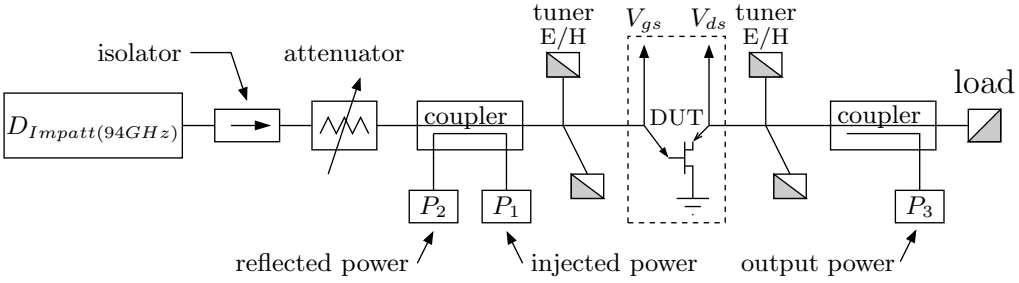


Figure 5.10: Power measurement setup working at 94 GHz.

The power performance has been characterized on-wafer on very small devices of 2x30 μm due to insufficient output power of the power source. For class-A operation at a drain voltage of 3 V and 260 mA/mm current density, the metamorphic device with the symmetric gate configuration shows a linear gain of 8.5 dB, a maximum output power of 13.6 dBm and a maximum power added efficiency of 28 % in figure 5.11. The output power corresponds to a power density of 380 mW/mm; the output power densities at 1 dB and 3 dB-compression are 180 mW/mm and 260 mW/mm with a PAE of 19.8 and 26.2 %, respectively.

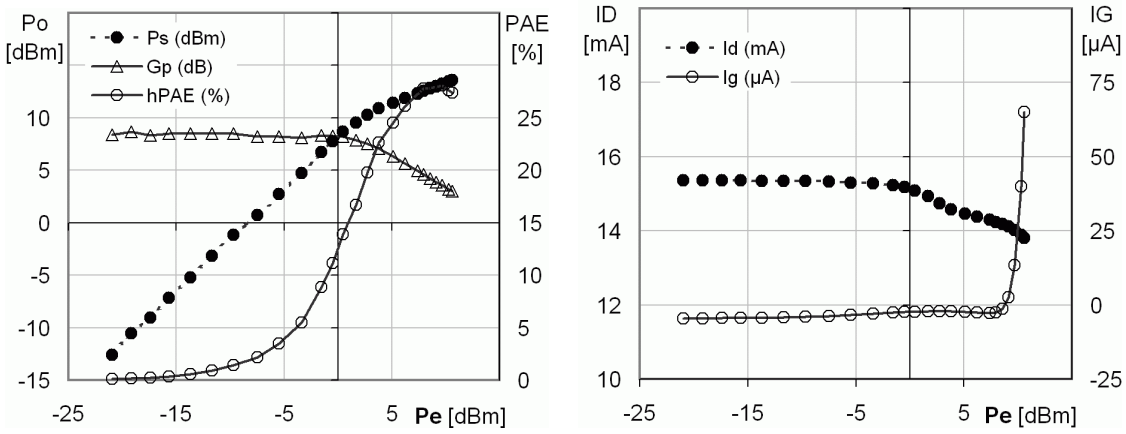


Figure 5.11: Power characterization at 94 GHz of a 2x30 μm metamorphic single recess power HEMT of symmetric gate configuration; the bias is V_{DS} = 3 V and V_{GS} = -0.5 V.

The reduction of the drain current under device compression indicates a clipping at open channel. The increasing gate current is linked to the forward current of the Schottky diode. As expected from the small signal characterizations, devices with the asymmetric gate configuration showed very similar results concerning power and gain. The power properties of the metamorphic single recess devices are close to state-of-the-art results [150, 22]. However, devices burn out for class-A operation at drain voltages exceeding 3 V. The single recess metamorphic power HEMTs do not benefit from the high off-state breakdown voltage.

5.2 Pseudomorphic power HEMT

A less sensitive on-state breakdown is expected for the pseudomorphic power HEMT due to the higher bandgap of the epitaxy layers. The disadvantageous transport properties

compared to the metamorphic approach, however, has to be compensated by a reduced gate length to obtain similar gain at high frequencies. The small gate length promotes short channel effects lowering the output resistance and makes it more difficult to obtain a high device breakdown due to enhanced drain leakage currents.

5.2.1 DC-performance

The output characteristic of a 1x100 μm pseudomorphic power HEMT is shown in figure 5.12. At open channel, the drain supply can exceed 4 V without device destruction. Due to higher gate leakage compared to the single recess power mHEMT, the humps related to impact ionization in the right chart appear at a drain voltage of 3 V; hole current levels are slightly lower for the pHEMT. The pHEMT can manage high gate currents in the order of 1 mA/mm for a drain voltage of 4 V and is more robust than the metamorphic version.

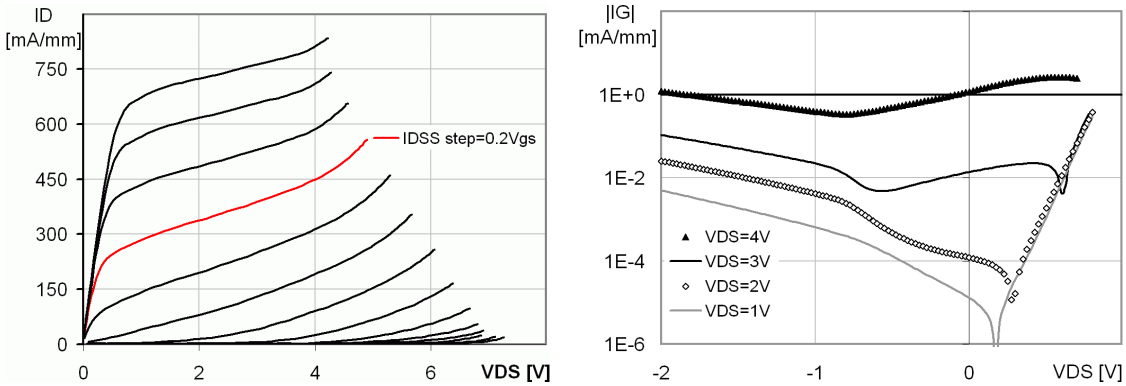


Figure 5.12: Output characteristic (l) of a 1x100 μm pseudomorphic HEMT. Absolute gate current (r) of the device for a gate voltage sweep from -2 to 0.8 V and a drain voltage from 1 to 4 V.

At V_{DS} = 2 V, the maximum saturation currents I_{DS+} are 680 mA/mm and 705 mA/m for the symmetric and asymmetric device. In figure 5.13, the gate asymmetry is evident by a direct comparison of the asymmetric device in normal and inverse mode operation.

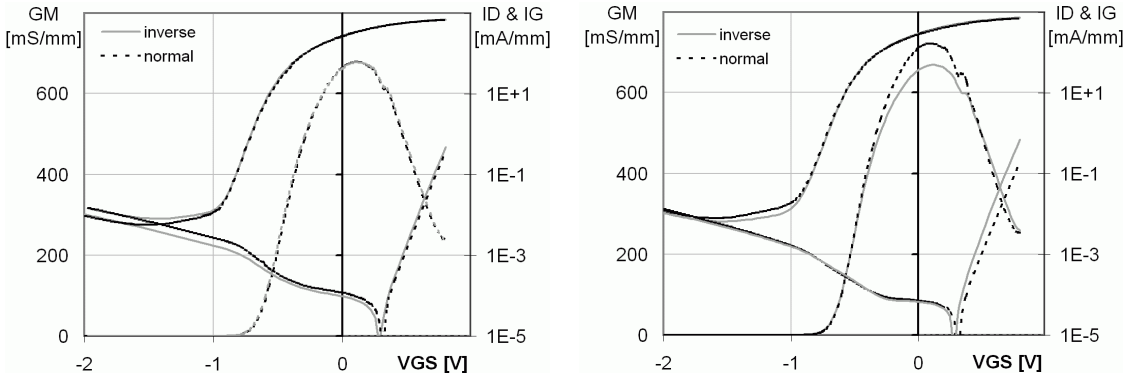
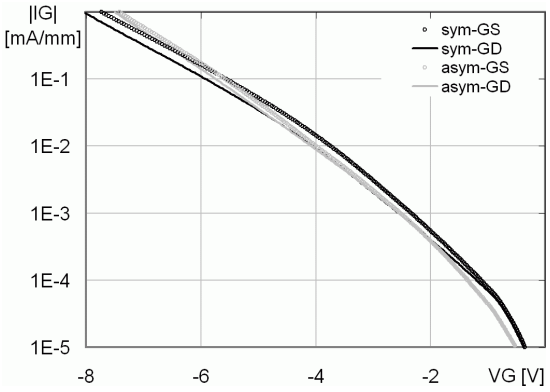


Figure 5.13: Transconductance of 1x100 μm pseudomorphic test device with symmetric (l) and asymmetric (r) gate configuration in normal and inverse operation mode.

For a similar pinch-off voltage of V_p = -0.65 V, the asymmetric gate configuration provides the higher maximum transconductance of 720 mS/mm compared to 680 mS/mm for the

symmetric gate. However, the difference is less pronounced compared to the single recess metamorphic power device. The difference of the source resistance is rather low due to the thick highly doped cap. The same argument explains that the reverse characteristic of the source diode for the asymmetric device in figure 5.14 shows no significant difference regarding the two terminal breakdown voltage.



VbDS [V]	2	3	4	5	6	7	8	9	10
	2					>>>				
	3				6.3		6.0			
Average 6.3	4					6.2				
σ 0.2	5		6.6		>>>		6.2		6.4	
Median 6.3	6	5.6		6.1		6.3		6.3		6.5
	7		6.3		6.4		6.4		6.4	
	8	6.3		6.2		6.3		6.5		6.6
	9		6.6		6.2		6.2		6.5	
	10					6.3				
	11				6.5		6.3			
	12					6.5				

Figure 5.14: Diode reverse characteristic (l) and device breakdown at 1 % of I_{DSS} which is around $I_D = 3$ mA/mm (r).

The device breakdown V_{bDS} is defined as the maximum drain voltage obtained during a gate voltage sweep for a constant drain leakage current of 1 % of I_{DSS}. The device breakdown of the pseudomorphic single recess power HEMT is around 2.5 V lower compared to the single recess metamorphic power HEMT. As shown in the right part of figure 5.14, a higher device breakdown of 6.9 V versus 6.1 V is reached for the symmetric gate configuration. Based on a statistical evaluation, there is a systematically lower device breakdown for the asymmetric gate configuration with a difference of 0.4 V. If operated in inverse mode, the gate asymmetry is not reflected in the device breakdown; there is a higher drain leakage for the gate located closer to the ohmic contact. However, the V_{bDS}-reduction is small, and no significant electrical impact is expected related to the asymmetric gate configuration.

During the device breakdown characterization, electron-hole pairs are generated in the high field area related to impact ionization. While generated electrons move towards the drain contact being part of the drain current I_D, holes contribute to the gate I_G and source current I_S. Holes may recombine radiative with incoming channel electrons or are drawn off to the source or gate contact. Light emission has been observed with a black-and-white CCD-camera, offering some sensitivity at near infrared as shown in figure 5.15 for a 1x100 μm test device with asymmetric gate configuration. For similar biasing conditions of 10 mA/mm drain leakage and -1.5 V gate voltage, the same drain voltage of 6.1 V with slightly different gate currents of 1.6 mA/mm and 1.7 mA/mm have been detected in normal and inverse operation mode. Light emission is "white" as far this can be described by visual observation. This fits to a broad band spectrum linked to the recombination of high energetic electron hole pairs created by impact ionization [56]. Since light emission is very weak, image processing has been applied such as transformation to false colors and an overlay with the device structure. Nearly no light emission is observed at the source side of the gate for the asymmetric device operated in normal mode. Due to the short

distance to the source, holes are directly drawn off towards the source contact without radiative recombination. In inverse mode, the emission intensity strongly increased. While light emission is observed at the source side of the gate for device pinch-off, emission moves to the drain side of the gate for open channel conditions; holes generated in the drift zone recombine rapidly due to the large number of electrons in the channel. Light emission of the symmetric gate configuration is similar in normal and inverse mode but of higher intensity related to the 0.4 V higher device breakdown voltage.

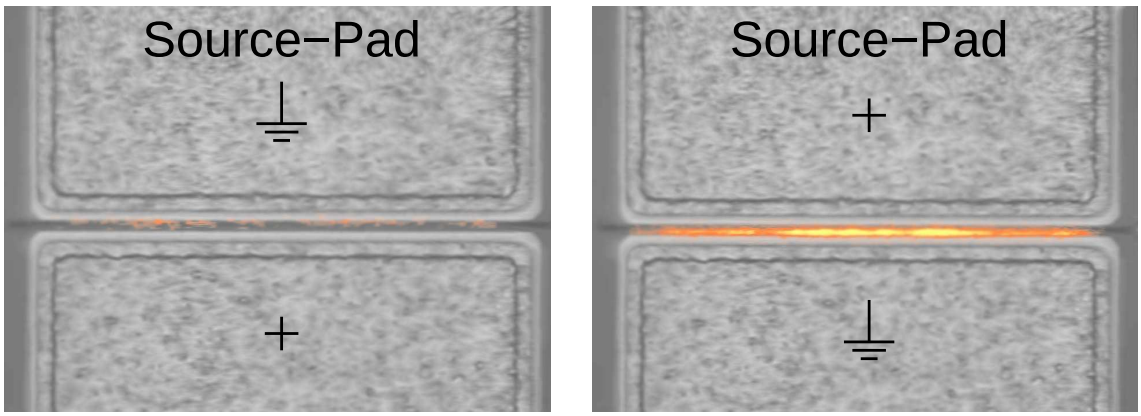


Figure 5.15: Light emission during normal (l) and inverse mode (r) operation of the asymmetric device close to the off-state breakdown voltage.

A summary of key DC-parameters based on the statistical evaluation of symmetric and asymmetric test devices is given in table 5.4. Due to the highly doped thick cap, there is less benefit for the asymmetric device regarding a lower source resistance compared to the metamorphic power technology.

parameter	symmetric	asymmetric		$\frac{\text{asym.}}{\text{sym.}}$	$\frac{\text{asym(inverse)}}{\text{asym(normal)}}$
	normal	normal	inverse		
I_{DS+} [mA/mm]	636	669	664	+5%	-1%
I_{DSS} [mA/mm]	239	259	248	+8%	-4%
G_{max} [mS/mm]	761	770	758	+1%	-2%
R_S+R_D [Ω mm]	0.50	0.51	0.51	+2%	—
Rs [Ω mm]	0.36	0.34	0.45	-5%	+31%
V_p [V]	-0.54	-0.57	-0.57	-5%	—
V_{bDS} [V]	6.3	6.0	6.0	-6%	—

Table 5.4: Comparison of the key DC-parameters obtained from a statistical evaluation of symmetric and asymmetric tests devices; V_{DS} = 1 V.

The on-wafer homogeneity is represented by the mapping of the maximum transconductance G_{max} in figure 5.16 for the symmetric 1x100 μm device. Further mappings are found on annex page 148. Apart from two failing devices, spreads are below 5 % referring to their mean values. Due to different biasing at V_{DS}=1 V and four pole probing on the automatic test bench, values deviate slightly from the manual in-line DC-characterization.

Gmax [mS/mm]			2	3	4	5	6	7	8	9	10
		2					>>>				
		3				776		765			
Average	761	4					777				
σ	17	5		722		>>>		769		765	
Median	764	6	713		754		744		767		761
		7		762		756		770		770	
		8	754		762		761		769		769
		9		736		742		765		787	
		10					787				
		11				764		780			
		12					752				

Figure 5.16: Mapping of the maximum transconductance for V_{DS} = 1 V.

Pulsed DC-characterizations have been performed using 100 ns pulses and 1 ms separation. As shown in figure 5.17, the pseudomorphic power technology shows little time dispersion effects at open channel. At the reference point of V_{DS} = 1 V and V_{GS} = 0.6 V, lagging is in the order of 6 % comparing the curves pulsed from zero bias and pinch-off conditions of V_{DS} = 0 V and V_{DS} = -2 V. Lagging diminishes to around 3 % with the onset of impact ionization, when pulsed from pinch-off conditions at high drain voltage.

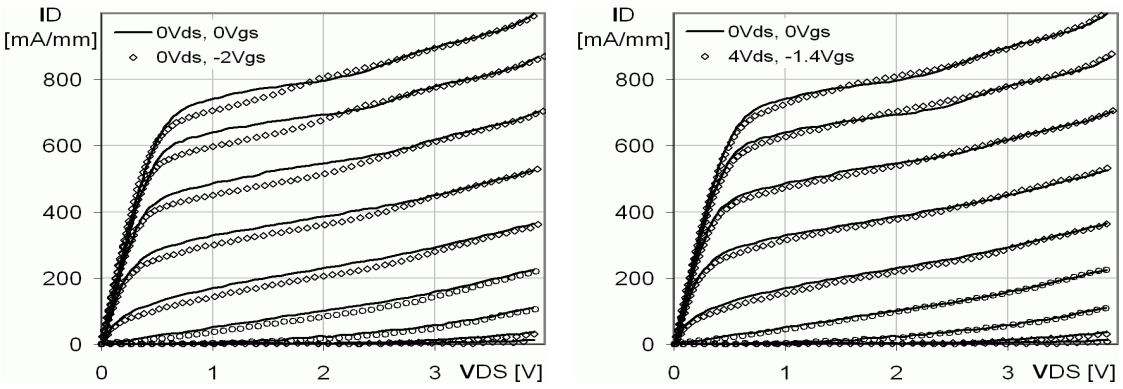


Figure 5.17: Pulsed DC-characteristic (100 ns /1 ms) from different separation points.

Compared to the metamorphic single recess power technology, the pseudomorphic device shows less current dispersion. No difference, however, is observed between the asymmetric and symmetric gate configuration.

5.2.2 Small signal performance

Similar to the DC-characterizations there are no significant differences for the small signal properties between the symmetric and asymmetric gate configuration. The small signal performance has been characterized up to 110 GHz for several transistor sizes and gate configurations. Bias scans for a drain voltage of 2 and 2.5 V are shown in figure 5.18 for a 2x40 μm and a 4x60 μm device. Compared to the metamorphic power HEMT, the pseudomorphic HEMT shows a higher transit frequency with values around 150 GHz for both device topologies. The maximum gain is reached for a current density of around 400 mA/mm with a maximum oscillation frequency f_{max} close to 250 GHz. The drop of

f_T and f_{max} for increased drain voltage is significantly less pronounced compared to the mHEMT and shows almost similar results between 2.5 and 3 V operation.

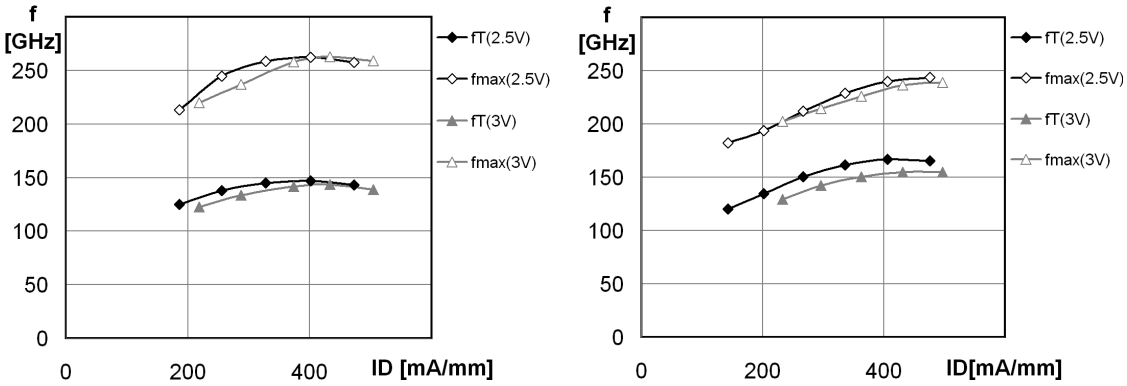


Figure 5.18: f_T and f$_{max}$ from a 2x40 μm (l) and 6x40 μm (r) pseudomorphic power HEMT.

To compare the gate configurations, elements of the small signal equivalent circuit have been extracted by fitting S-parameter results up to 110 GHz as summarized in table 5.5 for two device topologies of 2x40 μm and 2x60 μm.

parameter	2x40 μm		$\frac{\text{asym.}}{\text{sym.}}$	6x40 μm		$\frac{\text{asym.}}{\text{sym.}}$
	symmetric	asymmetric		symmetric	asymmetric	
I_{DSS} [mA/mm]	354	366	—	371	384	—
g_{me} [mS]	85.9	93.3	+8.6%	245.6	259.3	+5.6%
c_{gs} [fF]	82.3	96.1	+16.8%	205.5	211.4	+2.9%
c_{gd} [fF]	10.8	10.9	+0.9%	39.8	40.8	+2.4%
r_{ds} [Ω]	147.4	125.1	-15.1%	52.7	49.3	-6.5%
r_S [Ω]	4.4	4.2	-4.5%	1.34	1.26	-5.9%
$f_T(c_{gs})$ [GHz]	166	155	-7%	190	195	+3%
f_{Tc} [GHz]	147	139	-5%	159	164	+3%
f_{max} [GHz]	223	204	-9%	187	182	-3%

Table 5.5: Comparison of the small signal equivalent circuit elements for symmetric and asymmetric tests devices of 2x40 μm and 6x40 μm operated at V_{DS} = 3.0 V and V_{GS} = 0 V.

The charts for the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral gain MUG and the stability factor k are shown on annex page 151 to compare the symmetric and asymmetric 2x40 μm and 6x40 μm devices. The asymmetric gate configuration shows slightly less gain for the small device due to an increased input capacitance c_{gs}. In contrast, no significant difference is observed for the large device geometry, where benefits in transconductance are compensated by the increased input capacitance. The asymmetric gate configuration provides no advantage in comparison to the symmetric device. Since the pseudomorphic power technology provides a higher transit and maximum oscillation frequency even at higher operation voltage compared to the metamorphic power HEMT, better RF-power properties are expected for the pseudomorphic HEMT.

5.2.3 Power performance at 94 GHz

Small pseudomorphic power HEMTs in coplanar layout of 2x30 μm and a gate length of 70 nm have been characterized on the 94 GHz power measurement setup of IEMN. In class-A operation at 4 V and 400 mA/mm drain current, the best device provides a linear gain of 10.5 dB, a maximum output power of 16.9 dBm corresponding to a power density of 812 mW/mm and a maximum power added efficiency of 36.4 %. At the compression level of 1 dB and 3 dB, the output power density and PAE are 460 mW/mm and 792 mW/mm and 21.9 % and 36.4 %, respectively. Results fit well with the theoretically expected linear power density of 470 mW/mm calculated for a voltage and current swing of 6 V and 630 mA/mm.

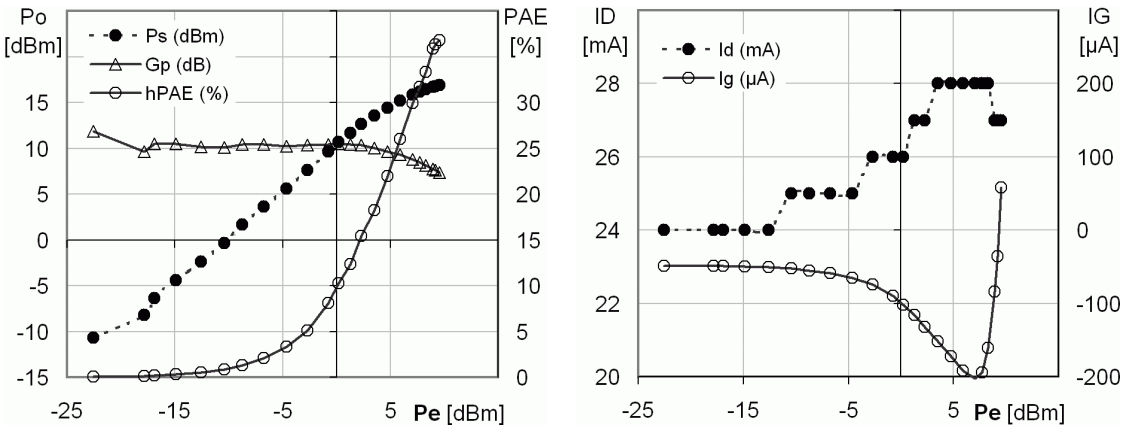


Figure 5.19: Power characterization at 94 GHz of a 2x30 μm pseudomorphic HEMT operated at V_{DS} = 4 V and a drain current density of 400 mA/mm.

As shown in the left part of figure 5.20, the output power at 94 GHz increases linearly with the drain voltage, and a maximum power density of 900 mW/mm is reached at 4.5 V. Operation at such high drain voltage is critical regarding reliability; likely there is strong long-term device degradation due to impact ionization and high gate currents. However, the power performance is still very promising for moderate operation at 3.5 V: The maximum output power density is 650 mW/mm with a power gain of 5.5 dB. The linear gain and a maximum PAE are 8.5 dB and 28 %, respectively.

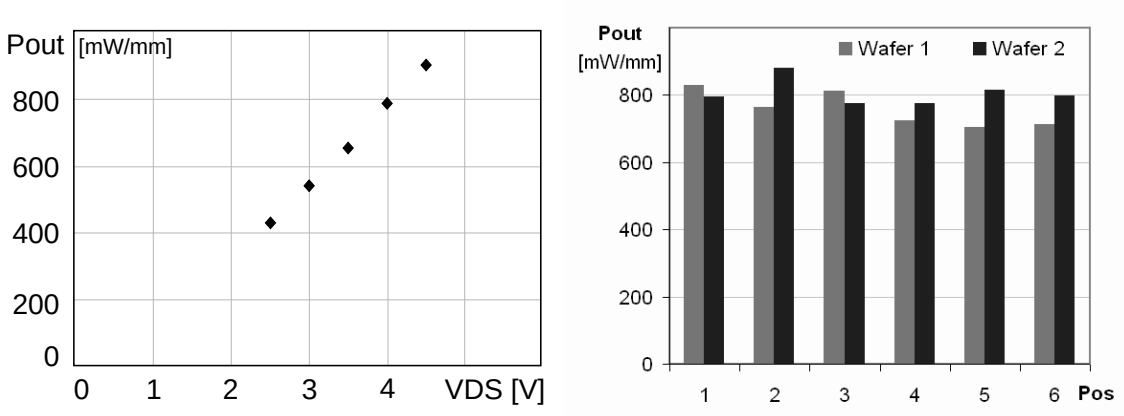


Figure 5.20: Power density as a function of the drain voltage (l) and reproducibility over 6 positions from two wafers (r).

Characterizations of several devices from two separately fabricated wafers in the right part of figure 5.20 show a good reproducibility; all samples provide more than 700 mW/mm power density on the 2x30 μm device biased in class-A at $V_{DS} = 4$ V. Due to a high robustness regarding impact ionization and the small gate length realized by the dielectric assisted gate technology, the pseudomorphic power HEMT demonstrates state-of-the-art power performance at 94 GHz [151, 152].

5.3 Base-cell optimization

Besides the gate configuration, several types of transistor base-cells as sketched in figure 5.21 have been simulated, fabricated and characterized with respect to their small signal performance. On the standard cell I), the drain supply is realized by a comb structure. The inner source pads are connected by air bridges contributing to the source inductance and drain to source capacitance. Outer source pads are connected to the backside metalization by via interconnects. The second base-cell II) shows a quite similar structure, but every source pad is connected to the backside by an individual source via. This reduces the source inductance on large multi finger devices. However, source pads with an individual source via require more space. This results in a higher drain inductance and drain to source capacitance. The fish bone structure III) promises superior RF-performance due to the benefits coming from the individual source via and the most compact design. Furthermore, the inevitable phase shift between the gate fingers are expected to be partly compensated by the drain access. On the other hand, high drain to source capacitances and a large drain inductance are expected due to air bridges connecting the drain pads on large devices.

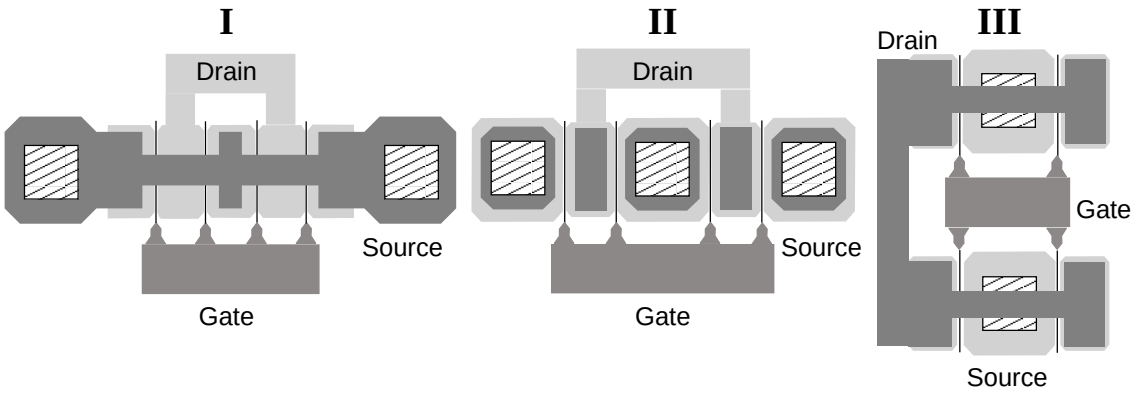


Figure 5.21: Different types of 4-finger base-cells with the same gate-periphery: I) Outer source pads are connected to the wafer back side by vias; the central source pad is connected by air-bridges. II) All source pads are connected to the wafer back side by individual vias to reduce the source inductance. III) The fish bone configuration allows a more compact design including the benefits from the individual source via. However, the complexity of the drain access increases due to the need of air bridges.

The base-cells have been simulated at IEMN using commercial electromagnetic field simulators like HFSS and ADS-momentum. The principles of the simulations are sketched in figure 5.22 for the example of a 8 finger device with individual source vias. Besides

the extrinsic parasitic elements (not shown) coming from the outer metalization levels, the model is divided up into each gate finger structure. Furthermore, there are parasitic elements typical for the base-cell like the RCL-circuit at each source pad. This separation into single gate finger structures allows to consider the phase relations of the incoming and outgoing waves for each gate finger.

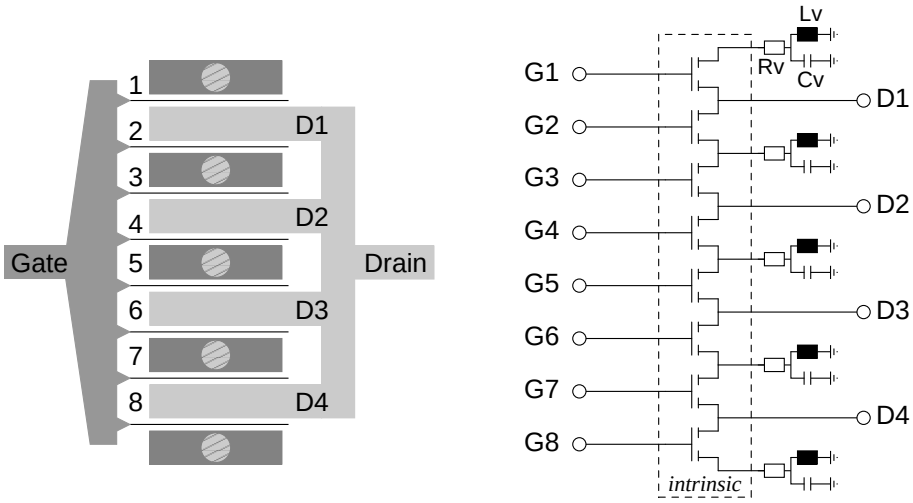


Figure 5.22: Model of an individual source via device regarding the phase relation at each gate and drain port; parasitics coming from the outer parts of the gate and drain pad are neglected.

The phase relations at 94 GHz are summarized in table 5.6 for the different base-cell designs of a 8-finger device. The phase difference between neighboring gate fingers mainly depends on their distance and wave propagation within the gate bus. This explains the higher difference between gate two and three (G_2G_3) compared to gate three and four (G_3G_4) on the standard structure I) where gate two an three are separated by the larger source pad. On the second structure, this effect is more pronounced since the individual source vias require even more space. The strongest phase shift is observed for the fish bone structure where the gate access is parallel to wave propagation, representing the worst case situation. However, some compensation due to the opposite effect for the outgoing wave at the drain bus may cause better RF-properties for the fish bone device.

	I) standard	II) s-vias	III) fish bone
$\Phi(G_1G_2) = \Phi(G_8G_7)$	$1.3°$	$3.1°$	$26.3°$
$\Phi(G_2G_3) = \Phi(G_7G_6)$	$2.2°$	$6.0°$	$19.4°$
$\Phi(G_3G_4) = \Phi(G_6G_5)$	$1.7°$	$2.4°$	$32.7°$
$\Phi(G_4G_5)$	$0°$	$0°$	$0°$

Table 5.6: Phase difference at 94 GHz between neighboring gate fingers for different base-cell configurations.

Simulations performed at IEMN [153] predict 1 dB less maximum available gain at 94 GHz for the eight finger fish bone structure compared to the standard structure. This is mainly due to a high parasitic capacitance between the drain air bridges and the source pads. Around 2 dB more maximum available gain has been calculated for the individual

source via structure thanks to a lower source inductance. To confirm the simulations results for pHEMT devices, the base-cells have been characterized on a S-parameter setup operating from 1 to 110 GHz. The charts for the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral gain MUG and the stability factor k are shown on annex page 152 to compare between the different transistor cells based on the 2x40 μm and 6x40 μm topology. Bias conditions are 3 V for the drain and -0.1 V for the gate which is close to the maximum gain. For the small device, the worst performance is observed for the fish bone structure due to a high output capacitance c_{ds} as given in table 5.7.

	2x40 μm			6x40 μm		
	I) standard	II) s-vias	III) fish bone	standard	II) s-vias	III) fish bone
c_{ds} [fF]	27.6	27.2	**35.4**	59.3	**82.6**	**87.1**
L_G [pH]	33.9	36.4	31.6	25.0	23.7	**36.2**
L_D [pH]	**55.6**	**49.5**	34.8	26.3	**31.8**	**30.4**
L_S [pH]	11.3	11.3	9.8	**14.3**	6.4	5.4
r_S [Ω]	4.4	4.1	3.8	1.0	1.4	1.4

Table 5.7: Parasitic elements of the small signal equivalent circuit for the different base-cells of 2x40 μm and 6x40 μm.

The characteristics of the individual source via and the standard structure are slightly disturbed by resonance phenomena around 52 GHz and 105 GHz. There are little differences in $|h_{21}|$ and the maximum stable gain between the standard and individual source via structure. Yet, the individual source via device provides more maximum available and unilateral gain. For the 6x40 μm structure, the fish bone configuration, again, shows the worst small signal performance due to a high drain to source capacitance and high drain and gate inductance; there is not sufficient benefit from the source vias or phase compensation. Base-cell I) with individual source vias performs the best but advantages in gain are less compared to the simulation. The lower source inductance is hardly equalized by an increased drain to source capacitance and drain inductance. Due to intensified resonance peaks at 52 GHz and 105 GHz, a comparative evaluation of the high frequency performance between the standard and individual source vias base-cell is quite hard; the large differences of e.g. maximum available gain around 100 GHz may be related more to resonance phenomena than to the base-cell performance itself.

Small signal characterizations clearly confirm disadvantages regarding gain for the fish bone structure as simulated. On the other hand, the individual source via design shows only slightly more gain compared to the standard structure.

5.3.1 Thermal aspects

In power devices, heat is generated due to power losses. Devices heat up themselves affecting the performance as well as their life-time. A reliable power device should not exceed its thermal limits given by a large variety of aspects starting at the semiconductor composition, the base-cell design, chip assembly and even the heat management of an assembled module. On the device fabrication level, the best opportunities to keep

devices cool are found in the semiconductor composition and base-cell design. The base-cells might be optimized from the thermal point of view, however, this may cause some conflicts with the electrical performance especially at high frequencies. In this section, thermal properties of the power devices are evaluated based on two and three dimensional thermal simulations to separate effects coming from the semiconductor composition and base-cell design. A basic element for thermal simulations within a semiconductor device is the description of the heat transfer in solids by heat diffusion. Considerations are based on the energy balance of an infinite small cube of the size $d_x\, d_y\, d_z$ as sketched in the left part of figure 5.23, symbolizing the continuity equation. The model includes a heat source which generates the thermal energy E_ϑ and the thermal flux q_x, q_y, q_z entering and leaving the volume $q_{x+dx}, q_{y+dy}, q_{z+dz}$.

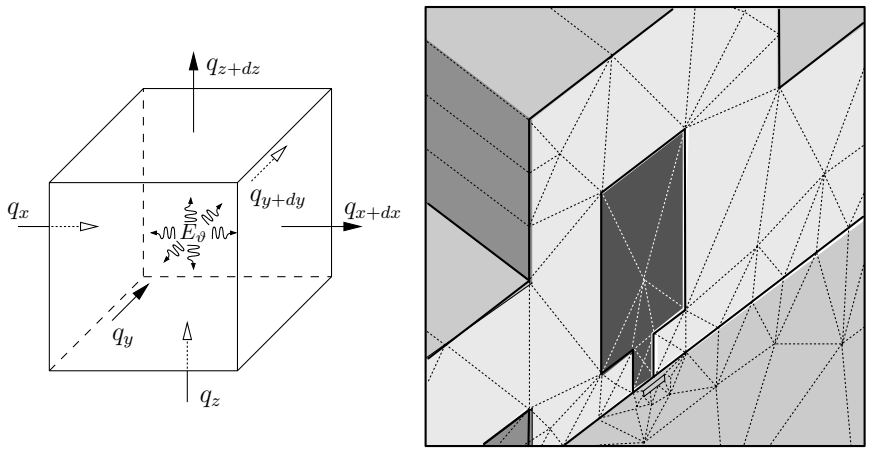


Figure 5.23: Subdivision of the transistor geometry in finite elements.

The generation of thermal energy E_ϑ is positive for exothermic and negative for endothermal reactions and can be described by the power density $g(x, y, z, t)$ of the heat source in equation 5.1.

$$E_\vartheta = g(x, y, z, t)\, d_x\, dy\, dz \tag{5.1}$$

The variation of the energy per volume element E_{vol} can be described by the specific heat C_p of the material and its density ρ as follows

$$E_{vol} = \rho \cdot C_p \cdot \frac{\delta T}{\delta t}\, d_x\, d_y\, d_z \quad = \quad \sum \Phi + E_\vartheta, \tag{5.2}$$

with the energetic flux $\Phi = q \cdot A_s$ defined as the heat flux though the surface A_s of the e.g. cubic volume-element. Applying a Tailor series of first order to the thermal flux leads to

$$\sum \Phi = (q_x - q_{x+dx})\, d_y d_z + (q_y - q_{y+dy})\, d_x d_z + (q_z - q_{z+dz})\, d_x d_y \tag{5.3}$$

$$= \text{-} \left(\frac{\delta q}{\delta x} + \frac{\delta q}{\delta y} + \frac{\delta q}{\delta z} \right) d_x\, d_y\, d_z\ . \tag{5.4}$$

The combination with equations 5.1 and 5.2 results in the heat diffusion in equation 5.6, to be solved for given material properties, initial state and boundary conditions.

$$\rho \cdot C_p \frac{\delta T}{\delta t} = -\frac{\delta q}{\delta x} - \frac{\delta q}{\delta y} - \frac{\delta q}{\delta z} + g(x,y,z,t) \quad (5.5)$$

$$= \nabla(\kappa \nabla(T)) + g(x,y,z,t) \quad (5.6)$$

There are three types of boundary conditions:

- Dirichlet-condition: a constant temperature is imposed on a given surface
- Neuman-condition: a power flux is imposed on a given surface
- Cauchy-condition: a thermal flux is expressed by a temperature difference between a given surface and a reference temperature

To form a thermal model for the active device, it is subdivided in small volume elements. The mesh density is increased close to the heat source located in the channel at the right border of the gate to maintain a high accuracy. To solve the Dirichlet problem for the pseudomorphic and metamorphic power HEMT structures with a point heat source dissipating a constant power density of 1 W/mm, the commercial finite element solver ANSYS [154] was used. Thermal simulations have been carried out at IRCOM laboratories (Limoges, France). Material properties like the thermal conductivity κ or the specific heat C_p required for thermal simulations are given in table 5.8 [155].

Material	$\kappa\ [\frac{W}{m \cdot K}]$	$C_p\ [\frac{J}{kg \cdot K}]$	$\rho\ [\frac{kg}{m^3}]$
GaAs	45	350	5307
$In_{53}Al_{47}As$	10	370	4430
SiN_x	10	720	3200
Pt	69	134	21450
Au	310	130	19300
Al	10	370	4430

Table 5.8: Thermal properties of materials required for thermal simulations [155].

In semiconductors, the thermal conductivity of the lattice, or thermal resistivity, results essentially from interactions between phonons and the scattering of phonons on crystalline imperfections. While elementary semiconductors with e.g. $\kappa(\mathrm{Si}) \approx 145$ W/mK provide high thermal conductivities, there is a strong reduction for compound semiconductors. On ternary semiconductors like $Al_xGa_{1-x}As$ or $In_xGa_{1-x}As$ in figure 5.24 [156, 157], the thermal conductivity decreases markedly with alloying and exhibits a minimum value of 10 W/mK and 5 W/mK at $x \sim 0.5$, respectively. Due to the high indium content in metamorphic devices and the thick ternary buffer, worse thermal properties are expected compared to the pseudomorphic HEMT devices.

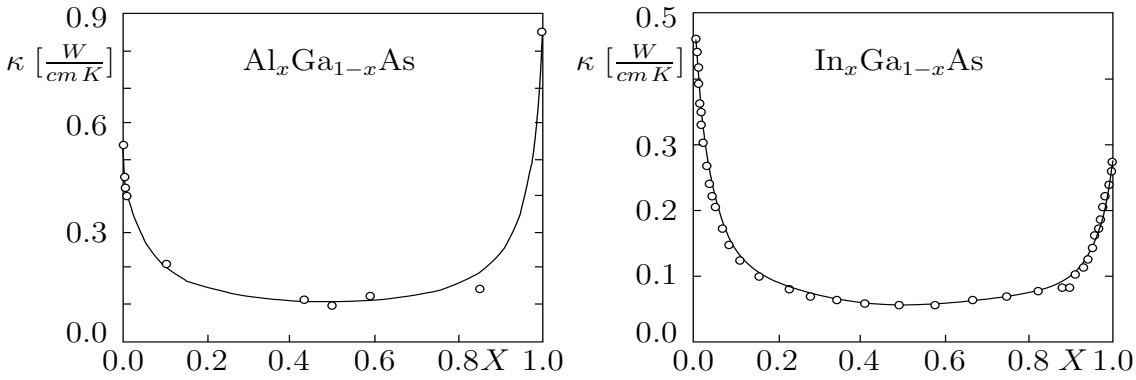


Figure 5.24: Thermal conductivity of $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$ [155, 157, 157].

2D-simulations: Metamorphic versus pseudomorphic

To evaluate the impact of the epitaxy layer sequence for the metamorphic and pseudomorphic power HEMT structures, two dimensional simulations, assuming an infinite expanded gate have been carried out for a power loss of 1 W/mm. Figure 5.25 shows the temperature profile for the pseudomorphic power HEMT.

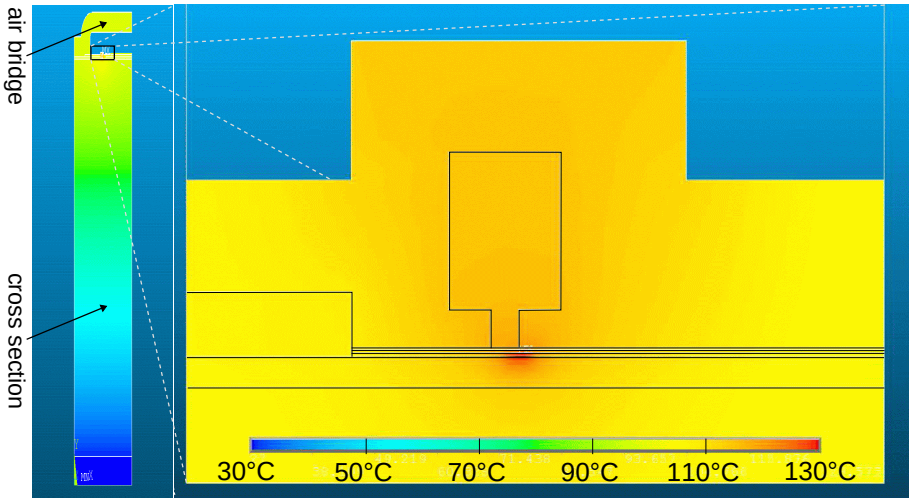


Figure 5.25: Temperature profile through an infinity expanded pseudomorphic HEMT: Cross section (l) and zoom into active area (r).

On the left, the cross section covers a linear heat gradient through the 70 μm thick wafer down to the ideal heat sink fixed at 27 °C. The right part of figure 5.25 shows a zoom of the gate area to identify the maximum temperature of T_{max} = 128.57 °C close to the heat source. The temperature of the ohmic contact is around 30 °C lower than the maximum temperature. For the metamorphic power HEMT, the thermal distribution is very similar to the pseudomorphic HEMT and no extra image is shown here. However, a significantly higher maximum temperature of T_{max} = 147.57 °C is found and confirms the worse thermal properties of the metamorphic power HEMT mainly related to the thick ternary buffer. From the material point of view, there is a clear disadvantage for the metamorphic power HEMT compared to the pseudomorphic power device.

To confirm less self heating during device operation for the pseudomorphic HEMT, the junction temperature of a 1x100 μm test structure has been determined on-wafer by several measurement techniques. Temperature dependent pulsed measurements, for instance, showed too large errors for a reliable temperature calculation. The temperature dependence of the Schottky barrier height might be used to extract the junction temperature of the device in combination with temperature dependent modeling of the IV-characteristics. However, on test device level this method is too expensive. A pragmatic way to determine the junction temperature approximately is to use the temperature dependence of the specific sheet resistance of the gate metalization. The corresponding measurement set-up is sketched in figure 5.26.

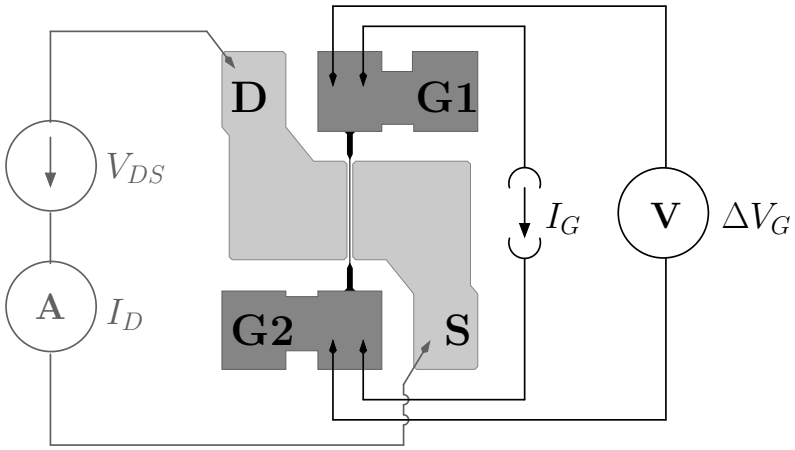


Figure 5.26: Set-up to characterize self heating on a 100 μm test device.

The DC-losses in the active area of the device are adjusted by the drain current and the drain voltage measured for a floating gate potential. Four-terminal sensing has been used to obtain the resistance of the 100 μm gate line between the gate pads G_1 and G_2. On the one hand, the current forced through the gate line has to be high enough to provide a sufficient differential gate voltage ΔV_G. On the other hand, a high current level may contribute to self heating due to power losses in the gate line. Furthermore, a high differential gate voltage causes a strong gradient of the drain current density along the gate which does not represent the standard device operation. For a gate current of 1 mA, the power dissipated in the gate line is below 1 mW/mm and has negligible impact on self heating of the device. The differential gate voltage is in the order of 30 mV. Close to the maximum transconductance, this causes a drain current variation of 22 mA/mm along the gate line. With respect to the mean drain current applied to the device during the characterization, this is an acceptable variation of ± 5 % for the worst case. Due to the different gate technologies and specific gate profiles, a separate calibration of the gate resistance versus the temperature is required for the pHEMT and mHEMT technology. Therefore, the temperature of the non-operated device is varied by a hot plate. The calibration curves shown in the left part of figure 5.27 have been used to calculate the average gate line temperature of the operated device.

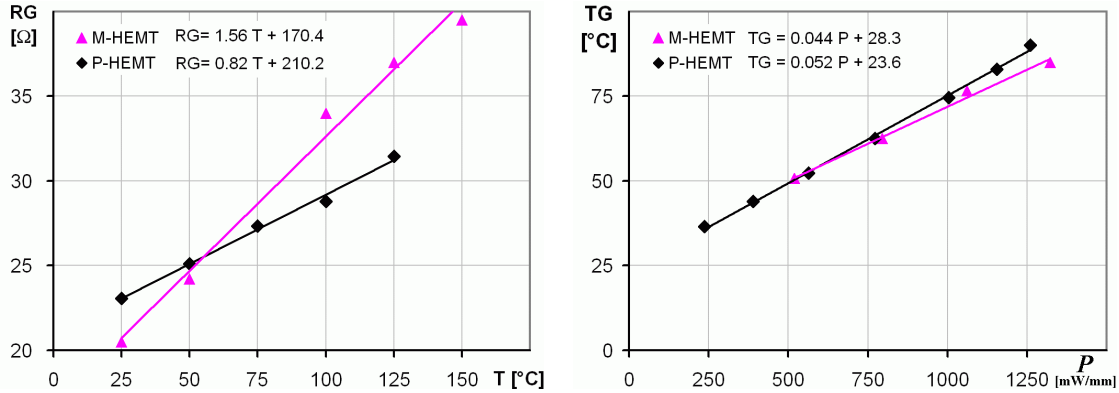


Figure 5.27: Gate resistance as a function of the ambient temperature (l) and self heating due to DC-power losses at 25 °C ambient temperature (r) for a metamorphic and pseudomorphic power HEMT of 1x100 μm.

For both devices, the temperature related to self heating increases with the DC-power loss as shown the right part of figure 5.27. At a power dissipation of 1300 mW/mm, the difference between the metamorphic and the pseudomorphic HEMT is rather small, and the temperature increases by around 65 °C. Likely, the heat generated in the 1x100 μm test device is spread efficiently in the non-thinned wafer independent of the material system.

To identify the different thermal properties of the metamorphic and pseudomorphic technology, the wafers have to be thinned to their target value, and test devices have to be assembled in a temperature controlled package. Furthermore, the accuracy of the junction temperature measurement can be significantly improved by Raman-spectroscopy [158].

3D-simulations: Effect of the device geometry

The infinitely expanded gate assumed for the 2D simulations represents the worst case of a very large device which usually is not representative for W-band applications. Thus, three dimensional models with the largest gate periphery of 8x40 μm have been established for the pseudomorphic power structure to compare thermal properties of the three types of transistor base-cells. To save computing time, symmetry conditions were taken into account, and gate fingers 1-4 also represent fingers 5-8; fingers 1 and 5 are located in the middle of the device and fingers 4 and 8 at the outside. A cross-sectional view of the different four finger base-cells already presented in figure 5.21 is drawn in figure 5.28, to demonstrate the vertical construction of the device. The thickness of the substrate is 70 μm in all cases, and vias are of the same shape and geometry.

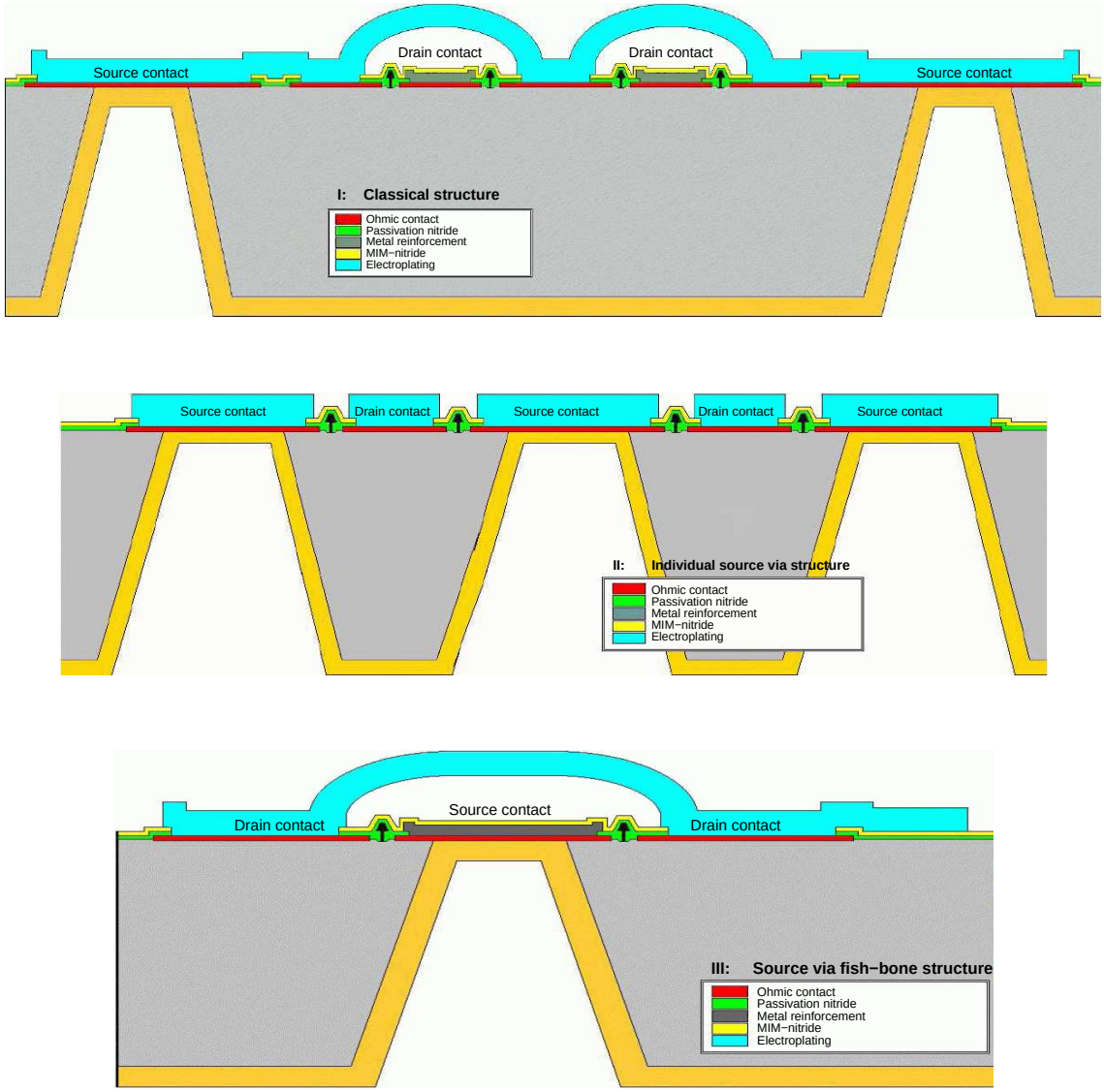


Figure 5.28: Cross-section through a standard-, an individual source-via- and an individual source-via fish bone structure as described below; thermal properties of materials are listed in table 5.8 and figure 5.24.

I) Standard structure: The source pads are connected to the backside metalization by vias for the outer pads and by air bridges for the inner pads. Connections to drain and gate pads are realized by comb-structures.

II) Individual source via structure: All source pads of the device are connected to the backside of the wafer by individual vias reducing the source inductance compared to the standard structure. Gate and drain pads are connected by comb structures.

III) Source vias fish bone structure: The source vias fish bone structure provides a low source inductance and the opportunity for a more compact base-cell design. While gates are still connected by a comb structure, the drain access is realized by air bridges introducing an additional inductance.

The temperature distribution of a standard 8x40 μm device is shown in figure 5.29 for 1 W/mm of dissipated power and ideal assembly on a 27 °C heat sink.

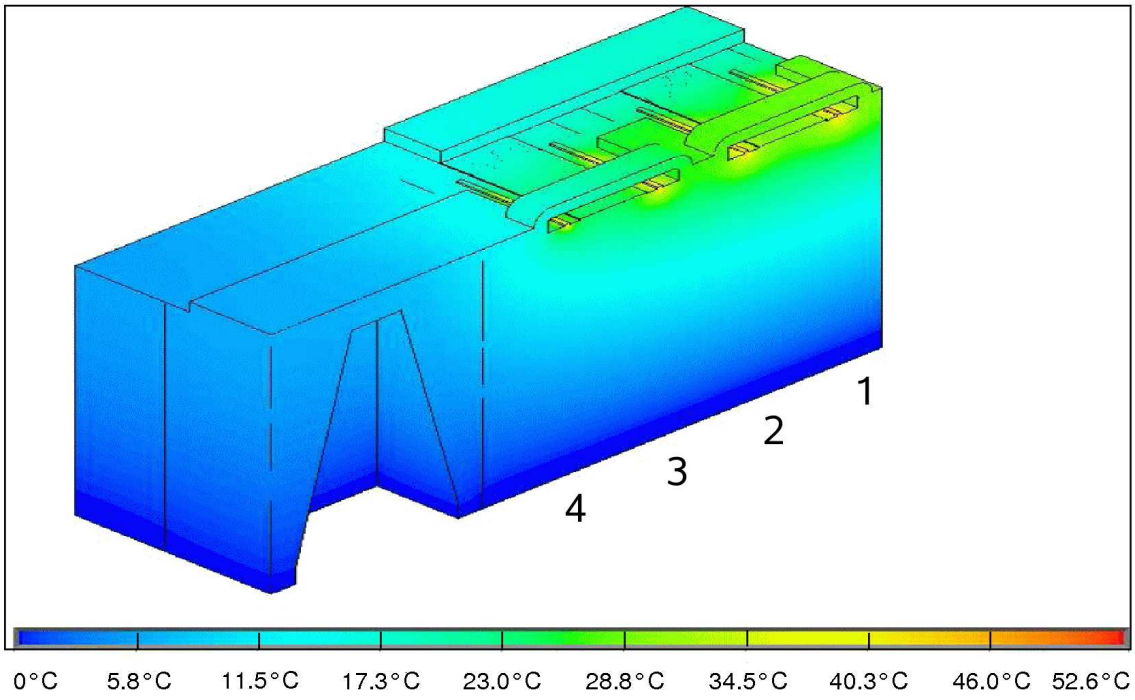


Figure 5.29: Self heating ΔT of an ideally assembled standard 8x40 μm device with respect to a heat sink temperature of 27 °C for a dissipated power of 1 mW/mm.

The increase of temperature ΔT for several positions is given in table 5.9. The maximum temperature increase found below the inner gate finger (1) is 52.6 °C above the heat sink temperature. While temperatures at gate fingers (2) and (3) are slightly lower, there is a significant drop for finger (4) which is partly explained by the large source pad and better lateral heat spreading but also by the presence of the source via.

heat-source in gate finger	1-8	1 and 5	4 and 8
	ΔT [°C]	ΔT [°C]	ΔT [°C]
Finger 1 (5)	52.58	38.17	2.52
Finger 2 (6)	51.47	7.56	3.16
Finger 3 (7)	49.32	4.33	5.16
Finger 4 (8)	43.82	2.77	32.96

Table 5.9: Heating of gate fingers in a standard $8x40\mu$m device.

The device asymmetry remains visible, when heat is generated at the central fingers (1&5) or outer fingers (4&8) alone. Separate feeding of finger pairs results in a temperature increase below 3 °C at the most distant passive gates. Since thermal coupling between the outer positions is even less, it can be neglected. However, it plays an important role between the inner positions due to the symmetry conditions; the temperature of the next neighboring passive gate is significantly increased by 7.6 °C. Since the temperature difference of 5.2 °C between the separately heated outer and central fingers is in the order

of the thermal coupling effects between neighboring fingers, the temperature asymmetry of the standard structure is likely more related to better heat spreading by the large outer source pads than to the via.
A higher uniformity compared to the standard structure is provided by the individual source structure, since all source pads are of the same shape and size. Together with enlarged source pads, the maximum temperatures may be lowered efficiently even for the inner fingers, resulting in a better thermal symmetry for the individual source structure. The thermal distribution of ΔT with respect to a heat sink temperature of 27 °C is shown in figure 5.30.

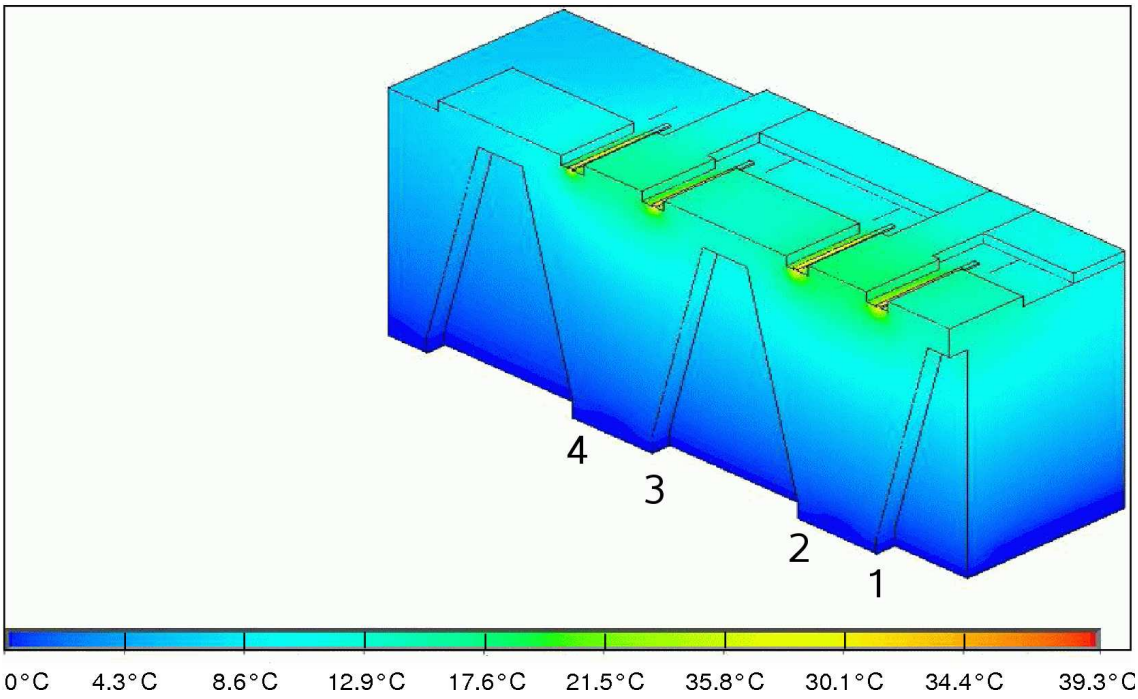


Figure 5.30: Self heating ΔT of an ideally assembled 8x40 μm individual source via device with respect to a heat sink temperature of 27 °C for a dissipated power of 1 mW/mm.

The maximum temperatures for each finger are given in table 5.10. The inner finger (1) shows the highes temperature increase of 39.34 °C which is more than 13 °C below that of the standard structure. Furthermore, the thermal gradient to finger (4) is much less pronounced and the small difference of 3.2 °C is related to less thermal coupling towards the outer fingers.

heat-source in gate finger	1-8	4 and 8	2 and 7
	ΔT [°C]	ΔT [°C]	ΔT [°C]
Finger 1 (5)	39.34	1.04	1.81
Finger 2 (6)	39.06	1.49	3.02
Finger 3 (7)	38.23	3.67	29.79
Finger 4 (8)	36.14	30.06	3.67

Table 5.10: Heating of gate fingers in a 8x40 μm individual source via device.

Feeding the finger pairs separately like the outer fingers (4&8) or the next inner fingers (2&7) shows nearly the same result for the maximum temperatures and confirms the high thermal symmetry of the individual source structure. On small device topologies, the individual source vias help to reduce temperatures in the order of 10-20 %. However cooling is much less pronounced, if the gate width exceeds the dimension of the via significantly like on power devices designed for much lower frequencies.

The fish bone structure may benefit from the individual source via. Yet, the air bridges used for the drain access and the more compact design may affect the temperature negatively. The thermal profile of the fish bone structure is given in figure 5.31 for a dissipated power of 1 W/mm and a heat sink temperature of 27 °C.

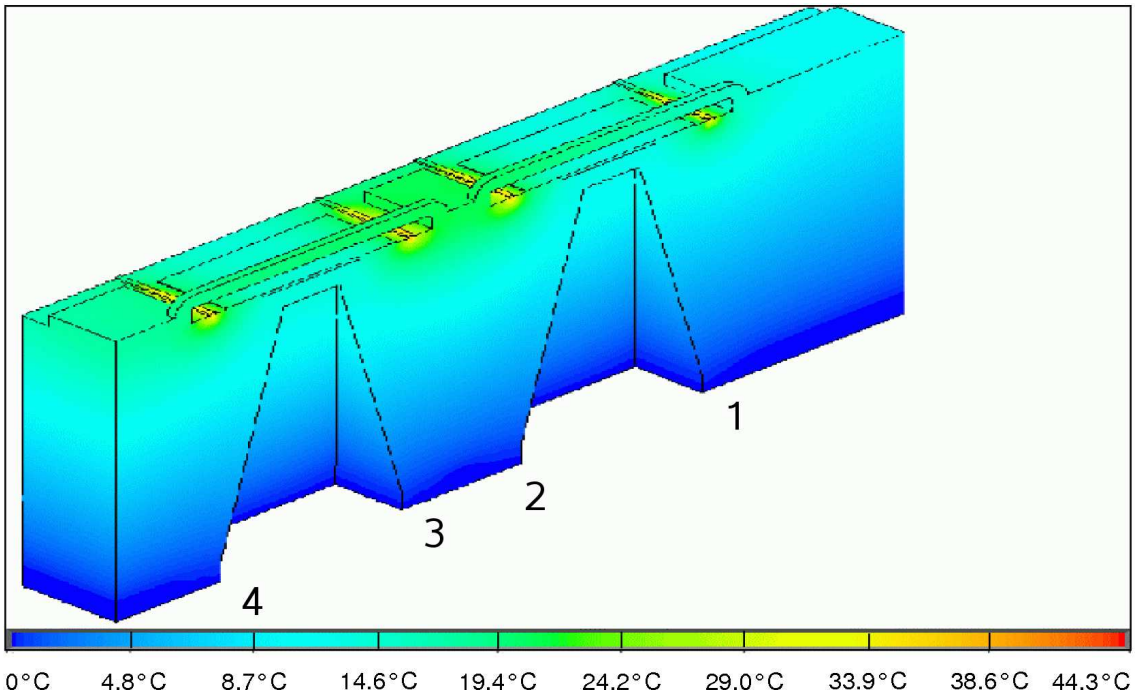


Figure 5.31: Self heating ΔT of an ideally assembled 8x40 μm source via fish bone device with respect to a heat sink temperature of 27 °C for a dissipated power of 1 mW/mm.

In table 5.11, the maximum temperature increase of 44.34 °C is found below gate finger (3). With a temperature range of 3.71 °C, the thermal uniformity of the fish bone structure is slightly worse compared to the individual source via structure.

heat-source in gate finger	1-8	1 and 5
	ΔT [°C]	ΔT [°C]
Finger 1 (5)	40.65	34.58
Finger 2 (6)	43.98	3.25
Finger 3 (7)	44.36	1.85
Finger 4 (8)	43.06	0.95

Table 5.11: Heating of gate fingers in a $8x40\mu$m source via fish bone device.

Thermal coupling between neighboring fingers (1-4) is low thanks to the individual source vias and enlarged source pads. However, the overall higher temperature indicates stronger coupling with the mirror fingers (5-8). Based on the maximum temperature increase ΔT, the equivalent thermal resistance $R_{th} = \Delta T / P_d$ can be calculated with the dissipated power P_d for each 8x40 μm structure. The highest equivalent thermal resistance of 164 K/W is found for the standard structure, followed by the fish bone structure with $R_{th} = 138$ K/W. The best thermal properties were simulated for the individual source via structure with an equivalent thermal resistance of $R_{th} = 123$ K/W for the 8x40 μm pseudomorphic HEMT device. Since ΔT from simulations is low, the RF-output power of the device is expected to be limited by the breakdown voltage and not by the power loss dissipation. However, simulations assume an ideal device assembly and heat sink, and temperatures of the operated device might be significantly higher. This is especially true for the on-wafer characterization of circuits on thinned wafers having a poor thermal contact to the chuck of the measurement set-up.

6 W-band demonstration amplifiers

After a short summary on wafer fabrication and yield, results from low noise and power amplifiers fabricated with the metamorphic low-noise technology and the pseudomorphic power technology are presented in this chapter.

6.1 Demonstrator fabrication

To conclude on the fabrication of the metamorphic and pseudomorphic HEMTs, two cake diagrams based on 27 and 48 wafers are depicted in figure 6.1 representing the percentage of successful wafer fabrication and failures. Only a quarter of all started metamorphic low-noise wafers have been finished successfully. Due to the thin barrier thickness and mesa-isolation, the main failure reason has been direct channel contacting at the mesa edge causing high leakage currents and a low device breakdown. The poor device passivation is linked to the 3-layer resist gate technology where insufficient removal of adhesion promoter prevented proper coverage of the semiconductor surface. The weakness of the 3-layer resist gate technology is related to the small gate length close to the theoretical limit; process fluctuations rapidly result in a not properly defined foot resist opening and irregular gate recess. To improve the metamorphic technology to a production worthy level, alternatives to mesa-isolation and the presented 3-layer resist gate technology are needed. Direct application of the pHEMT processing failed due to insufficient device isolation and plasma damage. However, implantation techniques based on combinations of oxygen, argon and boron as well as low damage nitride stripping may result in yield improvement.

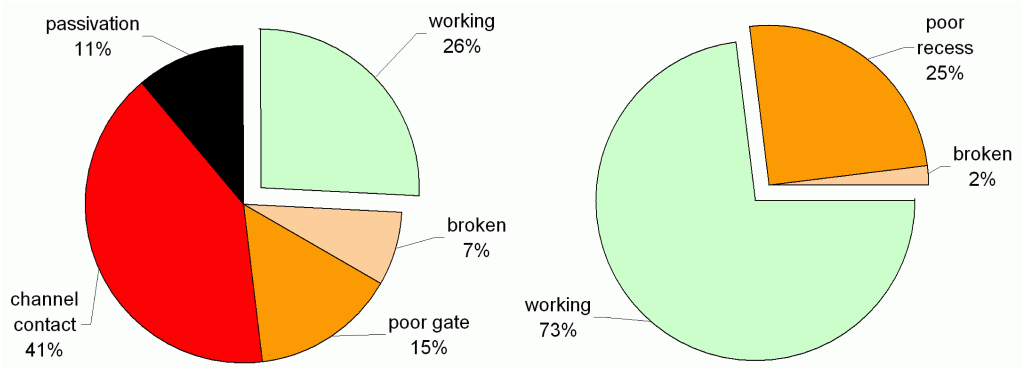


Figure 6.1: Wafer status after the end of fabrication for the metamorphic low-noise technology (l) and pseudomorphic power technology (r).

In contrast to the metamorphic low-noise technology, the pseudomorphic HEMT technology showed more than 70 % of working devices. Only 25 % of all fabricated wafers failed due to the gate recess fabrication step. Although, the gate recess of the pseudomorphic HEMT is the most sensitive step during the whole device fabrication, the etch solution itself did not initiate these failures; a clear relation to a small change in the rinse-drying

process after gate recessing had been identified to cause the problems. After remediation, the short gate length pHEMT technology developed in this work fulfills high yield production level requirements.

6.2 Metamorphic HEMT low noise amplifiers

Several metamorphic W-band low noise amplifier designs have been realized by A. Bessemoulin, member of the UMS-Orsay design department. Designs are based on common source and cascode configurations discussed in the annex on page 164. The small signal RF-characteristics and noise figures of the demonstrator circuits are presented in the following part as well as a brief view on MMIC-yield aspects.

6.2.1 Common source design

Several two- and three-stage LNAs have been fabricated for low-noise W-band applications. The two-stage common source version in figure 6.2 is based on 2x20 μm devices. It provides more than 10 dB of gain between 75 to 106 GHz when biased at 1.5 V and 15 mA. Simulations at 94 GHz result in a gain of 10 dB and a noise figure of 4.1 dB which are in good agreement with the measurement showing a gain of 12 dB and 4.5 dB of noise figure. From 83 to 105 GHz, the mean noise figure is below 5 dB.

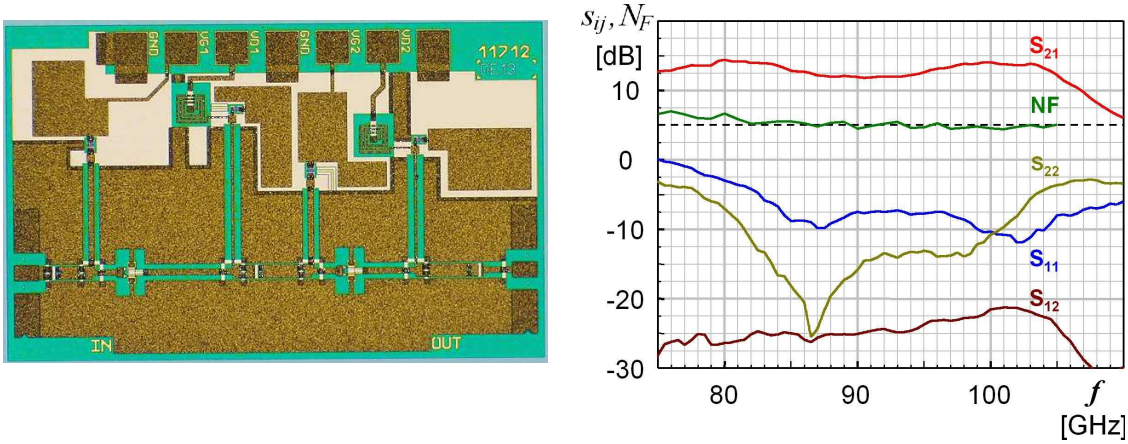


Figure 6.2: Top view and noise performance of a two-stage metamorphic common source low noise amplifier (1.75x1)mm^2. Small signal characterization at UMS, Orsay, France; noise measurement at IAF, Freiburg, Germany.

The three-stage common source version in figure 6.3 is also based on the 2x20 μm transistor cell. It provides more than 17 dB of gain from 75 to 100 GHz when biased at 1.5 V and 30 mA. The simulation (gain = 17 dB, N_F = 4.8 dB at 94 GHz) is in good agreement with the measured results of 19.1 dB for the gain and a noise figure of 4.4 dB. A mean noise figure of 5 dB is found between 81 GHz and 101 GHz.

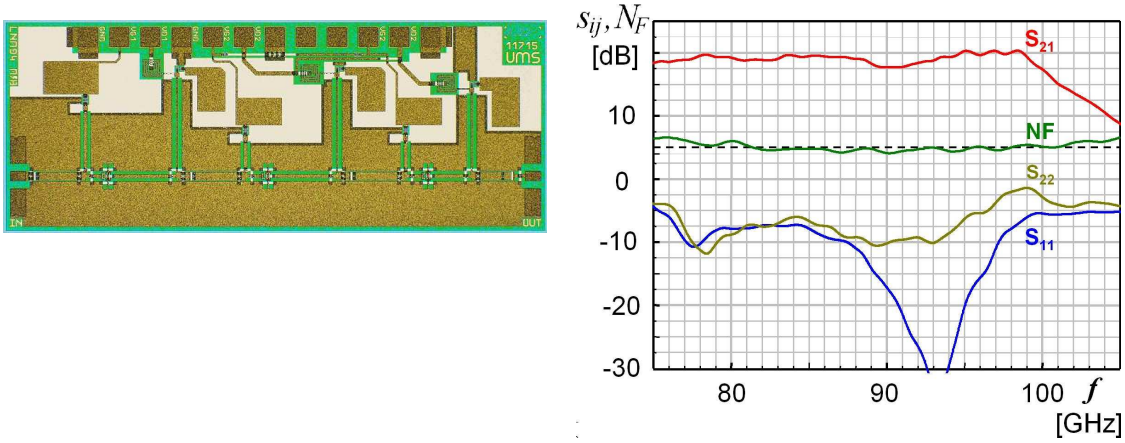


Figure 6.3: Top view and noise performance of a three-stage metamorphic common source low noise amplifier (2x1)mm^2. Small signal characterization at UMS, Orsay, France; noise measurement at IAF, Freiburg, Germany.

Both common source low noise amplifiers have a large band width of 20 GHz and provide a mean gain of 6 dB per stage with noise figures around 5 dB. Above 100 GHz there is a steep drop in RF-performance related to the common source design as discussed in the annex on page 164. With a gate length of 120 nm, the LNA-performance fits well with literature [159] data. Typical requirements for the LNA of a passive radar imaging system [123] are given in table 6.1:

	min	typical	max	measurement
frequency [GHz]	91	94	97	94
gain [dB]	8 (13)	10 (15)		12 (19)
flatness [dB]		$\pm$1 (1.5)		$\pm$ 0.8 (0.9)
noise figure [dB]		3.8	4	4.1 (4.3)
power dissipation [mW]		12 (20)	25 (40)	22.5 (45)

Table 6.1: Requirements for a two- (three-) stage LNA suited for passive radar imaging applications and obtained values from two representative demonstrators [123].

At 94 GHz, the measurement results of the metamorphic two and three-stage low noise amplifiers are close to the requirements. While the noise figure and power consumption are slightly above the target, the gain and its flatness are better than required. In the first iteration, the low noise amplifiers fabricated with the metamorphic low noise technology developed in this work demonstrate promising RF-gain and RF-noise performance.

6.2.2 Cascode design

To improve the RF-performance and to target for higher frequencies, several cascode demonstrators have been fabricated with the metamorphic low-noise technology. The top view of a single-stage cascode LNA and its RF-performance are shown in figure 6.4. Biased at 2 V and 15 mA, the amplifier provides 5 dB of gain over a wide frequency range from 76 to 120 GHz. A gain of 7 dB is obtained between 96 and 120 GHz. The minimum

noise figure of 3.8 dB is reached at the upper characterization limit of 105 GHz with a gain of 7.8 dB.

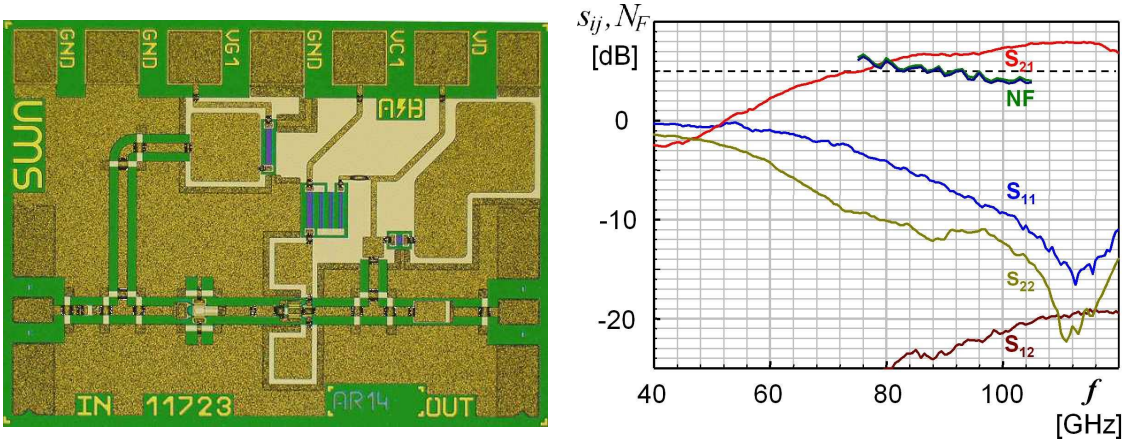


Figure 6.4: Top view and noise performance of the single-stage cascode metamorphic low noise amplifier (size)mm^2. Small signal characterization at UMS, Orsay, France; noise measurement at IAF, Freiburg, Germany.

The RF-performances of the two and three-stage cascode amplifiers are shown in figure 6.5. Similar to the single-stage design, operation is expanded to higher frequencies. The two-stage version provides 10 dB of gain over the whole frequency band from 75 to 120 GHz. A gain of 15 dB is obtained between 97 and 116 GHz. The minimum noise figure continues to decrease until the upper limit of the noise test bench with a value of 4.4 dB at 105 GHz and a gain of 15.8 dB.

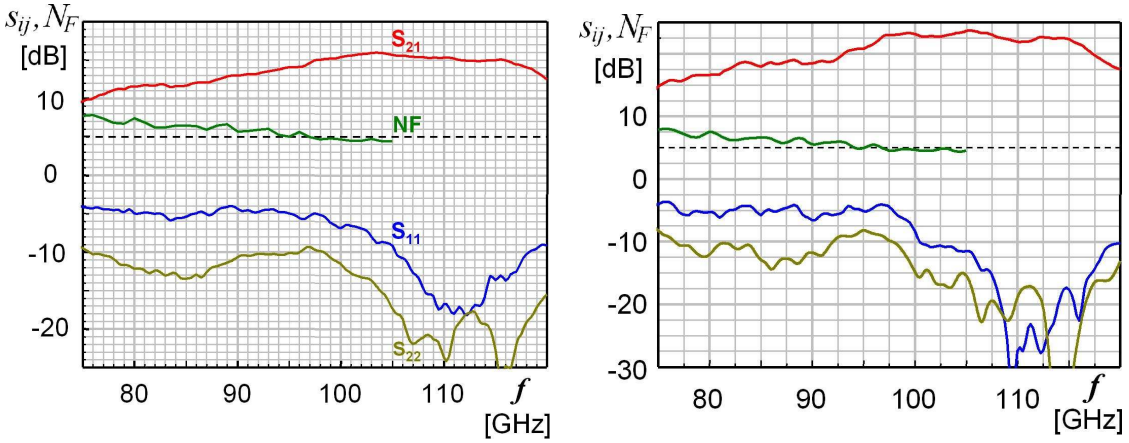


Figure 6.5: Noise performance of the two-stage (l) and three-stage (r) cascode metamorphic low noise amplifier (2x1)mm^2 and (2.5x1)mm^2. Small signal characterization at UMS, Orsay, France; noise measurement at IAF, Freiburg, Germany.

The three-stage cascode amplifier offers 15 dB of gain over the whole frequency range from 75 to 120 GHz and 20 dB from 93-117 GHz. Like for the single and two-stage versions, the minimum noise figure of 4.5 dB is found at 105 GHz with an associated gain of 23 dB. Compared to the common source designs, the cascode amplifiers provide around 2 dB more gain per stage. The minimum noise figure is below 4.5 dB at 105 GHz and

could not be determined exactly due to the frequency limitation of the test bench. The metamorphic low-noise technology with a gate length of 120 nm demonstrates an excellent RF-gain and low noise performance as required for low noise amplifiers in passive W-band radar imaging systems [3, 160, 21].

6.2.3 Yield of the metamorphic LNAs

Most of the 15 W-band LNA-versions had a high chip-yield in the order of 85 %. On one type of a two-stage common source LNA, however, around the half of the chips failed due to high leakage currents as shown in the small signal gain in figure 6.6. Since the appearance of the malfunction is not related to the total gate periphery within the circuit, the gate module, especially the critical part at the edge of the mesa can be excluded.

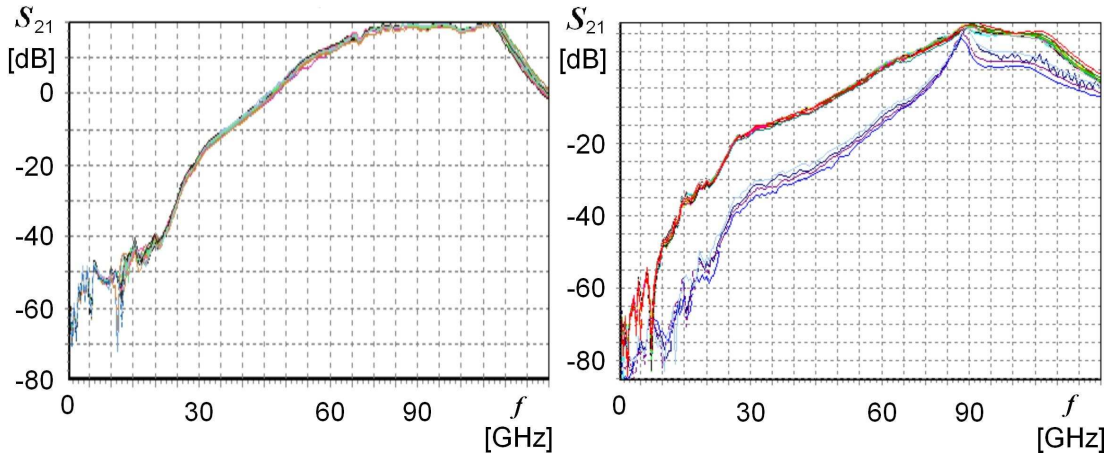


Figure 6.6: High MMIC functionality on most LNAs like the common source three-stage version (l) but poor yield on one type of a two-stage common source LNA (r). Small signal characterization at UMS, Orsay, France.

A four-stage V-band design which was designated for chip scale surface mount assembly [161] is shown in figure 6.7. In contrast to the coplanar W-band demonstrators, a micro strip design is used including individual source vias and hot vias.

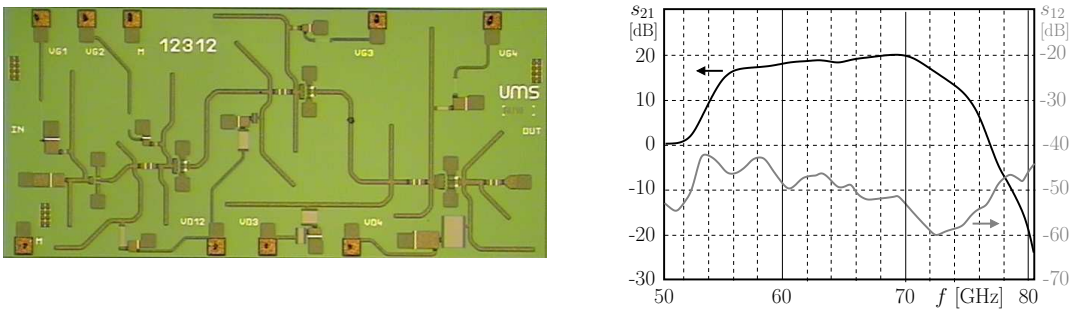


Figure 6.7: Four-stage V-band LNA fabricated with the metamorphic low-noise technology.

All DC- and RF-signals are supplied from the backside of the chip. Furthermore, the front side of the wafer is additionally protected by a thick high isolating BCB layer to

improve the handling properties during chip assembly. While the characterization of the test devices, showed a high degree of functionality at the end of fabrication, most of the demonstrator LNAs fail due to a high gate leakage in the first stage. Reverse engineering of an affected chip by removal of all passivation layers and the gate metalization shows the typical defect. The SEM-image in figure 6.8 identifies burn out at one finger of the first stage. An EDX-analysis has been carried out to identify the defect types as shown in the spectra in the right part of figure 6.8. Close to the ohmic contact, the semiconductor was attacked during the gate metal removal. The defects marked with spectrum 2 consist on arsenic oxides. Although As may act like a metal film causing a short, this defect does not explain the malfunction of the device since it was formed by the preparation of the sample. The gate recess is straight and smooth, however, it is interrupted by the defect linked with spectrum 1.

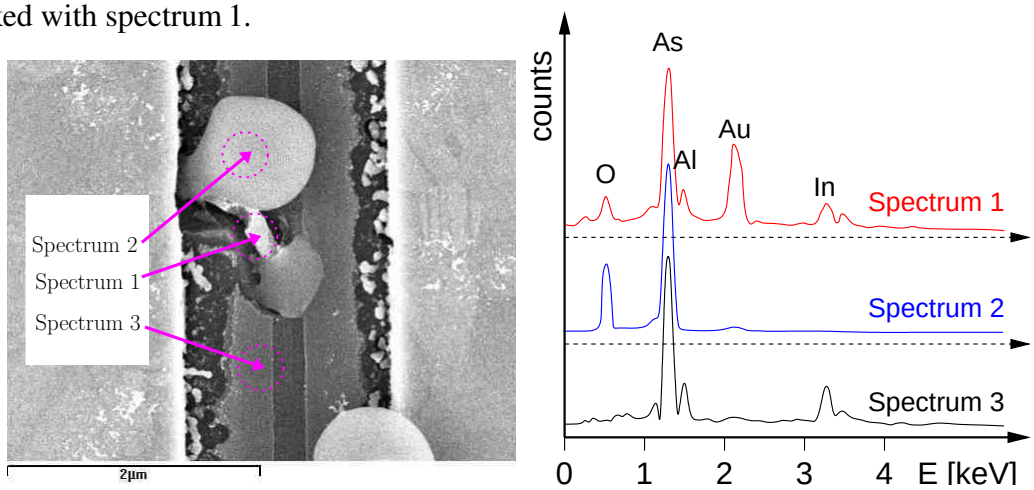


Figure 6.8: Sites (l) and EDX-spectrum (r) of a 4x20 μm device from a defective first stage of the V-band LNA.

The presence of gold in spectrum 1 indicates that a micro burn out occurred during the LNA-characterization without melting the ohmic contacts as typically observed for a real overload of the device input. The high yield of the test devices with the same topology indicates a failure mechanism occurring during the wafer fabrication which is related to the MMIC-design. While the fabrication of individual source via devices has been successfully demonstrated on pseudomorphic HEMTs [161], the metamorphic samples fail likely due to a more pronounced sensitivity towards electrostatic discharge. Especially during BCB-structuring and via hole etching, the RF-power of the ICP-etching tools can induce high electrical fields locally on the circuit due to antenna effects on the waveguide structures. In the worst case, a local, low energetic burn out may occur at a particular transistor or capacitor causing leakage currents without visible destruction of the device.

6.3 Pseudomorphic HEMT low noise amplifier

A W-band low noise amplifier, has been fabricated also with the pseudomorphic HEMT technology. In contrast to the metamorphic variety of demonstrators, merely one two-stage common source LNA has been designed and characterized [12] to evaluate the low-noise capabilities of the power technology. An image of the LNA and its RF-properties are shown in figure 6.9.

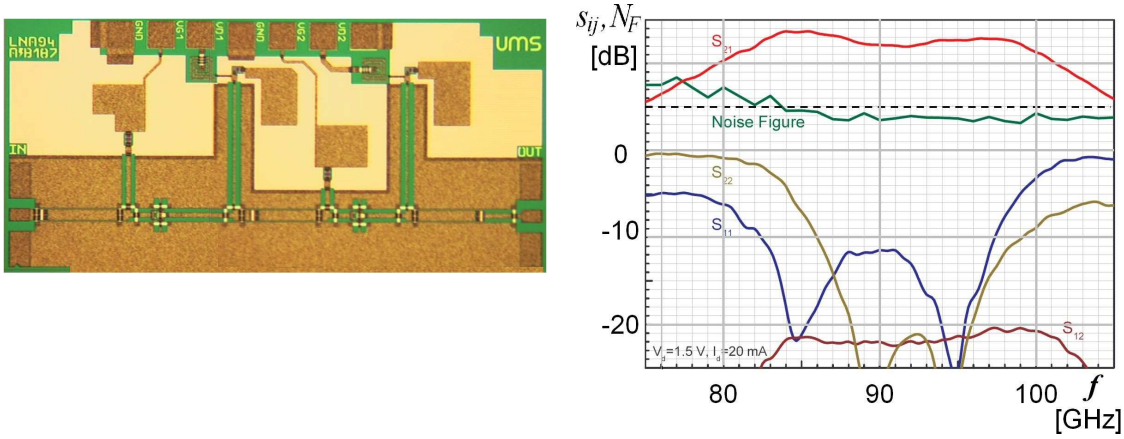


Figure 6.9: Top view (l) and small signal performance (r) of a two-stage pseudomorphic PPH10 low-noise amplifier suited for a passive radar imaging system working at 94 GHz. Small signal characterization at UMS, Orsay, France; noise measurement at IAF, Freiburg, Germany.

With a gate length of 100 nm, the pseudomorphic two-stage LNA provides more than 10 dB of gain from 80 to 101 GHz and a noise figure below 5 dB from 83 to 105 GHz. At 94 GHz, the noise figure is 3.7 dB with an associated gain of 12.8 dB. The minimum noise figure of 3.1 dB is obtained at 99 GHz with a gain of 10.3 dB.

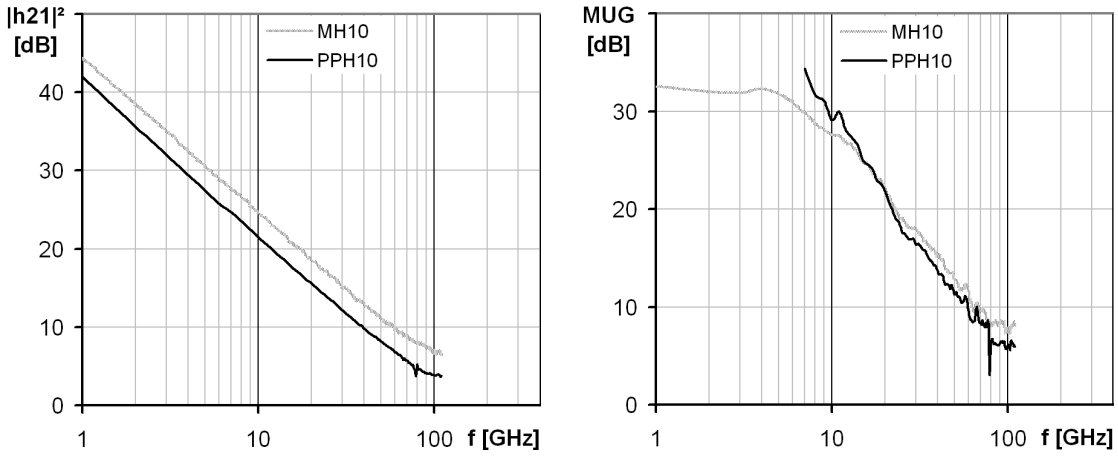


Figure 6.10: Comparison of the small signal RF-performance of a 2x30 μm pseudomorphic (black) and metamorphic (grey) device, normalized to a 50 Ω reference plane.

This excellent result for the pseudomorphic HEMT low noise amplifier can be explained by a direct comparison of the small signal RF-performance between the metamorphic and pseudomorphic HEMT technology as shown in figure 6.10. The comparison is based on the same transistor cell of 2x30 μm and maximum gain biasing at $V_{DS} = 1$ V. The metamorphic device clearly benefits from its high indium content regarding the current gain $|h21|^2$ and reaches a higher transit frequency f_T. Concerning the maximum unilateral gain MUG, however, the difference is significantly lower, and the associated gain for low-noise matching might become similar. The low-noise performance of the power pHEMT technology between 80 and 100 GHz is even better than for the metamorphic demonstrators presented in this work and compares well to the best results achieved with

noise-optimized InP-HEMTs [162] or metamorphic HEMTs [159], respectively. With a limited gate length of 120 nm for the metamorphic low-noise technology in this work, the pseudomorphic HEMT is the more promising candidate for W-band low-noise applications. Besides the higher fabrication yield, the pHEMT is less sensitive regarding electrostatic discharge during wafer processing and thermal stress, and is highly compatible with existing pHEMT production steps.

6.4 Power amplifiers

As a result of small signal characterizations, electromagnetic field and thermal simulations the individual source via device with a symmetric gate configuration has been selected to design the power amplifier demonstrators. Non-linear modeling of these devices has been performed and several HPA-versions have been designed by T. Huet, member of the UMS-Orsay design department. The characterization results are presented within this section.

6.4.1 Large signal model

In contrast to the small signal model, the input and feedback capacitances c_{gs} and c_{gd} values are not fixed under large signal operation. An empirical non-linear large signal model according to "Yusuke Tajima" [163] is shown in figure 6.11.

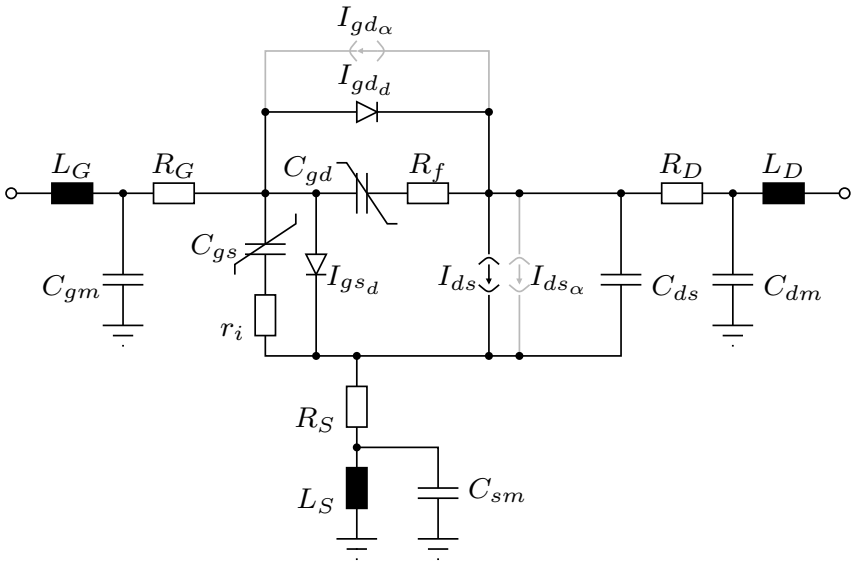


Figure 6.11: "Tajima" [163] large signal model for the individual source pseudomorphic HEMT.

The input and feedback capacitances depend on the operation voltage; gate leakage is related to a non-ideal Schottky diode. Impact ionization is described by additional diodes and current sources. To quantify impact ionization, an extensive pulse characterization has to be carried out on the device. For simplification, impact ionization has not been implemented in the model, although observed at high drain voltage operation. Since the target for the demonstrators is to deliver power disregarding linearity properties, the

voltage dependence is only realized for the dominating input capacitance c_{gs}; for highly linear applications, the voltage dependence of the feedback capacitance c_{gd} has to be characterized precisely and considered in the non-linear model. Elements of the non-linear model are summarized in the annex on page 163.

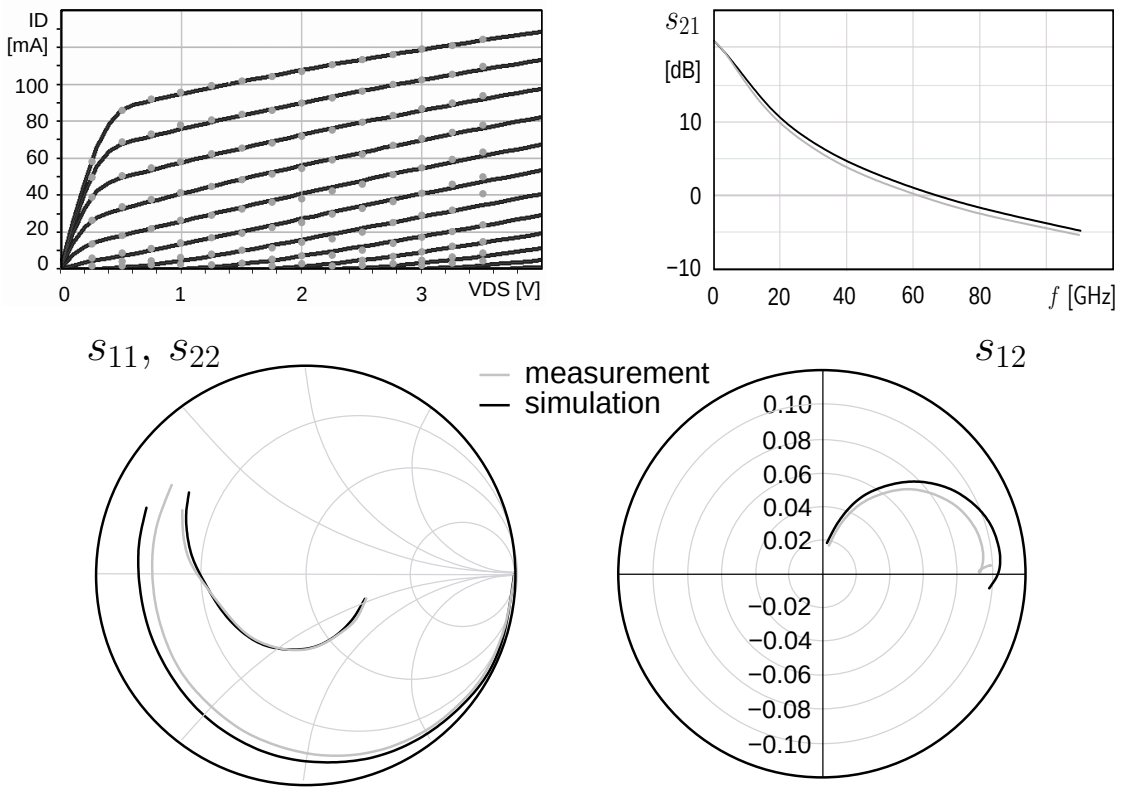


Figure 6.12: Simulated drain current and small signal parameters of a pseudomorphic 6x40 μm individual source via device operated at V_{DS} = 3 V and V_{GS} = -0.1 V and I_D of 300 mA/mm.

The modified Tajima model has been implemented in the electronic design simulation software ADS. The simulated output characteristic of a 6x40 μm device operated at V_{DS} = 3 V, V_{GS} = -0.1 V and I_D of 300 mA/mm is in good agreement with the measurement in figure 6.12. Similar for the small signal gain s_{21}, the input s_{11} and output s_{22} reflection coefficients and reverse isolation s_{12}.

6.4.2 Pseudomorphic power pHEMT amplifiers

Several power amplifiers have been designed and fabricated to provide 100 mW of output power at 94 GHz and 10 dB of power gain. To meet the gain requirements, a three-stage structure has been selected. Based on non-linear simulations, 4x40 μm base-cells are chosen for all three amplifier stages. Especially at the output stage, the combination of two four finger devices promises a higher output power of 18.7 dBm compared to 17.8 dBm provided by a 6x40 μm device. However, the better power performance of the small base-cell might be compensated by combining losses, calculated to -0.8 dB at 94 GHz. Two power amplifier demonstrators are depicted in figure 6.13. Both demonstrators show a very similar structure; for improved power gain, the biasing networks of the right version

have no resistive parts within the current supply. The amplifiers consist of 4x30 μm base-cells with the symmetric gate configuration for the first and second stage and 4x40 μm for the output stage. Only the first stage is matched for maximum gain and divides the signal in two pathes. Devices of the second stage are matched for power as well as the output stage. Connections between the stages are realized by couplers with a typical loss between 0.5 and 0.8 dB. At 1 dB-compression, an output power of 21 dBm, a gain of 13.5 dB and a power added efficiency of 7.5 % is calculated for operation at $V_{DS} = 3.5$ V.

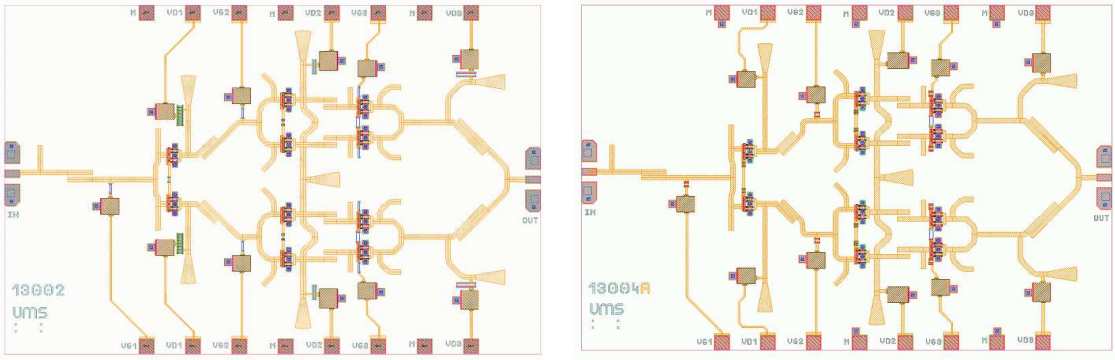


Figure 6.13: Layouts of the two W-band power amplifier versions of (2.3x3.5)mm^2 size.

The small signal performance has been characterized on-wafer from 75 to 110 GHz. Gain and reflection coefficients given in figures 6.14 and 6.15 are obtained from several devices and wafers. A comparison between simulation and measurement of the first demonstrator on the left shows around 1 dB less measured gain. The lower gain is explained by self-heating of the circuit during cw-measurement and the poor thermal contact of the wafer to the chuck of the test bench. While the bandwidth of 10 GHz is in good agreement with the simulation, the center frequency is shifted by 2 GHz to 96 GHz. In fact, the frequency response strongly depends on the passive structures such as lines, and small deviations at W-band can be easily explained by fabrication tolerances.

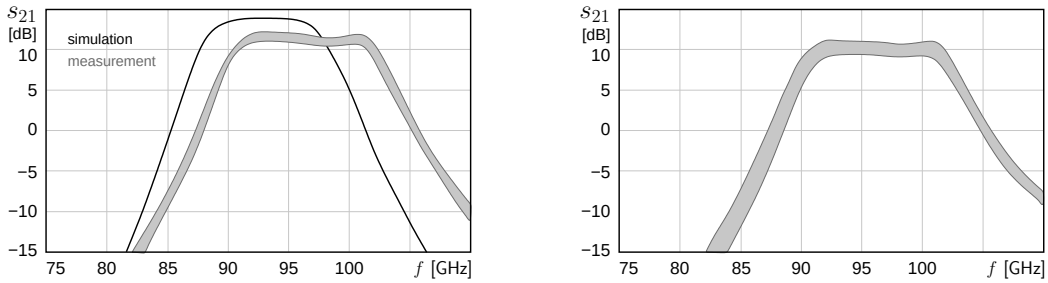


Figure 6.14: Simulated and measured small signal gain of the two HPA-versions; spreads from several MMICs are indicated by grey shadings. Simulation and measurement were performed at UMS, Orsay, France.

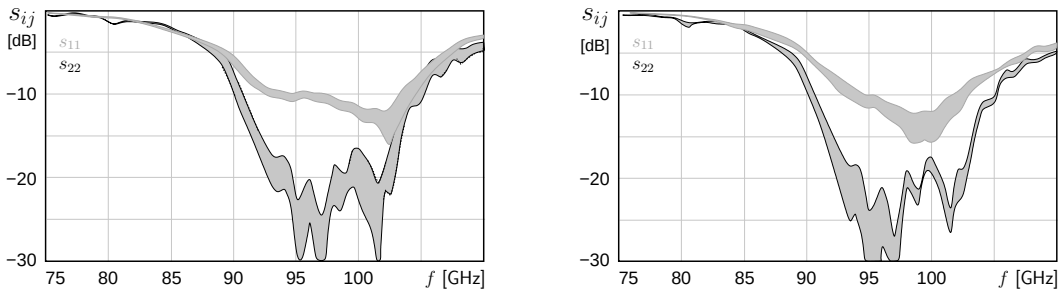


Figure 6.15: Simulated and measured input and output matching of the two HPA-versions; spreads from several MMICs are indicated by grey shadings. Simulation and measurement were performed at UMS, Orsay, France.

The small signal gain of the first demonstrator is around 11 dB from 92 to 102 GHz with a good flatness over the frequency range. The input reflection s_{11} is below -10 dB, the output reflection s_{22} around -20 dB. Spreads indicated by grey shaded areas are considerably small. Against the expectation, the small signal gain of around 10 dB from 92 to 102 GHz is slightly lower for the second demonstrator. The input and output matching is comparable to the first HPA version.

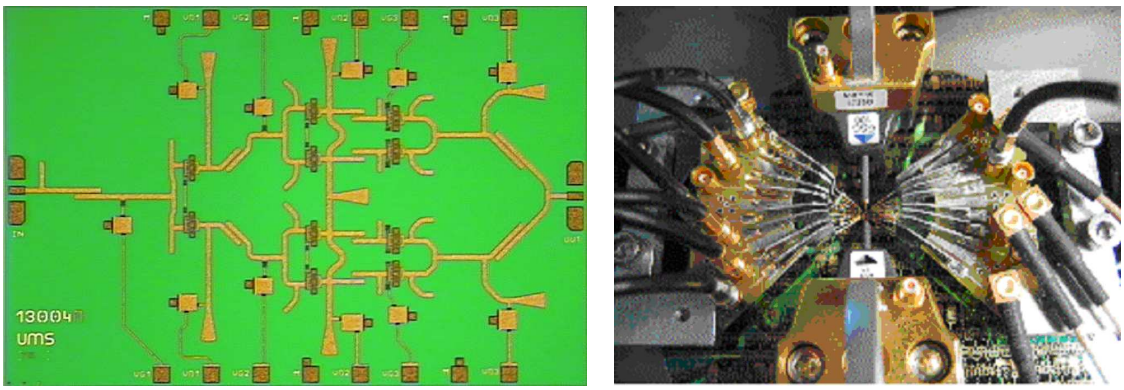


Figure 6.16: Top view on a HPA-demonstrator (l) contacted by probe cards for power characterization at 94 GHz (r).

The power performance of the demonstrators has been characterized at IEMN (Lille, France) at 94 GHz. A picture of a demonstrator and the probe-card of the power measurement setup are shown in figure 6.16. DC-pads of the MMIC for drain and gate supply are connected by 8-needle probes from the left and right. RF-connections are realized by GSG-probes from the top and the bottom. Resistors and capacitors on the probe card suppress oscillations of the circuit during power measurements. The output power at 94 GHz, the power gain and the power added efficiency of the two demonstrator versions are shown in figure 6.17 and 6.18 for a supply voltage of V_{DS} = 3.5 V and V_{GS} = -0.1 V. The power gain of the first version is 10 dB. The maximum output power is 20.8 dB with a power added efficiency of 7.6 %. Apart from the lower gain already observed during small signal characterizations, the measurement results are close to the simulation.

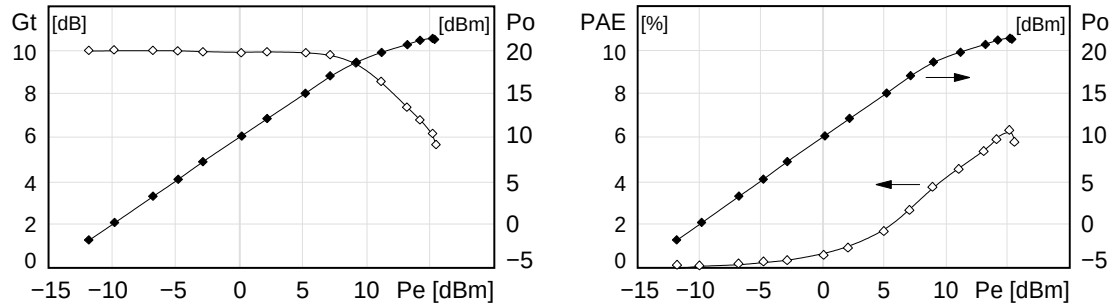


Figure 6.17: Power performance of HPA-version 1 at 94 GHz. Data from IEMN, Lille, France.

The second demonstrator version offers a linear power gain of 11 dB at 94 GHz, a maximum output power of 22.3 dBm and a power added efficiency of 8.7 %. Against the small signal characterization, a higher gain can be confirmed for the second demonstrator version without resistive parts in the biasing networks. The best results are obtained from this version biased at V_{DS} = 3.5 V and V_{GS} = -0.1 V. The maximum output power of 22.7 dBm is equivalent to a power density of 290 mW/mm in the third stage devices, neglecting combining losses. At 1 dB-compression the output power reduces to 130 mW. The highest PAE of 10.6 % is found for a reduced supply voltage of V_{DS} = 3 V with a maximum output power of 151 mW.

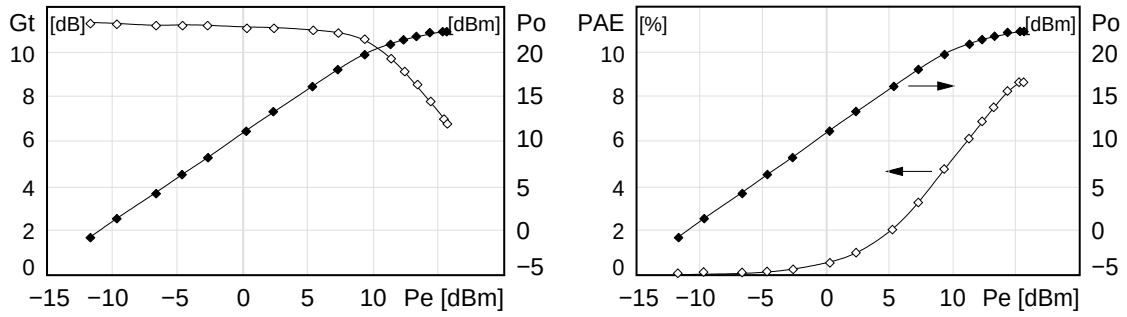


Figure 6.18: Power performance of HPA-version 2 at 94 GHz. Data from IEMN, Lille, France.

The power densities in the output stages are much less compared to values observed on device level. This is partly due to the larger base-cell topology and combination of the devices within the circuit causing non-optimum device matching and phase relation between inner stages. Furthermore, the absolute power losses are significantly higher for the HPA having 1.36 mm overall gate width compared to the small 2x30 μm test device. In combination with a poor thermal contact between the backside of the thinned wafer and the chuck of the measurement set-up, the real temperature of the circuit devices may significantly exceed the simulation result of 82 °C which relies on an ideal chip assembly on a 25 °C heat sink. To confirm the thermal aspects, chips either have to be characterized in pulsed conditions which were not available at 94 GHz or have to be assembled in packages which provide a good thermal management. Nevertheless, the pseudomorphic power technology demonstrates promising power performances at W-band on device and MMIC-level, surpassing that of the metamorphic approach [150, 164] and performances obtained on InP substrates [165, 166].

7 Conclusion

Pseudomorphic and metamorphic HEMT technologies compatible to the UMS 4" production facility have been developed to provide components for industrial W-band applications. Small signal, noise and non-linear device modeling has been performed to support LNA and HPA demonstrator design. Thermal aspects, relevant for power devices have been evaluated on base-cell level by finite element simulations. Low noise amplifiers were fabricated using the metamorphic low noise- and pseudomorphic HEMT technology. The metamorphic LNA demonstrated a good RF-noise performance at 94 GHz which complies with the requirements for passive radar imaging systems [123]. Although not optimized for low-noise, the pseudomorphic HEMT low noise amplifier offers the same performance. State-of-the-art RF-power performance at 94 GHz has been demonstrated on device level for pseudomorphic and metamorphic power technologies. Although a higher off-state breakdown was realized for the metamorphic power device, the maximum operation voltage and RF-power density is higher for the pseudomorphic technology. Thus, power amplifiers have been designed for the pseudomorphic HEMT technology. Promising power performance has been demonstrated by several HPA-designs suited for 94 GHz active radar imaging systems.

Technology

To optimize for low-noise and power requirements, bandgap engineering has been performed for the metamorphic $In_xGa_{1-x}As$ channel structure. Due to the high indium concentration, most fabrication modules from pHEMT production are incompatible with the metamorphic epitaxy and had to be reinvestigated. Device isolation for instance has to be performed by mesa and side wall etching. Ohmic contacts have to be annealed at low temperatures implying a strong sensitivity concerning further thermal budgets; nevertheless, a reasonable thermal stability has been proven on metamorphic low noise devices by temperature storage. A 3-layer ebeam resist technology has been developed to realize T-gates without the use of RIE-etching attacking the semiconductor surface. Due to the aluminium based gate metal and production-level 50 kV exposure technique, the minimum gate length is limited to 120 nm. The low noise metamorphic technology provides a high maximum transconductance above 1000 mS/mm confirming the simulated benefits of the low bandgap material. With an off-state breakdown of 4.5V, requirements for a low-noise technology are fulfilled. However, electrical yields of the metamorphic low-noise technology are unsatisfactory for several reasons:

- shorts at the mesa edge are frequently formed between the gate metal and the channel - this is related to the epitaxy reproducibility showing some variation of the barrier thickness and the mechanical stability during high temperature device passivation.
- poor device pinch-off is observed due to not properly structuring of the gate foot resist - the gate length of 120 nm is close to the lower limit of the process.
- destruction of the device by not clearly identified influences such as ESD.

For a channel indium concentration of 43 %, the metamorphic power technology provides a much higher off-state breakdown voltage above 10 V. However, the devices cannot take advantage of the high off-state breakdown since impact ionization limits the operation voltage to the minimum requirement of 3 V. Electrical yields are significantly better compared to the low-noise technology linked to the thicker barrier layer.

Merely slight epitaxial modifications are necessary for the pseudomorphic HEMT technology to match with a gate length reduction from 130 to 80 nm. Most fabrication modules from the pHEMT production have been adopted except the gate foot lithography. Several ebeam exposure strategies have been compared to stabilize the gate length between 80 and 90 nm. As simulated, the pseudomorphic HEMT provides a lower maximum transconductance around 700 mS/mm. The off-state breakdown of typically 6.5 V fulfills the requirements for the power technology. At open channel, the pseudomorphic HEMT is much more robust than the metamorphic power device, and higher operation voltage levels result in superior RF-power densities. High electrical yields and a good reproducibility confirm a high maturity for the pHEMT technology.

Performance

An overview of the device performance is given in figure 7.1. The left part shows the transit frequency f_T and maximum oscillation frequency f_{max} as a function of the gate length L_g for the pseudomorphic single recess and metamorphic low noise devices characterized in this work. Cutoff frequencies increase linearly with reduced gate length. Comparing similar gate length, there is a clear advantage for the metamorphic HEMT. Due to a limitation of the gate length to 120 nm related to the available machine park, the metamorphic technology developed in this work could not demonstrate its whole low-noise potential. Therefore, values of the 50 nm gate length mHEMT technology of the Fraunhofer institute IAF (Freiburg, Germany) are added to the chart demonstrating cutoff frequencies of $f_T = 280$ GHz and f_{max} around 350 GHz [21] which cannot be realized with the pseudomorphic HEMT technology.

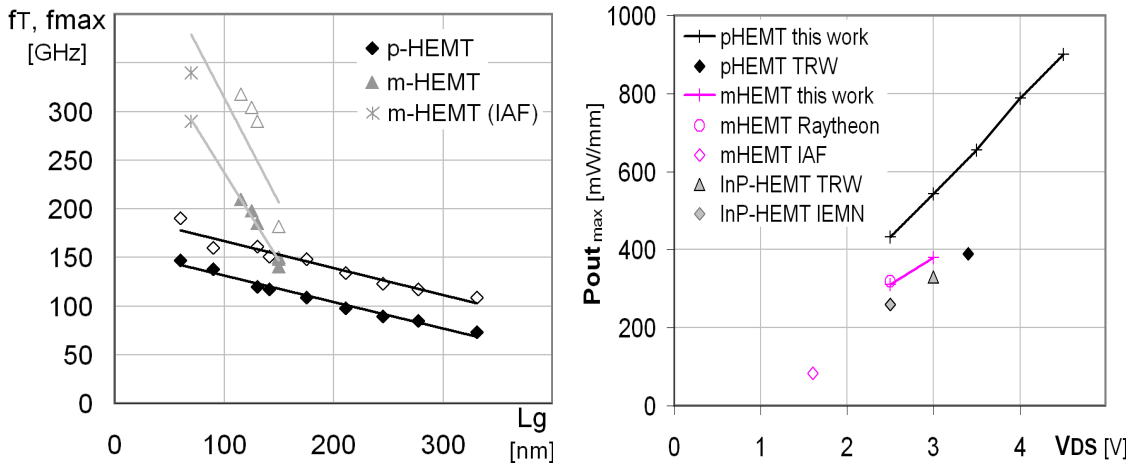


Figure 7.1: Dependence of the transit frequency f_T and maximum oscillation frequency f_{max} from the gate length for metamorphic and pseudomorphic low-noise devices (l). Power density at 94 GHz obtained from different power HEMT technologies (r).

Recent works on low band gap material HEMT structures demonstrate cutoff frequencies in the order of 600 GHz and target for MMIC operation beyond 300 GHz [167, 168]. These impressive results are mainly realized by gate length reduction down to 30 nm and minimization of the parasitic capacitances thanks to extremely thin or even no device passivation. It remains questionable, whether such technologies comply with the yield and reliability requirements of a production worth fabrication process.

On MMIC-level, the two-stage common source metamorphic low noise amplifier demonstrated 10 dB of gain from 75 to 106 GHz with a noise figure below 5 dB from 83 to 105 GHz. At 94 GHz, the noise figure is 4.5 dB for a gain of 12 dB. Due to the shorter gate length realized on the pseudomorphic HEMT technology, the two-stage pHEMT design showed almost similar performances with 12.8 dB gain at 94 GHz and even a lower noise figure of 3.7 dB. RF-power densities at 94 GHz are plotted in the right part of figure 7.1 for metamorphic, InP and pseudomorphic power HEMTs as a function of the supply voltage V_{DS}. Compared to literature results obtained on metamorphic and InP-based devices [164, 169, 166, 165], the metamorphic power technology developed in this work demonstrates state-of-the-art power performance. Similar for the pseudomorphic power technology. Due to the higher operation voltage and device robustness, the pseudomorphic HEMT provides the best power performance with power densities up to 900 mW/mm at 4.5 V. On MMIC-level, a maximum output power of 180 mW has been demonstrated at 94 GHz by a three-stage power amplifier design operated at 3.5 V with a linear gain of 11 dB, ranging from 92 to 102 GHz. At 1 dB-compression, the amplifier provided 130 mW of output power, sufficient for active radar imaging systems [5].

Outlook

Based on results from this work and the expertise on pHEMT production, UMS started the industrialization of the 80 nm gate length technology to provide low noise and power amplifiers for the next generation of W-band applications. Since wide band gap material devices continuously improve in RF-gain [170], once GaN-HEMTs may replace the pseudomorphic HEMT technologies, especially for high power amplifiers. At very high frequencies above 200 GHz, low band gap materials such as used for metamorphic HEMTs on GaAs or InP-technologies will remain the choice for MMIC-fabrication.

A Epitaxy

A.1 Sheet resistance: Metamorphic low-noise epitaxy

The sheet resistance of the 4” low-noise metamorphic HEMT epitaxy has been monitored by the contactless eddy current technique using a "Lehighton"-system. A wafer map of a representative wafer is given below. Compared to the values obtained by TLM measurements in figure 2.36 on page 42 there is a systematic offset of $10\,\Omega/_{\square}$ related to the different measurement tools.

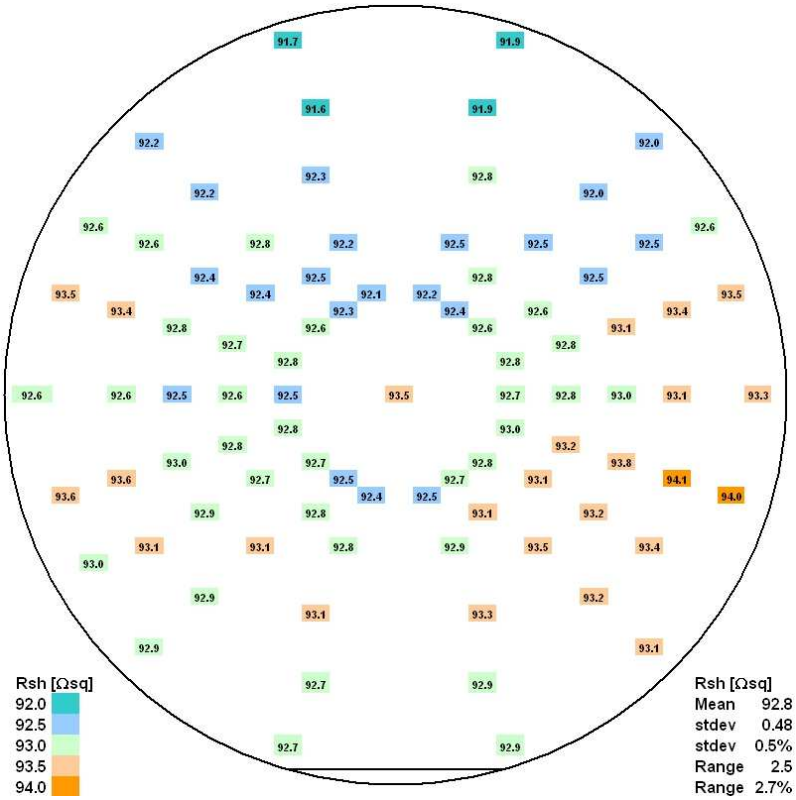


Figure A.1: Mapping of the sheet resistance R_{sh} of a 4” low-noise metamorphic HEMT epitaxy wafer.

A.2 Sheet resistance: Metamorphic epitaxy for power

In contrast to the metamorphic HEMT epitaxy material for the single recess configuration, merely very few wafers have been grown for the double recess technology. The characterization of the sheet resistance of both epitaxy versions has been performed by the contactless eddy current technique using a "Lehighton"-system.

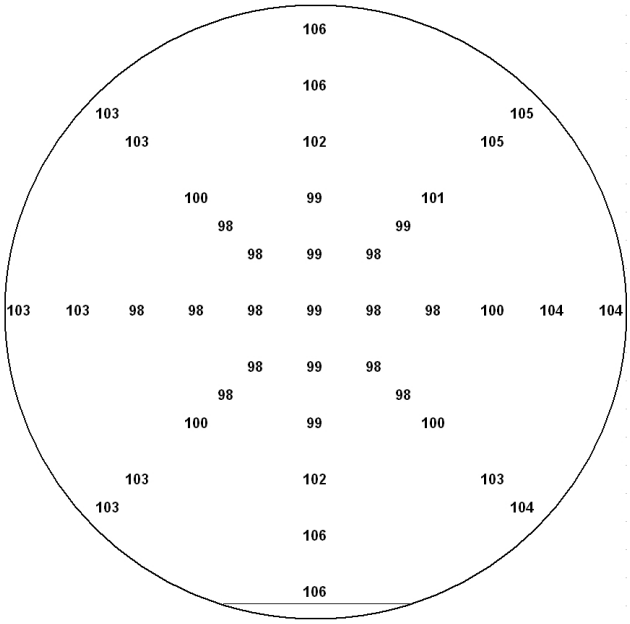


Figure A.2: R_{sh}-mapping of a 3" double recess metamorphic power HEMT epitaxy wafer.

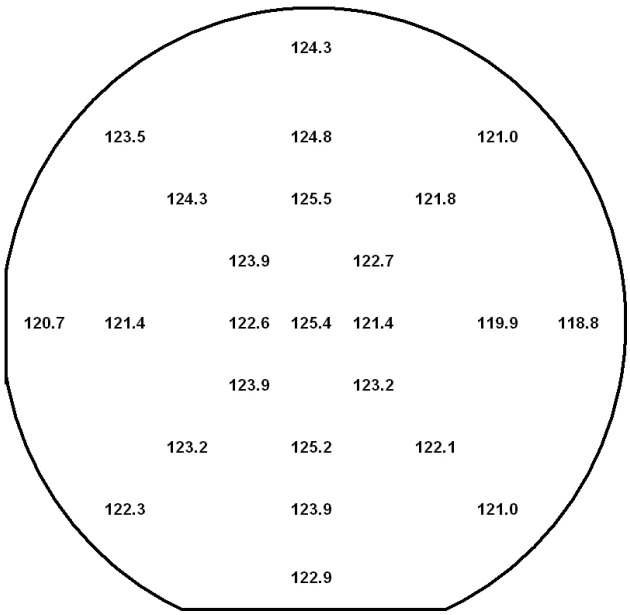


Figure A.3: R_{sh}-mapping of a 4" single recess metamorphic power HEMT epitaxy wafer.

A.3 Sheet resistance: Pseudomorphic HEMT epitaxy

The sheet resistance of the pseudomorphic HEMT epitaxy has been monitored by contactless characterization using the eddy current technique. Due to the high reproducibility of the epitaxy growth, measurement efforts has been reduced to spot check characterizations on the first and last wafer of a growth campaign.

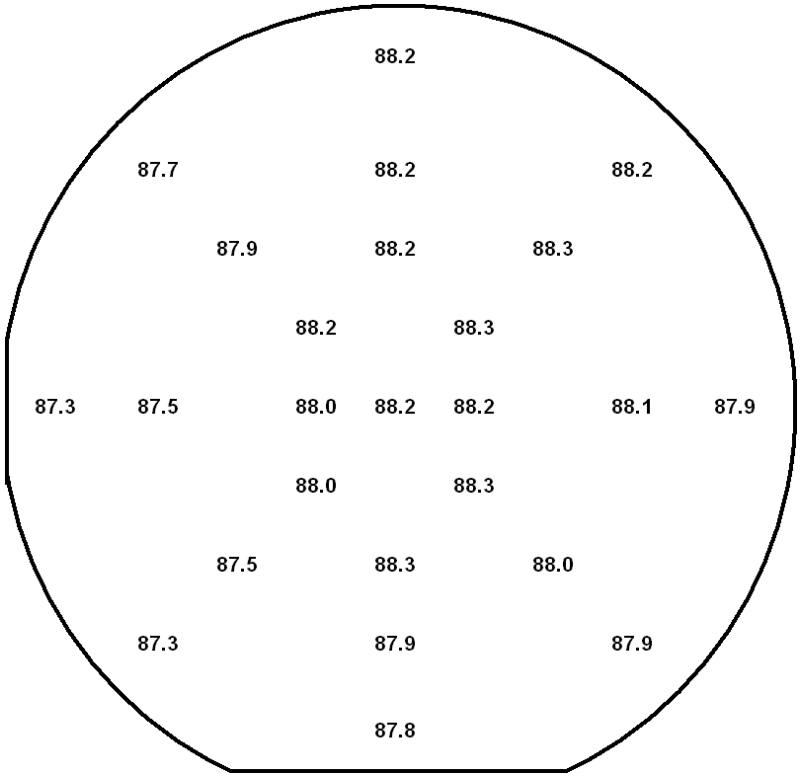


Figure A.4: Mapping of the sheet resistance R_{sh} on a 4" pseudomorphic HEMT epitaxy wafer.

B Mappings & further investigations

B.1 Ohmic contact resistance

The mappings of the ohmic contact resistance R_{co} on metamorphic low-noise and power HEMT technology wafers are shown below. A low, homogeneously distributed contact resistance of 0.083 Ωmm, $\sigma = 6\,\%$ and 0.123 Ωmm, $\sigma = 4\,\%$ is realized for the low-noise and power mHEMT technology, respectively. The lower value for the low-noise structure is related to the higher indium concentration of the channel and cap layer.

Rco	2	3	4	5	6	7	8
2							
3	0.08		0.08	0.08	0.08		0.07
4		0.09		0.09		0.08	
5	0.09		0.09		0.08		0.08
6		0.09		0.08		0.08	
7	0.08		0.09	0.09	0.09		0.08

Rco	2	3	4	5	6	7	8	9	10
2					0.12				
3				0.12		0.12			
4					0.13				
5		0.13		0.13		0.12		0.13	
6	0.13		0.13		0.13		0.13		0.12
7		0.13		0.13		0.13		0.12	
8	0.13		0.13		0.13		0.12		0.12
9		0.13		0.12		0.12		0.12	
10					0.12				
11				0.12		0.12			
12					0.12				

Figure B.1: Mapping of the ohmic contact resistance R_{co} (Ωmm) on metamorphic low-noise (l) and power HEMT technology (r) wafers.

B.2 Parameter mappings: low-noise mHEMT

The mappings of the key DC-parameters for a representative wafer of the metamorphic low-noise HEMT technology are shown below. The maximum saturation current I_{DS^+}, the maximum transconductance G_{max} and the pinch-off voltage V_{G100} are determined for a drain voltage of 1 V. The pinch-off voltage and the device breakdown voltage V_{bDS} are determined for a leakage current of 1 % of I_{DSS} which is close to 3 mA/mm.

Flat at bottom		Param.	IDS+__FET		Lot	K17014/ASTROLAN_02A			
		Unit	mA/mm		Wafer	2/R004			
Average	702		2	3	4	5	6	7	8
σ	14	1							
% s	2.0%	2							
Range	52	3	707		696	718	>>>		720
% Range	7.4%	4		702		710		697	
Min	675	5	706		695		710		710
Max	727	6		688		705		727	
Median	704	7	689		702	675	>>>		676

Figure B.2: Low-noise mHEMT: Mapping of I_{DS^+}.

Flat at bottom		Param.	Gmax__FET		Lot	K17014/ASTROLAN_02A			
		Unit	mS/mm		Wafer	2/R004			
Average	1122		2	3	4	5	6	7	8
σ	14	1							
% s	1.2%	2							
Range	55	3	1117		1107	1129	>>>		1156
% Range	4.9%	4		1127		1118		1121	
Min	1102	5	1118		1114		1131		1135
Max	1156	6		1124		1121		1140	
Median	1121	7	1104		1123	1102	>>>		1108

Figure B.3: Low-noise mHEMT: Mapping of G_{Mmax}.

Flat at bottom		Param.	VG100_FET						
		Unit	Volt						
Average	-0.43		2	3	4	5	6	7	8
σ	0.01	1							
% s	2.2%	2							
Range	0.03	3	-0.44		-0.43	-0.44	<<<		-0.43
% Range	7.2%	4		-0.43		-0.44		-0.43	
Min	-0.44	5	-0.44		-0.42		-0.43		-0.43
Max	-0.41	6		-0.41		-0.43		-0.44	
Median	-0.43	7	-0.43		-0.42	-0.41	<<<		-0.41

Figure B.4: Low-noise mHEMT: Mapping of V_{G100}.

Flat at bottor		Param.	VBDS_FET		Lot	K17014/ASTROLAN_02A			
		Unit	Volt		Wafer	2/R004			
Average	4.9		2	3	4	5	6	7	8
σ	0.2	1							
% s	4.0%	2							
Range	0.8	3	4.7		4.5	4.8	>>>		5.0
% Range	16.0%	4		4.7		4.7		5.1	
Min	4.5	5	4.7		4.6		4.9		4.8
Max	5.3	6		5.0		5.0		5.0	
Median	4.9	7	4.8		4.9	5.0	>>>		5.3

Figure B.5: Low-noise mHEMT: Mapping of V_{bDS}.

The mappings of the key RF-parameters of a 2x75 μm test device have been extracted from s-parameter measurements at 4 GHz. Bias conditions are 1 V drain voltage and 0 V gate voltage. The mappings below show the input capacitance c_{in}, the feedback capacitance c_f, the output resistance r_{out} and the RF-transconductance g_{me} of the RF-test device.

Flat at bottom		Param.	cin						
		Unit	fF						
Average	184.8		2	3	4	5	6	7	8
σ	250.1	1							
% s	135.4%	2							
Range	1127.8	3	123		155	128	129		1247
% Range	610.4%	4		129		129		126	
Min	119.3	5	127		126		126		126
Max	1247.1	6		132		131		128	
Median	128.2	7	129		130	130	119		124

Figure B.6: Low-noise mHEMT: Mapping of c_{in}.

Flat at bottom		Param.	cf						
		Unit	fF						
Average	73		2	3	4	5	6	7	8
σ	189	1							
% s	261.3%	2							
Range	849	3	30		33	29	29		877
% Range	1170.5%	4		29		29		29	
Min	29	5	30		29		29		30
Max	877	6		33		33		29	
Median	29.8	7	31		31	31	29		30

Figure B.7: Low-noise mHEMT: Mapping of c_f.

Flat at bottom		Param.	rout						
		Unit	Ohm						
Average	94.0				4	5	6	7	8
σ	14.8	1							
% s	15.8%	2							
Range	70.2	3	98		90	94	96		32
% Range	74.6%	4		98		96		100	
Min	32.2	5	98		101		98		95
Max	102.3	6		100		99		97	
Median	97.5	7	98		97	96	102		95

Figure B.8: Low-noise mHEMT: Mapping of R_{out}.

Flat at bottom		Param.	gme						
		Unit	mS						
Average	167.1		2	3	4	5	6	7	8
σ	6.8	1							
% s	4.1%	2							
Range	31.9	3	160		189	164	168		181
% Range	19.1%	4		166		167		165	
Min	156.6	5	165		162		165		168
Max	188.6	6		166		166		167	
Median	166.1	7	165		166	168	157		167

Figure B.9: Low-noise mHEMT: Mapping of g_{me}.

B.3 Parameter mappings: single recess power mHEMT

The mappings of the key DC-parameters obtained from a 1x100 μm test device of a representative metamorphic power technology wafer with single recess configuration are shown below. The maximum saturation current I_{DS^+}, the maximum transconductance G_{max} and the device pinch-off voltage V_{G100} are measured by a gate voltage sweep for a constant V_{DS} of 1 V. The device breakdown V_{bDS} and the pinch-off voltage V_{G100} are determined for a drain current of 1 % of the saturation current I_{DSS} obtained at V_{GS} = 0V.

IDS+ [mA/mm]		2	3	4	5	6	7	8	9	10
Mean	703	2					629				
σ	50	3				571		632			
Median	708	4					681				
		5		707		701		719		690	
		6	753		731		709		691		751
		7		774		719		711		726	
		8	776		737		612		698		754
		9		698		684		667		697	
		10					640				
		11				733		715			
		12					788				

Figure B.10: Mapping of I_{DS^+}.

GM [mS/mm]		2	3	4	5	6	7	8	9	10
Mean	681	2					637				
σ	30	3				627		663			
Median	687	4					675				
		5		694		692		681		686	
		6	723		702		701		681		701
		7		711		689		692		707	
		8	706		703		610		680		713
		9		676		665		638		685	
		10					610				
		11				705		674			
		12					709				

Figure B.11: Mapping of G_M.

VG100 [V]		2	3	4	5	6	7	8	9	10
Mean	-1.02	2					-0.98				
σ	0.06	3				-0.97		-0.98			
Median	-1.00	4					-0.98				
		5		-1.00		-0.99		-1.02		-0.99	
		6	-1.01		-1.02		-0.98		-0.99		-1.00
		7		-1.05		-1.01		-1.01		-1.00	
		8	-1.05		-1.03		-1.02		-1.01		-1.00
		9		-1.01		-0.98		-1.02		-0.98	
		10					-0.99				
		11				-1.03		-1.33			
		12					-1.06				

Figure B.12: Mapping of V_{G100}.

VbDS [V]		2	3	4	5	6	7	8	9	10
Mean	8.0	2					9.0				
σ	2.8	3				0.1		9.2			
Median	9.0	4					9.7				
		5		8.9		9.4		9.2		9.3	
		6	8.6		0.2		9.0		8.8		8.8
		7		8.7		9.6		8.8		9.0	
		8	8.5		9.4		0.4		9.1		9.0
		9		8.8		9.0		9.1		9.3	
		10					4.7				
		11				10.5					
		12					8.6				

Figure B.13: Mapping of V_{bDS}.

The key RF-parameters have been extracted from s-parameter measurements at 4 GHz; the 2x75 μm test devices have been operated at 1 V drain and 0 V gate voltage.

Cin [fF]			2	3	4	5	6	7	8	9	10
Mean	113.6	2					105.5				
σ	9.7	3				106.5		115.2			
Median	115.9	4					113.2				
		5		106.6		115.1		117.8		117.4	
		6	107.3		113.9		117.3		115.1		106.5
		7		114.2		116.6		118.2		118.2	
		8	117.7		112.4		120.8		111.9		118.1
		9		115.7		119.0		68.3		120.2	
		10					120.3				
		11				120.0		122.2			
		12					116.2				

Figure B.14: Mapping of c_{in}.

Cf [fF]			2	3	4	5	6	7	8	9	10
Mean	23.3	2					22.8				
σ	3.9	3				22.7		23.1			
Mediar	22.7	4					23.1				
		5		21.7		23.9		22.7		21.4	
		6	22.1		22.7		24.7		23.7		22.9
		7		22.1		23.7		23.6		21.8	
		8	27.2		22.0		24.0		42.3		20.9
		9		22.2		23.2		18.0		22.3	
		10					23.0				
		11				21.7		22.4			
		12					22.3				

Figure B.15: Mapping of c_f.

rout [Ω]			2	3	4	5	6	7	8	9	10
Mean	82.5	2					68.9				
σ	5.8	3				77.1		78.4			
Median	83.1	4					75.3				
		5		85.1		79.5		83.0		88.4	
		6	83.3		83.2		80.7		81.7		97.8
		7		85.6		83.2		80.8		86.1	
		8	82.8		84.5		79.1		87.2		88.7
		9		84.0		84.0		67.9		82.1	
		10					80.0				
		11				88.2		89.1			
		12					80.3				

Figure B.16: Mapping of r_{out}.

gme [mS]			2	3	4	5	6	7	8	9	10
Mean	55.5	2					58.8				
σ	7.4	3				55.0		53.1			
Mediar	55.0	4					53.3				
		5		51.5		60.7		54.7		63.3	
		6	51.4		60.3		54.3		56.1		50.0
		7		63.1		59.8		60.0		59.9	
		8	65.7		62.2		53.1		53.2		58.9
		9		57.0		53.7		23.3		58.9	
		10					51.2				
		11				52.2		54.7			
		12					55.0				

Figure B.17: Mapping of g_{me}.

B.4 Parameter mappings: power pHEMT

Mappings of the key DC-parameters obtained from a 1x100 μm test device of a representative power pHEMT wafer. The maximum saturation current I_{DS+}, the maximum transconductance G_{max} and the device pinch-off voltage V_{G100} are measured by a gate voltage sweep for a constant V_{DS} of 1 V. The device breakdown V_{bDS} and the pinch-off voltage V_{G100} are determined for a drain current of 1 % of the saturation current I_{DSS} obtained at V_{GS} = 0V.

IDS+ [mA/mm]		2	3	4	5	6	7	8	9	10
	2					>>>				
	3				647		646			
Average	636					647				
σ	16		637		>>>		644		643	
Median	638	651		658		634		647		629
	7		627		616		627		638	
	8	645		650		622		627		621
	9		631		625		649		662	
	10					652				
	11				618		634			
	12					585				

Figure B.18: Mapping of I_{DS+}.

Gmax [mS/mm]		2	3	4	5	6	7	8	9	10
	2					>>>				
	3				776		765			
Average	761					777				
σ	17		722		>>>		769		765	
Median	764	713		754		744		767		761
	7		762		756		770		770	
	8	754		762		761		769		769
	9		736		742		765		787	
	10					787				
	11				764		780			
	12					752				

Figure B.19: Mapping of G_M.

VG100 [V]		2	3	4	5	6	7	8	9	10
	2					<<<				
	3				-.53		-.53			
Average	-0.54					-.55				
σ	0.01		-.54		<<<		-.56		-.56	
Median	-0.54	-.56		-.56		-.54		-.53		-.53
	7		-.53		-.51		-.55		-.56	
	8	-.54		-.53		-.55		-.54		-.54
	9		-.54		-.52		-.53		-.52	
	10					-.54				
	11				-.52		-.53			
	12					-.50				

Figure B.20: Mapping of V_{G100}.

VbDS [V]		2	3	4	5	6	7	8	9	10
	2					>>>				
	3				6.3		6.0			
Average	6.3					6.2				
σ	0.2		6.6		>>>		6.2		6.4	
Median	6.3	5.6		6.1		6.3		6.3		6.5
	7		6.3		6.4		6.4		6.4	
	8	6.3		6.2		6.3		6.5		6.6
	9		6.6		6.2		6.2		6.5	
	10					6.3				
	11				6.5		6.3			
	12					6.5				

Figure B.21: Mapping of V_{bDS}.

The key RF-parameters have been extracted from s-parameter measurements at 4 GHz; the 2x75 μm test devices have been operated at 3 V drain and 0 V gate voltage.

cin [fF]			2	3	4	5	6	7	8	9	10
Mean	98.9	2					84.6				
σ	3.8	3				95.4		97.3			
Median	100.1	4					101.7				
		5		100.3		100.3		99.2		89.1	
		6	100.7		100.0		100.2		100.4		96.2
		7		100.1		99.4		100.6		98.7	
		8	99.8		100.1		99.2		100.8		NoM
		9		99.2		99.0		100.9		98.1	
		10					103.0				
		11				101.3		100.5			
		12					103.1				

Figure B.22: Mapping of c_{in}.

cf [fF]			2	3	4	5	6	7	8	9	10
Mean	21.9	2					17.6				
σ	0.9	3				21.2		22.4			
Median	22.1	4					22.6				
		5		21.5		21.9		21.9		21.5	
		6	22.6		22.1		21.4		21.4		23.1
		7		22.1		21.7		21.6		22.5	
		8	22.2		22.3		21.4		22.2		NoM
		9		22.8		22.1		22.1		22.5	
		10					22.1				
		11				22.4		22.2			
		12					22.1				

Figure B.23: Mapping of c_f.

rout [Ω]			2	3	4	5	6	7	8	9	10
Mean	124.6	2					69.0				
σ	11.9	3				104.0		126.8			
Median	127.3	4					123.2				
		5		124.5		122.8		126.7		125.9	
		6	124.5		128.5		131.1		128.5		121.8
		7		126.5		130.3		129.2		128.0	
		8	121.1		126.5		130.0		130.3		NoM
		9		131.0		124.9		128.2		132.2	
		10					127.3				
		11				131.2		131.3			
		12					127.4				

Figure B.24: Mapping of r_{out}.

gme [mS]			2	3	4	5	6	7	8	9	10
Mean	105.3	2					84.3				
σ	5.0	3				98.6		99.3			
Median	106.5	4					107.8				
		5		107.4		106.2		106.4		99.1	
		6	109.0		106.3		105.9		105.4		102.8
		7		106.6		106.1		106.8		104.6	
		8	107.6		107.0		105.3		108.8		NoM
		9		106.5		106.7		108.1		104.2	
		10					110.0				
		11				109.4		108.6			
		12					110.3				

Figure B.25: Mapping of g_{me}.

B.5 S-parameter characterization up to 110 GHz

B.5.1 Gain of the metamorphic single recess power HEMT

Comparison of the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral gain MUG and the stability factor k between the symmetric and asymmetric gate configuration. Device topologies are 2x40 μm and 6x40 μm.

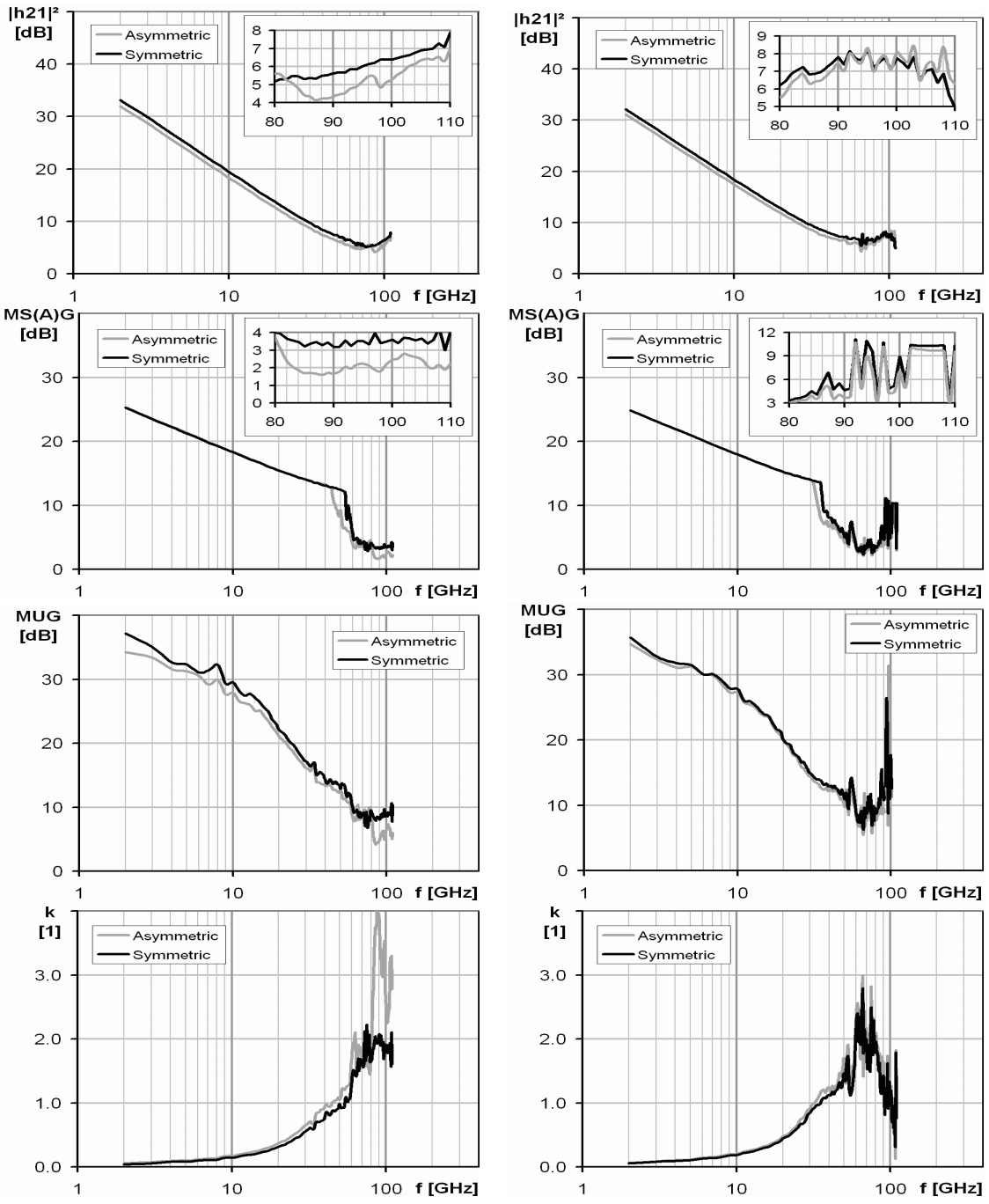


Figure B.26: Small signal performance of a 2x40 μm (l) and 6x40 μm (r) metamorphic power HEMT with symmetric (black) and asymmetric (grey) gate configuration. Biasing is close to maximum gain with V_{DS} = 2.5 V and V_{GS} = -0.4 V.

B.5.2 Gain of the pseudomorphic power HEMT

Comparison of the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral gain MUG and the stability factor k between the symmetric and asymmetric gate configuration. Device topologies are 2x40 μm and 6x40 μm.

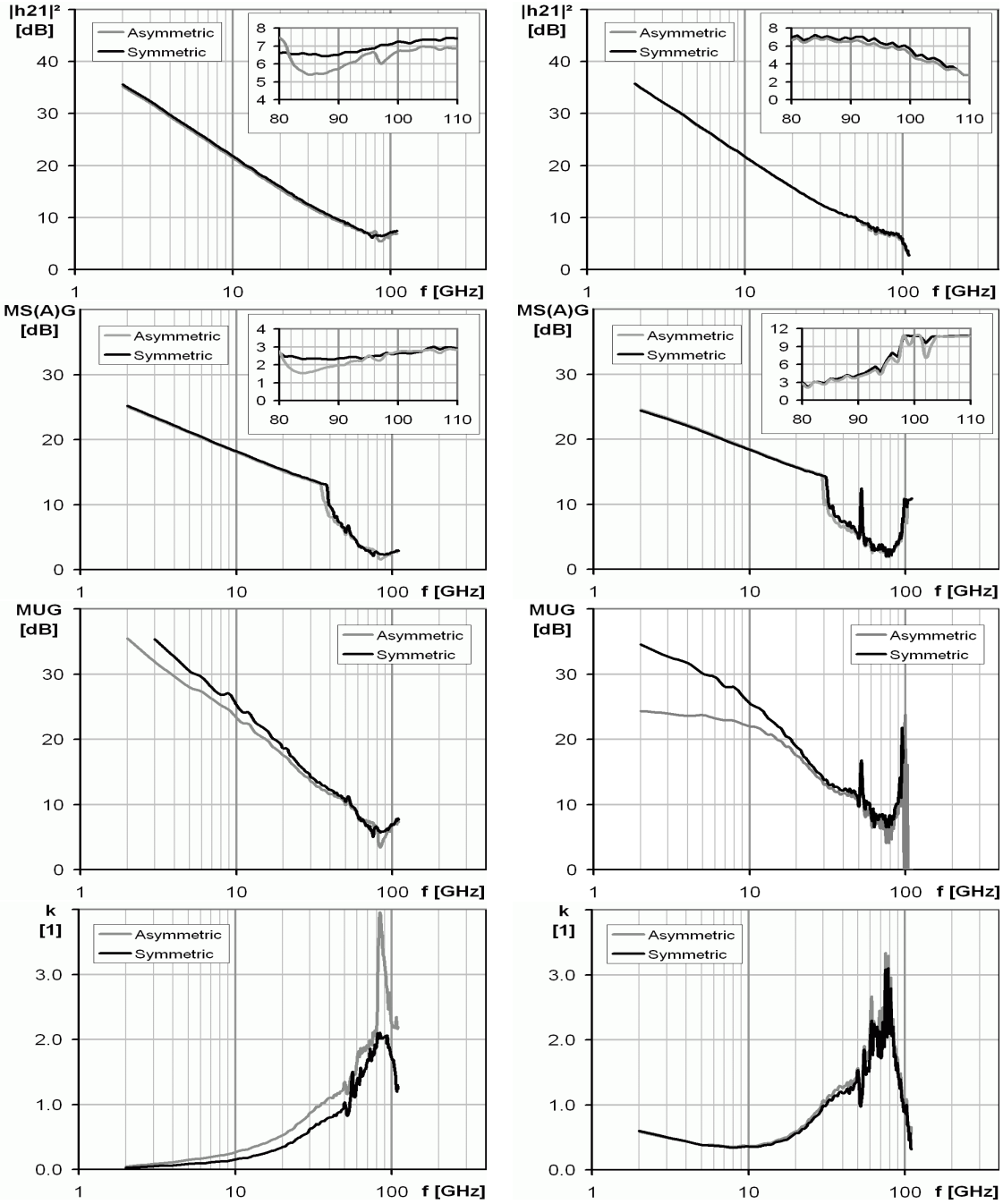


Figure B.27: Small signal performance of a 2x40 μm (l) and 6x40 μm pseudomorphic HEMT with symmetric (black) and asymmetric (grey) gate configuration biased at $V_{DS} = 3.5$ V and $V_{GS} = 0$ V.

B.5.3 Gain of different pHEMT base cells

Comparison of the current gain $|h_{21}|^2$, the maximum available gain MAG, the maximum unilateral gain MUG and the stability factor k between different types of transistor cells. Device topologies are 2x40 μm and 6x40 μm.

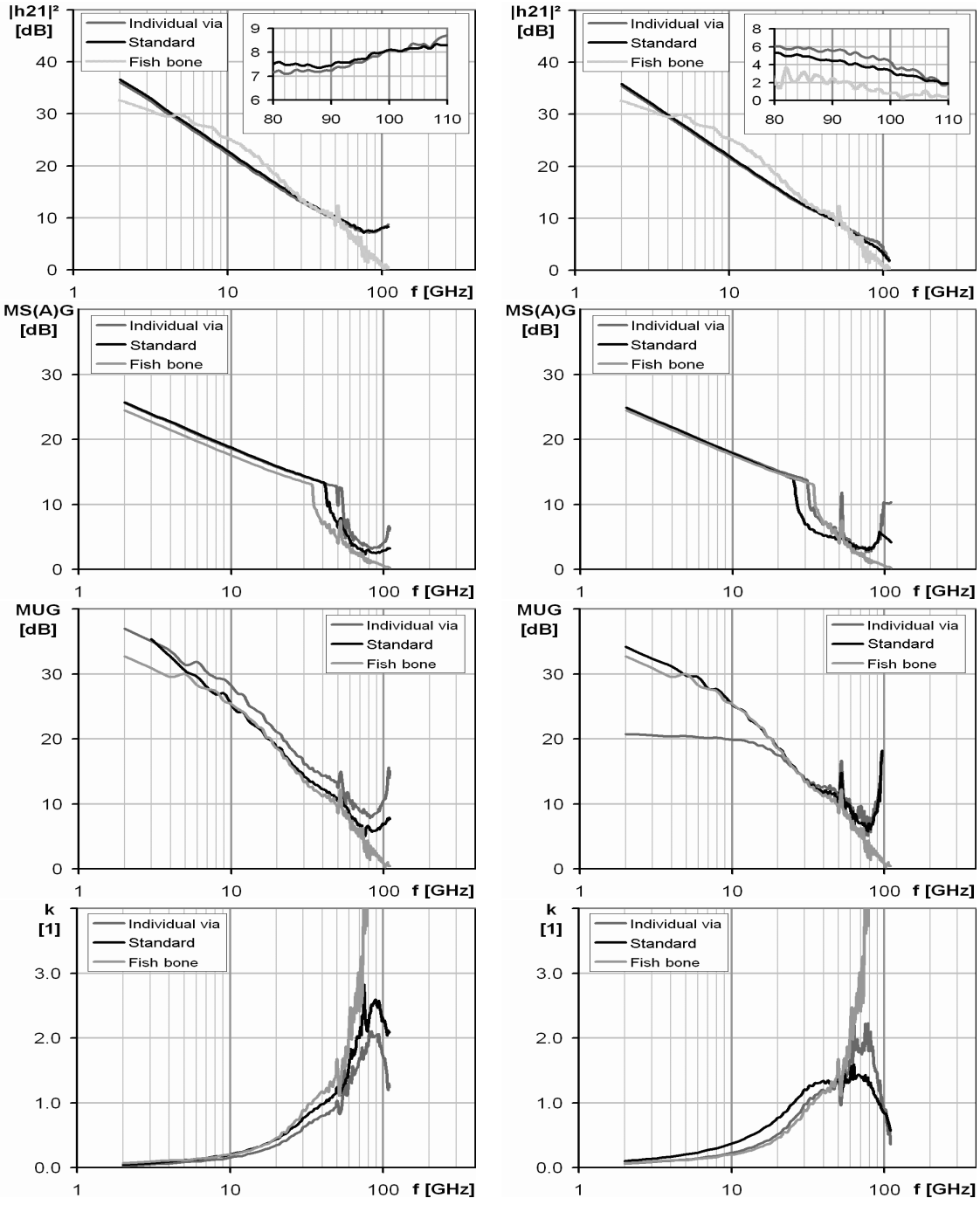


Figure B.28: Small signal performance of a 2x40 μm (l) and 6x40 μm pseudomorphic HEMT with symmetric gate configuration but different base cell type; bias is V_{DS} = 3 V and V_{GS} = -0.1 V.

B.6 Passive components

After the fabrication of the active devices, the passive components like resistors, capacitors, inductors, lines and interconnects are realized. Besides the semiconductor resistors which are formed together with the active device and connected by the ohmic metalization, thin film resistors as shown in the left part of figure B.29 of $30\,\Omega/_{\square}$ and $1000\,\Omega/_{\square}$ are formed by TaN and TiWSi deposition and the lift off technique. In integrated circuits, the negative temperature coefficient of the thin film resistors allows compensation of the positive coefficient of the semiconductor resistors.

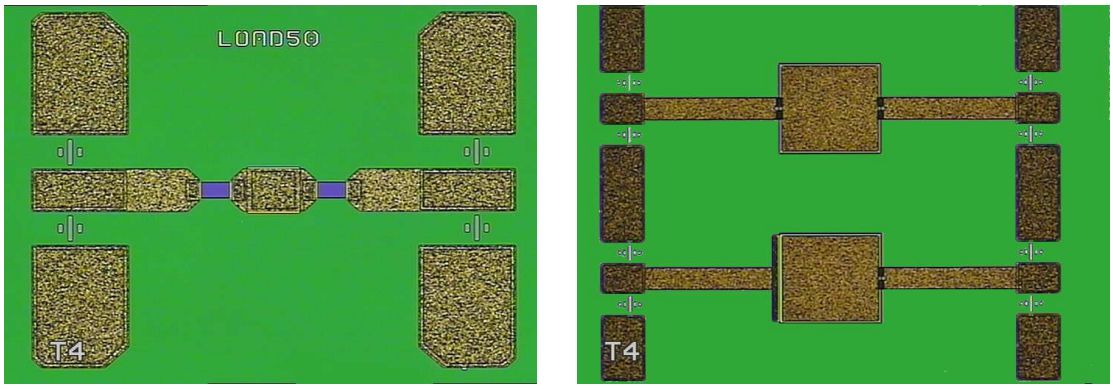


Figure B.29: Passive components: Thin film resistor (l) and MIM-capacitor (r).

To realize MIM-capacitors as depicted in the right part of figure B.29, a third metalization layer is used for the bottom electrode. A second silicon nitride layer forms the dielectric material, and the top electrode is based on electroplated gold. Electroplating is also used to realize air-bridges, lines and spiral inductors as shown in B.30.

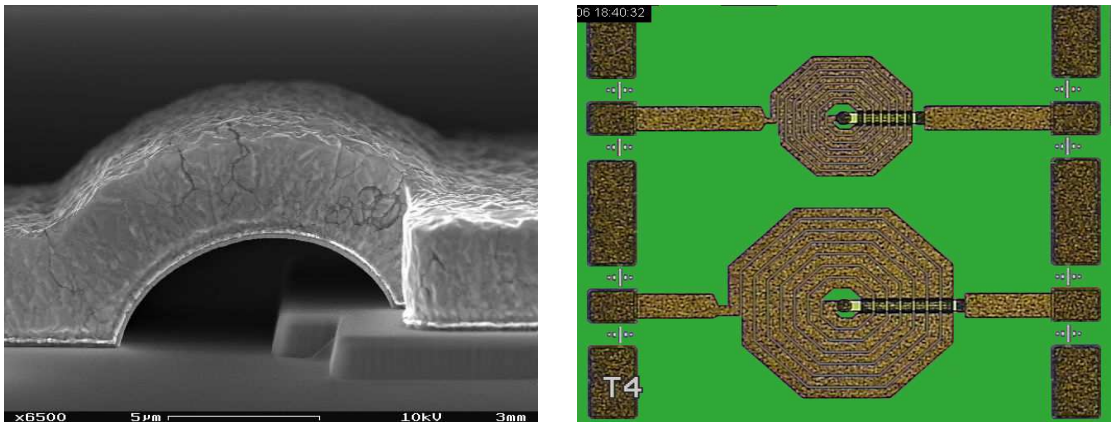


Figure B.30: Passive components: Air bridge (l) and inductor (r).

To contact the different conductive layers of the active and passive components, several interconnect openings through the dielectric layers are formed by lithography and plasma etching.

B.7 Backside fabrication

To realize micro strip design circuits, a backside metalization layer is used as a ground plane. To connect the ground pads on the wafer front side with the back side metalization, via interconnects are formed through the GaAs substrate. Therefore, the GaAs substrate has to be thinned down from 650 μm to 100 μm. Wafer thinning down to 70 μm is required to realize individual source vias for the active device. The reduced substrate thickness further supports the heat transfer between the active device and the heat sink. However, the reduction of the substrate thickness for a fixed impedance Z_0 increases conductor losses due to the narrowed conductor width [171]. Therefore, the thickness of the substrate strongly depends on the application; while power designs preferably use thin substrates down to 50 μm to improve heat transfer, a thickness of 100 μm is frequently used for micro strip low-noise circuits. A limitation for micro strip designs is further given by the application frequency where lowest order TE-surface mode propagation gets supported for a substrate thickness above h_{TE} as given in equation B.1 [172]. The substrate thickness of the coplanar low noise amplifiers fabricated in this work is 200 μm.

$$h_{TE} = \frac{c}{4f} \left(\varepsilon_r - 1\right)^{-\frac{1}{2}} \tag{B.1}$$

For the power technologies the substrate thickness is 70 μm. Even for the more rigid criterium of $\lambda/10$ of 2.5 mm for the evaluation of minimum substrate thickness, the corresponding maximum frequency is around 120 GHz and fits for W-band operation .

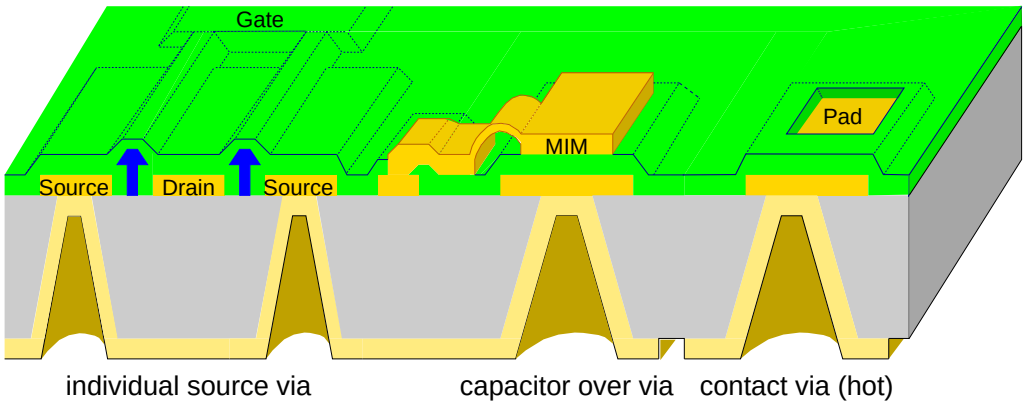


Figure B.31: Several ways to use via interconnects.

The substrate thickness is reduced by a grinding and polishing process. Via interconnects are formed by contact lithography and reactive ion etching. These via interconnects contact the ground pads of the wafer surface with the electroplated backside metalization and are located at the bottom electrodes of capacitors and the source pads of individual source via transistors. The individual source via provides a small source inductance, especially on large multi finger devices used for high power application designs.

B.8 Nano-indentation on $In_{53}Ga_{47}As$

Nano-indentation characterizations have been performed at the Technical University of Wildau. Since the doping level [173] and crystal defects caused by boron implantation [174] affect the micro hardness of semiconductor materials, a comparison has been performed between a 1 μm thick $In_{53}Ga_{47}As$ layer grown lattice matched on InP and on the GaAs substrate using a metamorphic buffer. While the metamorphic structure shows a significant surface roughness of 70 nm peak-to peak, the lattice matched sample is perfectly smooth.

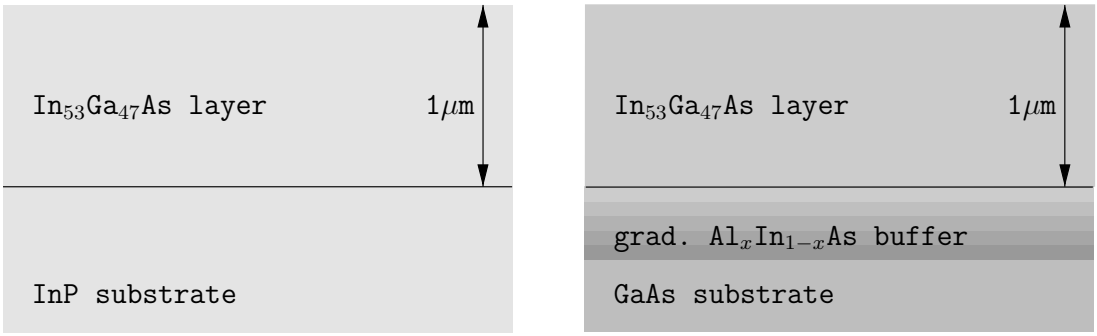


Figure B.32: Layer sequence of the $In_{53}Ga_{47}As$ samples grown lattice matched on InP (l) and GaAs substrate (r) using a metamorphic buffer.

A schematic sketch of the epitaxy samples is given in figure B.32. The samples have been grown on the 3" solid source MBE of the Daimler-Research group in Ulm, Germany. A large layer thickness of 1 μm has been chosen to reduce the impact of the substrate or buffer layer on the $In_{53}Ga_{47}As$ layer characterization.

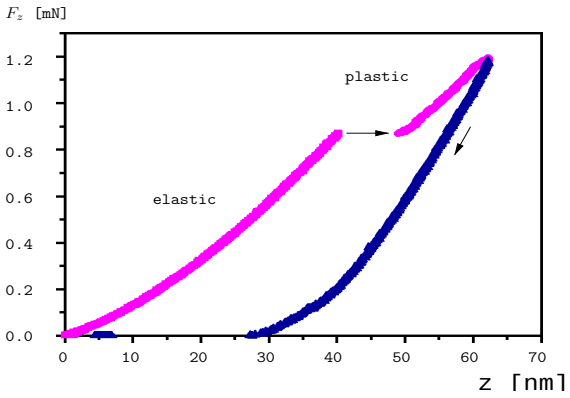


Figure B.33: Principle load-depth curve obtained from nano-indentation. On GaAs, there is elastic (reversible) deformation followed by sudden pop-in and further plastic deformation.

The load-depth curve obtained during nano-indentation is shown in figure B.33. A diamond tip (indenter) is pressed on the sample's surface with increasing force F_z while monitoring the penetration depth z. Below the critical indentation force F_{crit}, the deformation is elastic and completely reversible. For a higher load e.g. on silicon or InSb crystals, the area of plastic deformation is entered and phase transformations are observed [174]. On GaAs however, the plastic deformation starts suddenly with a "pop-in" event of around 10 nm depth. This is linked to the motion of dislocations induced by the contact

pressure of the indenter at a load level above 0.88 mN. For a high defect density material, like boron implanted GaAs, pop-in events are significantly reduced or completely disappear.
To evaluate the influence of the surface roughness of the metamorphic sample, the indentation has been performed with two different indenter geometries. A spherocone indenter was used with a tip radius of 400 nm which is in the order of the pattern size of the crosshatch structure. The second indenter of Berkowich type had a shape of a triangular pyramid with a smaller radius of 150 nm. Figure B.34 shows the load-depth characteristic of both samples using the large tip radius for indentation. Like for GaAs, a pop-in event is observed at a penetration depth of around 40 nm. However, pop-in occurs for a lower load of 0.7 mN.

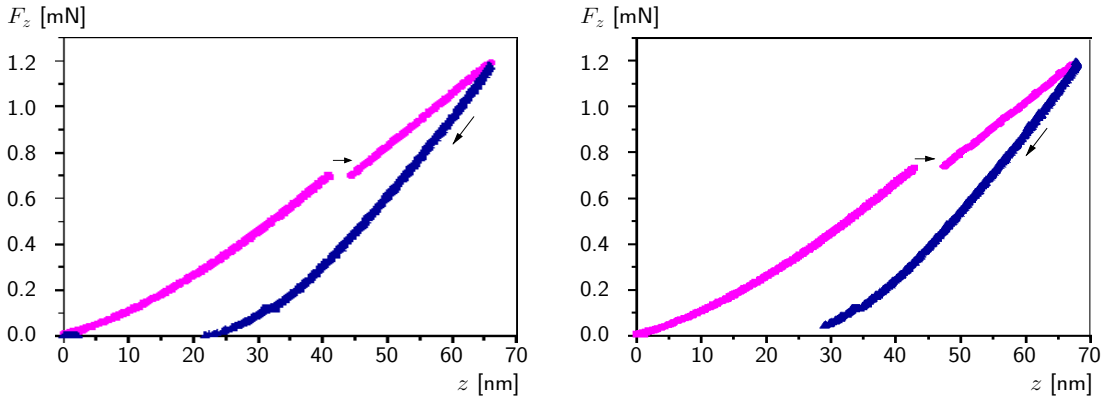


Figure B.34: Load-depth characteristic of $In_{53}Ga_{47}As$; lattice matched on InP (l) and metamorphic on GaAs substrate (r) using a 400 nm spherocone indenter.

For a easier comparison, the normalized load-depth characteristic is depicted in figure B.35 giving evidence of the premature but less pronounced pop-in event of the InGaAs-samples compared to GaAs. The slightly reduced pop-in-behavior for the metamorphic sample is related to the surface roughness.

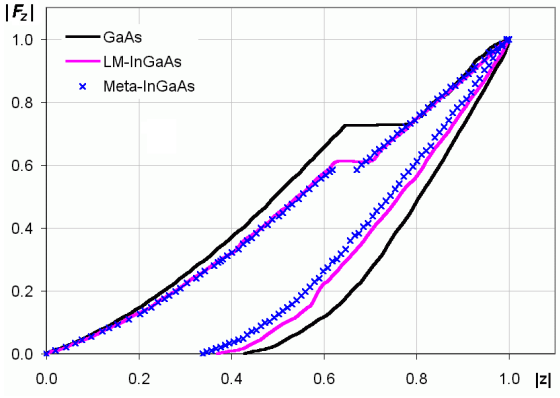


Figure B.35: Normalized load-depth-curves for the GaAs and both InGaAs-samples using a 400 nm spherocone indenter.

Experiments have been repeated for the smaller tip geometry to minimize the impact of surface roughness. The results are depicted in figure B.36. With the small tip radius

of 150 nm, the measurement noise is increased related to the lower load and penetration depth.

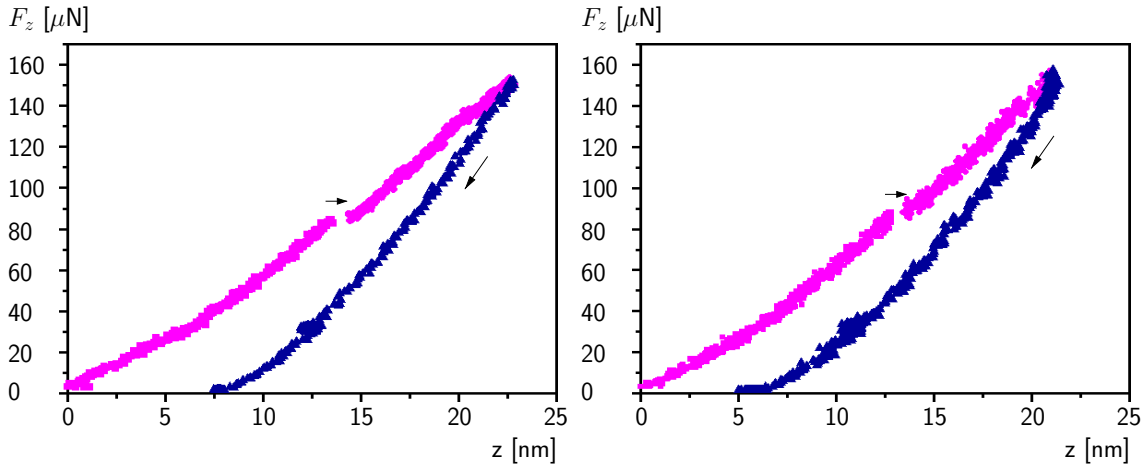


Figure B.36: Load-depth characteristic of $In_{53}Ga_{47}As$; lattice matched on InP (l) and metamorphic on GaAs substrate (r) using a small 150 nm Berkowich indenter.

An overlay of the normalized and smoothed curves for both $In_{53}Ga_{47}As$ samples in figure B.37 confirms the similar indentation behavior for the small tip geometry.

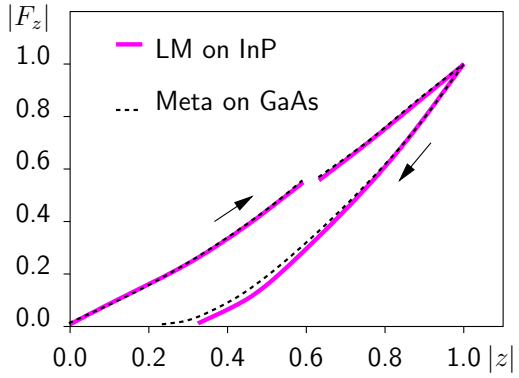


Figure B.37: Normalized load-depth curves for the GaAs and both $In_{53}Ga_{47}As$ samples using a 150 nm Berkowich indenter.

After nano-indentation, a contact mode surface scan of the indentation area has been performed showing the imprint of the 400 nm conical indenter in figure B.38. Although the round indenter causes an isotropic stress field, the strong covalent bonding forces cause a quadratic indentation hole, representing the cubic crystallographic structure of $In_xGa_{1-x}As$. In contrast to GaAs, there is an unequal pile-up pattern reflecting the one-fold symmetry of the $In_xGa_{1-x}As$ alloy with respect to the (100) surface [175].

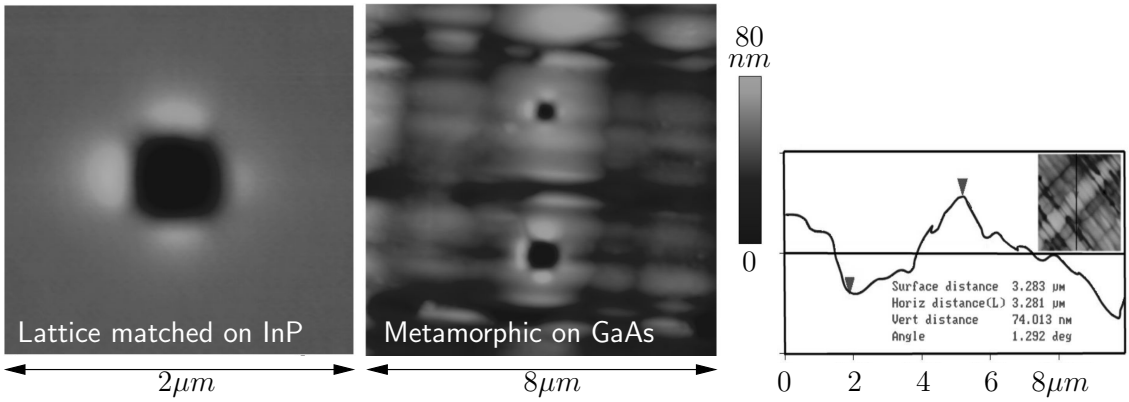


Figure B.38: Imprint after indentation on InP and metamorphic substrates. The AFM line scan (r) identifies the high surface roughness of the metamorphic sample.

By experiment, an elastic indentation module of 105 GPa has been calculated for the $In_{53}Ga_{47}As$ layer. Calculations of the indentation module as proposed by Hill [176] result in a 7 % lower value of 97.5 GPa. The higher experimental value is explained by surface oxidation. Surface deoxidation by ammonia solutions and nano-indentation in inert atmosphere may reduce the discrepancies between theory and measurements.

B.9 Two step RIE-free gate technology

For a resist thickness of 900 nm, the minimum gate length for the 50 kV exposed 3-layer resist gate technology is limited to 100 nm. To reduce the impact of forward scattering, a two step exposure technique has been investigated. Here, the top and middle resists are exposed with 50 kV using a low dose level followed by resist development. A second 50 kV exposure at high dose is performed for the bottom resist to define the gate foot. As shown in the left part of figure B.39, large structures can be realized more accurately in the 3-layer resist stack compared to the direct writing exposure technique; proximity effects causing round corners are oppressed.

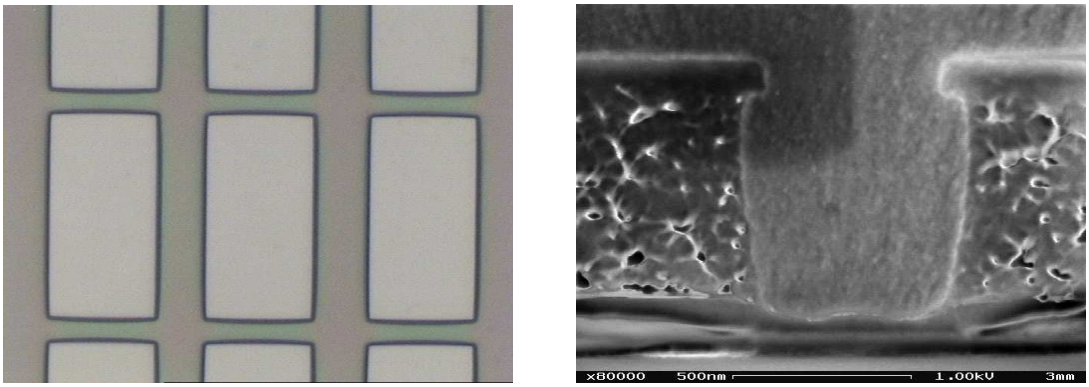


Figure B.39: Improved shape for large gate pads (l) due to the double exposure technique. After the first lithography and resist development, there is an undercut profile required for the lift off (r).

The right part of figure B.39 shows the resist profile of the gate structure after the development of the top and middle resist with a clearly defined undercut profile. To optimize the conditions for the first exposure, dose variations have been performed including the complete resist development sequence for all resist layers. The electron microscopy images of the resist profile in figure B.40 demonstrate the effect of a too high first exposure dose on the bottom resist. While two trenches are formed in the bottom resist representing a moderate overexposure, a very high dose results in complete removal of the bottom resist.

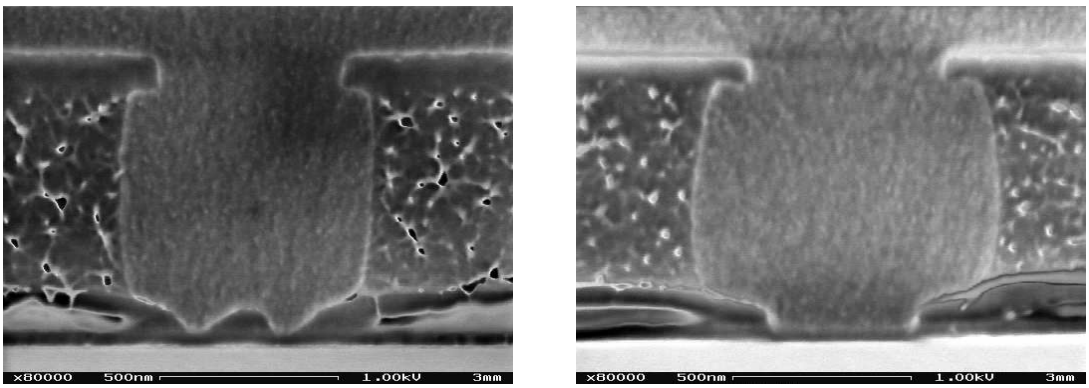


Figure B.40: Impact of a too high dose for the first exposure on the resist profile after the complete development sequence. A slightly too high dose forms trenches within the bottom resist (l). Complete bottom resist removal is observed for a significant over exposure (r).

With optimized exposure conditions for the first lithography step, the bottom resist withstands the complete development sequence without being attacked. Anyway, the first exposure provides a significant preliminary dose to the bottom resist worsening its contrast properties. As a consequence, the resist profile in figure B.41 shows a foot opening larger than 150 nm. A dose reduction for the gate foot exposure helps to reduce the gate length down to around 100 nm similar to the direct write strategy.

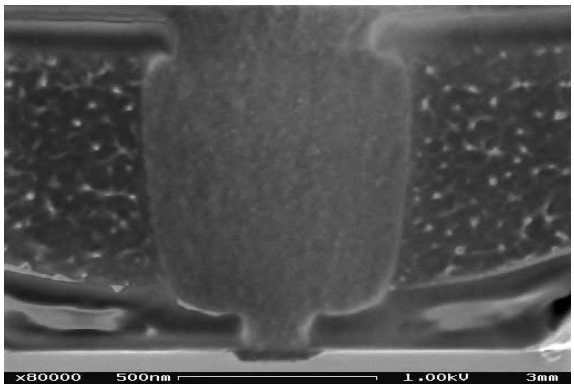


Figure B.41: Profile of the 3-layer resist stack exposed by the two step strategy. Due to degraded contrast properties of the bottom resist caused by the first exposure dose, the foot opening is much larger than expected from a single resist ebeam lithography.

The gate length could not be reduced by the two step exposure strategy due to an insufficient process window regarding the critical dose and the contrast properties of the different resist types. Improvements demonstrated on large structures alone do not justify this more complex and cost intensive technology. Furthermore, the two step strategy is sensitive towards misalignment between the gate foot and gate head; in combination with the reduced contrast properties of the bottom resist, a misaligned gate foot exposure would cause increased spreads for the gate length.

C Models & circuit principles

C.1 Simplified small signal model

For process control monitoring on RF-test devices, the small equivalent circuit of figure 2.15 is drastically simplified [93] as shown in figure C.1. Extrinsic parasitic elements, leakage currents and impact ionization are neglected.

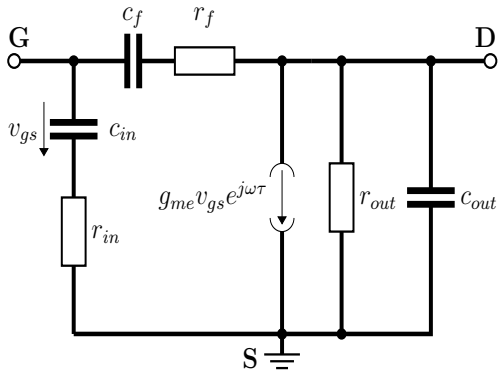


Figure C.1: Simplified small signal equivalent circuit of the 2x75 μm RF-test device [93].

This simplification can be accepted as long the intrinsic parts dominate the device performance. Elements of the simplified equivalent circuit are calculated from the admittance parameters y_{ij} in equations C.1; admittance parameters are obtained from the scattering parameters by linear transformation.

$$
\begin{aligned}
c_f &= \frac{-|y_{12}|^2}{\omega\,\Im(y_{12})} & r_f &= \frac{-\Re(y_{12})}{|y_{12}|^2} \\
c_{in} &= \frac{|y_{11}+y_{12}|^2}{\omega\,\Im(y_{11}+y_{12})} & r_{in} &= \frac{\Re(y_{11}+y_{12})}{|y_{11}+y_{12}|^2} \\
c_{out} &= \frac{\Im(y_{22}+y_{12})}{\omega} & r_{out} &= \Re(y_{22}-y_{12})^{-1} \\
g_{me} &= |y_{22}-y_{12}|\sqrt{1+\omega^2 r_{gs}^2 c_{gs}^2} & \omega &= 2\pi\, f
\end{aligned}
\tag{C.1}
$$

C.2 ADS-model elements: low-noise mHEMT

The small signal equivalent circuit elements of two base cell devices have been derived from small signal parameter measurements up to 110 GHz. Noisy elements are based on V- and W-band noise parameter measurements performed at Millilab. The model has been implemented into the electronic device simulation software ADS to support the design of the low noise amplifier demonstrators.

Element	2x20 μm device	4x20 μm device
L_G [pH]	45.8	38.5
L_S [pH]	3.4	3.4
L_D [pH]	25.6	30.6
c_{gm} [fF]	6.5	6.5
c_{sm} [fF]	0.01	0.01
c_{gs} [fF]	38.4	72.0
c_{gd} [fF]	10.6	25.4
c_{ds} [fF]	13.6	27.2
R_S [Ω]	6.3	3.1
R_D [Ω]	6.3	3.1
R_G [Ω]	0.93	0.46
r_{ds} [Ω]	216	101
r_i [Ω]	10	4.5
g_m [mS]	61.4	125
τ [pS]	0.61	0.61
kk [1]	$5 \cdot 10^8$	$1 \cdot 10^9$
rr [1]	0.128	0.397
v_{sat} [10^6 m/s]	0.188	0.216
r_{gs} [$k\Omega$]	147	36.8
r_{gd} [$k\Omega$]	188	39.4
r_{im} [kΩ]	35.8	32.9
c_{im} [fF]	0.66	0.99
I_{im} [pA]	48.6	65.7
$I_{ng}(94\,GHz)$ [pA]	0.038	0.028
$I_{nd}(94\,GHz)$ [pA]	865	1128

Table C.1: Elements of the small signal equivalent circuit of figure 4.13 including noise sources for the metamorphic low-noise technology with 60 % mean channel indium content. Device topologies are 2x20 μm and 4x20 μm; biasing is set to 1 V drain source voltage and current density of 220 mA/mm as typically applied in the LNA demonstrators.

C.3 Non-linear model: Power pHEMT

The non-linear equivalent circuit elements of the power pHEMT are derived from small signal measurements covering the whole output characteristic. Voltage dependent elements extracted by fitting routines such as the input capacitance and gate currents are described by the Tajima [163] equations. For simplification reasons, impact ionization as well as the voltage dependence of the feedback capacitance which are relevant to describe the device linearity performance have been neglected. The model has been implemented into the electronic device simulation software ADS to support the design of the power amplifier demonstrators.

element	value or formula	
	N = 4 fingers	N = 6 fingers
L_D [pH]	29.0	34.0
C_{gm} [fF]	23.0	27.0
L_G [pH]	$16.6 + 0.24 \cdot W_G/N$	
L_S [pH]	$20/(N/2+1)$	
C_{dm} [fF]	$5.88 + 0.25 \cdot N/2 + 0.026 \cdot N \cdot W_G$	
C_{gd} [fF]	$39/240 \cdot N \cdot W_G$	
C_{ds} [fF]	$62/240 \cdot N \cdot W_G$	
R_S=R_D [Ω]	$350/(N \cdot W_G)$	
R_G [Ω]	$0.088 \cdot W_G/N$	
r_i [Ω]	$3.3 \cdot 240/(N \cdot W_G)$	
τ [ps]	0.65	
C_0 [fF]	$3.7610^{-14} N W_G/240$	
C_1 [fF]	$4.6410^{-13} N W_G/240$	
C_2 [fF]	$1.9910^{-13} N W_G/240$	
a [1/V]	1.27	
b [1/V]	5.71	
V_m [V]	0.21	
V_p [V]	0.063	
$\alpha_d = \alpha_{dg}$ [1/V]	$q/(1.6\ k_B T)$	

Table C.2: Elements of the non-linear equivalent circuit of figure 6.11. The voltage dependence of the feedback capacitance c_{gd} and impact ionization are neglected. N is the number of gate fingers with a width of W_G per finger in micrometers.

$$C_{gs} = NW_G\left(C_0 + (C_1 - C_0)\frac{1 + tanh(a(V_{gs} + V_m)))}{2} - C_2\frac{1 + tanh(b(V_{GS} + V_p)))}{2}\right)$$

$$I_{gs} = NW_G(1.35\ 10^{-16} \cdot (e^{\alpha_d V_{gs}} - 1)$$

$$I_{gd} = NW_G(1.35\ 10^{-16} \cdot (e^{\alpha_{dg} V_{gd}} - 1)$$

C.4 Common source and cascode amplifiers

A single FET based common source amplifier as shown in the left part of figure C.2 provides a high voltage gain which is calculated to A_v = -S r_{ds} with the transconductance S of the active device, its output resistance r_{ds} and the power supply resistance R_{DD}. Limited only by the parasitic parallel resistors of the non-ideal Schottky contact, the common source amplifier has a high input resistance. The output resistance r_o is formed by the parallel circuit of R_{DD} and r_{ds}.
While the common source configuration satisfies high gain requirements, there is one main drawback limiting the high frequency response due to the presence of the feedback capacitance c_{gd}. Using Miller's Theorem, the capacitance c_{gd} may be split into two parts connected to the input and the output of the amplifier as shown in the middle of figure C.2. The Miller capacitances c_M are given by $c_{gd}(1+|A_v|)$ at the input and the output by $c_{gd}(1+1/|A_v|) \approx c_{gd} \stackrel{!}{=} c_M$ for a high voltage gain. Due to the high voltage gain, the equivalent input capacitance formed by c_{gs} and $c_M(1+|A_v|)$ is very large and results in a low high frequency pole given by equation C.2.

$$p_1 = \frac{1}{R_{in} \cdot c_{gs} \| [c_{gd}(1+|A_v|)]} = \frac{1}{R_{in}(c_{gs} + c_{gd}|A_v|)} \tag{C.2}$$

In order to improve the high frequency properties, a cascode amplifier as sketched in the right part of figure C.2 may be employed.

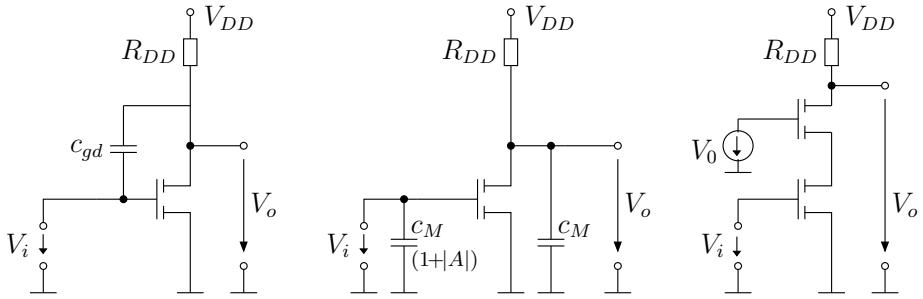


Figure C.2: Equivalent circuit of a FET in common source (l) configuration showing the Miller capacitance c_{gd} and its equivalent circuit (m) separating c_{gd} in $c_M(1+|A|)$ at the input and c_M at the output; (r) two FETs in cascode configuration compensating the Miller effect.

Due to the series of a common source and common gate transistor, the output resistance seen by the common source stage is given by the common gate device to $R_L \approx 1/S$. With this, the voltage gain of the common source device is reduced to A_{cs} = $S\,(r_{ds} \| R_L) \approx 1$, and the Miller capacitance at the input of the common source FET is reduced to approximately 2·c_{gd}. Due to the constant potential at the gate of the second FET, the internal feedback capacitance c_{gd} is grounded well with respect to the input of the common gate device, and the Miller effect has only little impact on the output of the amplifier. The low voltage gain of the common source stage is compensated by the common gate device, and the cascode amplifier provides a similar voltage gain and input resistance as the common source approach. Due to the compensation of the Miller effect, the high frequency pole is pushed to higher frequencies. The improvement of the high frequency performance, however, is linked to a more complex amplifier design.

Glossary

A	Material parameter for critical layer thickness
A^-	Conjugate base of generic acid
A_{cs}	Voltage gain related to a common source amplifier stage
a_i	Incident normalized wave of index i
A_ν	Voltage gain
A_s	Finite surface element
b	Material parameter for critical layer thickness
b_i	Reflected normalized wave of index i
C	Noise correlation coefficient
c	Speed of light in vacuum
$c(\mathrm{A}^-)$	Concentration of generic conjugate base
C_{dm}	Large signal model: metallic capacitance of drain pad
C_{sm}	Large signal model: metallic capacitance of source pad
C_{ds}	Large signal model: drain to source capacitance
c_{ds}	Intrinsic drain to source capacitance
c_f	Feedback capacitance of 2x75μm test device
C_{gd}	Large signal model: bias dependent gate to drain capacitance
c_{gd}	Intrinsic gate to drain capacitance
C_{gm}	Large signal model: metallic capacitance of gate pad
C_{gs}	Large signal model: bias dependent gate to source capacitance
c_{gs}	Intrinsic gate to source capacitance
$c(\mathrm{H_3O^+})$	Oxonium concentration
$c(\mathrm{HA})$	Concentration of generic acid
c_{im}	Capacitance to describe frequency response of impact ionization
c_{in}	Input capacitance of 2x75μm test device
c_M	Miller capacitance
c_{out}	Output capacitance of 2x75μm test device
C_p	Parallel capacitance
Cp	Specific heat
C_{pDS}	Drain to source pad capacitance
C_{pGD}	Gate to drain pad capacitance
C_{pGS}	Gate to source pad capacitance
D	Drain contact
$d^\star$	Effective distance between the gate electrode and the 2DEG
D_{2D}	Density of states in the 2DEG
d_b	Barrier thickness
d_{gc}	Distance: drain to channel
D_H	High electric field diffusion constant
e	Elementary charge
E_a	Activation energy
E_c	Conduction band energy level
E_{crit}	Critical electric field for ionization

E_f	Fermi energy
E_g	Semiconductor band gap
E_i	Eigenenergy i in quantum well
E_v	Valence band energy level
E_{vol}	Variation of energy per volume element
E_x	Electric field in x-direction
F	Noise factor
f	Frequency
F_{crit}	Critical indentation force to cause pop-in events
F_∞	Noise factor of infinite amplifier chain
f_{max}	Maximum oscillation frequency
F_{min}	Minimum noise figure
F_n	Noise figure of n-stage amplifier
f_T	extrinsic transit frequency
f_{Tc}	Transit frequency calculated from g_{me} & $c_{gs} + c_{gd}$
f_{Tgs}	Transit frequency calculated from g_{me} & c_{gs}
f_{T_i}	Intrinsic transit frequency
F_z	Indentation force
G	RF-gain
G	Gate contact
G_A	Available gain
G_{ass}	Associated gain
G_l	Gain of amplifier stage l
G_m	Transconductance
gm	Small signal transconductance
G_{max}	Maximum transconductance
g_{me}	Small signal transconductance of 2x75μm test device
gm_{im}	Transconductance due to impact ionization
G_p	Large signal (power) RF-gain
G_t	Transducer gain
$\hbar$	Planck's constant
$\|h_{21}\|^2$	Current gain
HA	Generic acid
h_c	Critical thickness
h_{TE}	Critical substrate thickness regarding TE-surface mode propagation
I	Intensity
I_{D_0}	Bias drain current
I_{ds}	Drain current under RF
I_{DS^+}	Maximum saturation drain current
$\mathrm{I}_{D_{max}}$	Maximum saturation drain current
I_{DSS}	Saturation current at zero gate voltage
I_{im}	Impact ionization current
$\Im(x)$	Imaginary part of x
I_{nd}	Noise current related to intrinsic drain resistance
I_{ng}	Noise current related to intrinsic gate resistance
I_{nL_x}	Noise current across the non-ideal Schottky barrier

I_{nR_D}	Noise current related to drain resistance
I_{nR_G}	Noise current related to gate resistance
I_{nR_S}	Noise current related to source resistance
I_{ns}	Noise current related to intrinsic source resistance
k	Rollet stability factor
k_x	Wave vector in x-direction
L_D	Drain inductance
L_d	Extension of the drift zone
L_G	Gate inductance
L_g	Gate length
L_K	Decoupling inductance
L_p	Parallel inductance
L_R	Size of the drain side gate recess
L_S	Source inductance
L_s	Extension of the saturation zone
L_x	Transfer length between drain and source
M	Noise number
$MS(A)G$	Maximum stable (available) gain
MTF	Mean time to failure
MUG	Maximum unilateral gain
m_x	Effective electron mass in x-direction
N	Number of gate fingers
N_b	Effective doping level in barrier
N_d	Noise power of the device
N_F	Noise figure
N_i	Power of intrinsic noise
N^+	Cap layer doping level
N_R	Charge density below the gate recess
N_s	Charge density of 2DEG
n_s	Hall charge density of epitaxy wafer
$n_s(x)$	Channel charge density at position x
N_{WR}	Charge density below the wide recess
P	Constants of noise model
P_{1dB}	RF-output power at 1dB compression
PAE	Power added efficiency
P_d	Dissipated power
P_{DC_0}	DC-power loss at quiescence operation bias
pK_{s_i}	Logarithmic acid constant of dissociation level i
P_o	Maximum RF-output power
$P_{RF_{lin}}$	Maximum linear RF-output power
P_{sat}	Saturated RF-output power
R	Constants of noise model
r_0	Lattice constant of the crystal
R_{ac}	Access resistance

R_{co}	Ohmic contact resistance
R_D	Drain resistance
R_{DD}	Supply resistor
R_{ds}	Drain to source noise resistance
r_{ds}	Intrinsic drain to source resistance
$\Re(x)$	Real part of x
r_f	Feedback resistance of 2x75μm test device
RG	Resistance of a 100μm gate line
R_G	Gate resistance
R_{gd}	Gate to drain noise resistance
r_{gd}	Intrinsic gate to drain resistance
R_{gs}	Gate to source noise resistance
R_i	Isolation resistance on test structure
r_i	Intrinsic gate to source resistance
r_{im}	Resistance to describe frequency response of impact ionization
R_{in}	Input load
r_{in}	Input resistance of 2x75μm test device
R_L	Load resistance
rms	Root mean square roughness
R_n	Normalized noise resistance
r_o	Output resistance of an amplifier
R_{out}	Output resistance of 2x75μm test device
$r_{\parallel gd}$	Parallel gate to drain resistance
$r_{\parallel gs}$	Parallel gate to source resistance
R_S	Source resistance
R_{sh}	Sheet resistance of epitaxy wafer
R_{th}	Equivalent thermal resistance
S	Transconductance
S	Source contact
S_i	Power of intrinsic signal
S_{ID}	Noise power density
s_{ij}	Scattering parameter of indices ij
T	Temperature
T_0	Ambient temperature
t_{eff}	Effective depth
TG	Average temperature in a 100μm gate line
E_ϑ	Thermal energy
T_L	Lattice temperature
T_{xx}	Noise temperature of noise resistance xx
V_{acc}	Acceleration voltage
V_{bDS}	Tree terminal(device) breakdown voltage at 1% of I_{DSS}
V_{bGD}	Two terminal breakdown voltage of the gate-drain diode at 1mA/mm
V_{DD}	Supply voltage
V_{DS}	Drain voltage
v_{ds}	Intrinsic drain voltage
V_{DS_0}	Bias drain voltage
$V_{DS_{max}}$	Maximum drain voltage

V_{G100}	Gate voltage at 1% of I_{DSS}
V_{gBD}	Gate voltage applied for three terminal breakdown voltage
V_{GS}	Gate voltage
v_{gs}	Intrinsic gate voltage
V_{knee}	Knee voltage
V_p	Pinch off voltage
v_{sat}	Saturation drift velocity
V_{th}	Threshold voltage
$v(x)$	Electron velocity at position x
$V(z)$	Electrostatic potential at position z
W	Total gate width
W_G	Width of one gate finger
x	x-coordinate or ratio of material composition
X_D	Extension of the depletion zone
y_{ij}	Admittance parameters of indices ij
Z_0	Wave resistance
z	z-coordinate or indentation depth
α_n	Electron ionization coefficient
β	Fitting factor
δ	Delta doping level
ΔL_T	Increase of the transfer length
ΔE_c	Conduction band discontinuity
ΔE_v	Valence band discontinuity
ΔT	Temperature increase
ΔV_G	Voltage drop across 100μm long gate line
Δ_y	Undercut of gate recess
$\Delta(z)$	Widening of electron beam at depth z
ε_0	Electri constant
ε_b	Dielectric constant of barrier layer
ε_r	Dielectric number
η_A	Efficiency
Φ	Energetic flux
Φ_b	Schottky barrier height
γ	Exponent
$\Gamma_{L,G}^{(i)}$	Reflection coefficient of load or generator at reference plane i
Γ_{opt}	Optimum noise reflection coefficient
κ	Thermal conductivity
λ	Wave length
μ	Hall electron mobility of epitaxy wafer
μ_n	Low electric field electron mobility
ω	Angular frequency
Ψ	Wave function
ρ	Material density
τ	Delay time
$\tau_{\omega n}$	Electron energy relaxation time
ζ_i	Solution of the Schrödinger equation for eigenvalue i

Abbreviations

AFM	Atomic force microscope
ATLAS	Device simulation software, SILVACO
ADS	Electronic design software: Advanced design system, Agilent
ANSYS	Finite element software: Analysis system, ANSYS Inc.
BCB	Benzocyclobutene
CCD	Closed caption display
2DEG	Two dimensional electron gas
DD-model	Drift diffusion model
DUT	Device under test
EDX	Energy dispersive X-Ray spectroscopy
FET	Field effect transistor
HD-model	Hydro dynamic model
FFSS	Finite element software: High frequency structure simulation, Ansoft
HMDS	Hexamethyldisilazane
HPA	High power amplifier
IAF	Fraunhofer Institut Angewandte Festkörperphysik, Thullastrasse 72, 79108 Freiburg i. Br., Germany
ICP	Inductively coupled plasma
IEMN	Institut d'Electronique, de Microélectronique, et de Nanotechnologie, Lille, France
IMPATT	Impact ionization avalanche transit time
IRCOM	Institut de Récherche en Communication Optique et Microonde, 123 Rue Albert Thomas, Limoges 87060 Cedex, France
JFET	Junction gate field-effect transistor
LNA	Low noise amplifier
MBE	Molecular beam epitaxy
mHEMT	Metamorphic high electron mobility transistor
MilliLab	Millimeter Wave Laboratory of Finland, Tietotie 3, Otaniemi, Espoo, Finland
MIM	Metal-insulator-metal capacitor
MOCVD	Metal-organic vapor phase deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTF	Mean time to failure
PBE	Parasitic bipolar effect
PMMA	Poly methyl methacrylate
PMGI	Poly methyl glutarimide
pHEMT	Pseudomorphic high electron mobility transistor
RHEED	Reflection high energy electron diffraction
RIE	Reactive ion etching
SEM	Scanning electron microscope
SA	Succinic acid
SL-buffer	Superlattice buffer
TE	Transverse electric
UMS	United Monolithic Semiconductors - GmbH: Wilhelm-Runge-Strasse 11, 89081 Ulm, Germany - SAS: Route départementale 128, BP46, 91401 Orsay Cedex, France
XLith	Extreme Lithography, Wilhelm-Runge-Strasse 11, 89081 Ulm, Germany

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Acknowledgement

I would like to thank Professor Dr.-Ing. Erhard Kohn very much for supervising and supporting this industrial work and for many skilled advice.

I would like to acknowledge the close collaboration with IEMN for device simulation and characterization, particularly Professor Ph.D Cristophe Gaquière and Ph.D Didier Théron. I am indebted to my Colleagues of UMS-Orsay, Ph.D Alexandre Bessemoulin and Ph.D T. Huet for low noise and power amplifier demonstrator design and Ph.D Philippe Fellon supporting device characterization and modeling. I further would like to thank Ph.D Raphaël Sommet from IRCOM for thermal simulation of the metamorphic and pseudomorphic HEMT structures.

I would like to thank C. Wölk from the Daimler-Research group who provided me the 3" metamorphic epitaxy wafers. Furthermore, I would like to thank Dr Bernd Maile from XLith and Hüsyin Sahin from UMS-Ulm for Monte Carlo simulations and support in electron beam lithography during the development phase of the gate technologies. I had the pleasure of sharing may office with Dr Helmut Jung and would like to thank him for numerous suggestive discussions.

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