A 64–84-GHz PLL With Low Phase Noise in an 80-GHz SiGe HBT Technology

Gang Liu, *Member, IEEE*, Andreas Trasser, and Hermann Schumacher, *Member, IEEE*

***Abstract*—This paper presents a 64–84-GHz phase-locked loop (PLL) realized in a low-cost 80-GHz HBT technology. The circuit consists of a wide tuning-range voltage-controlled oscillator, a push–push frequency doubler, a divide-by-32 frequency divider, a phase detector and an active loop filter. The measured phase noise at 1-MHz offset is −106 dBc/Hz. The output power is −2.5 dBm at 64 GHz, and it slowly decreases to −8.1 dBm at 84 GHz, with a maximum dc power consumption of 517 mW. To the authors' knowledge, the circuit achieves the widest frequency tuning range and its in-band phase noise is the lowest among the fully integrated V/W-band PLLs reported to date.**

***Index Terms*—Heterojunction bipolar transistors (HBTs), millimeter-wave (mm-wave) integrated circuits (ICs), phase-locked loops (PLLs).**

I. Introduction

HIGHLY stable frequency sources are a key requirement of many millimeter-wave (mm-wave) communication and sensing systems. Stability is typically achieved using a phase-locked loop (PLL) approach, tying the mm-wave output to a lower reference frequency. With emerging applications in communications at 60 GHz and radar at 77 GHz, V/W-band signal sources are in high demand. Owing to their potential for highly complex multifunctional integrated circuit (IC) implementations, Si/SiGe heterojunction bipolar transistor (HBT), Si/SiGe BiCMOS and ultra-scaled CMOS have made silicon the predominant platform for integrated synthesizer developments. Aside from phase noise and output power, tuning range is another important parameter, either because the application requires it (e.g., high-resolution frequency-modulated continuous wave (FMCW) radar) or because it provides the flexibility to use the synthesizer for a number of different applications. In sensor applications, the tuning speed is often another critical challenge.

A review of published wideband integrated synthesizers with output frequencies in the 60–100-GHz frequency range shows a significant variety of approaches. The voltage-controlled oscillator (VCO) may oscillate directly at the frequency of operation, or a lower frequency VCO may be used with subsequent frequency multiplication [1] (and also this paper). Alternatively, a low-frequency PLL-stabilized VCO may be up-converted using an injection-locked oscillator at the higher frequency of operation [8]. To achieve a very wide tuning range, CMOS and BiCMOS synthesizers use switched MOS varactors, usually via a 3-bit digital control word [2], [3], or even multiple VCOs on one chip [5]–[8].

The choice of loop bandwidth and divider ratio between the frequency of operation and the reference frequency affects phase noise, but also locking range (for analog PLLs) and locking speed. Most of the surveyed PLLs use small loop bandwidths, 4 MHz or below, down to 100 kHz [1]–[3], [5]–[8], and only [4] uses a large loop bandwidth (45 MHz) comparable to the design presented here. Most of the designs [1]–[3], [5], [7], [8] also use rather high divider ratios, between 768–8184. Only [4] and [6] use low divider ratios, 64 and 16, respectively, comparable to the work presented here. Low divider ratios lead to low phase noise, provided that a stable reference source is available. The dividers use injection-locked [5] dynamic and static division principles. In case of the injection-locked divider, it imposes a limitation on the tuning range of the synthesizer.

All reviewed designs, finally, use a charge pump in the loop. This is a common approach, but requires fast pnp or pMOS devices.

A tabular overview of the reviewed designs, along with results of the synthesizer presented here, is shown in Table I.

The design reported here had the following objectives.

- Frequency of operation very close to the technology $f_{\max}$. This is, on the one hand, motivated by the need of very low-cost front-end ICs for consumer applications at 60 GHz, and on the other hand, provides valuable insight into design techniques capable of addressing sources for systems operating much above 100 GHz.
- Very wide tuning range. This is motivated by the need to address several applications with one synthesizer IC.
- The ability to sweep over a wide frequency range without band switching, as needed by high-resolution FMCW sensors.
- Fast settling time for applications requiring high-frequency agility.
- State-of-the-art phase-noise suppression despite the partially conflicting requirements above.

Specifically, an approach was chosen that uses a moderate divider ratio (64 with respect to the frequency of operation) to lower phase noise, a loop bandwidth of 50 MHz for large

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The authors are with the Institute of Electron Devices and Circuits and the Competence Center on Integrated Circuits in Communications, Ulm University, 89081 Ulm, Germany (e-mail: gang.liu@uni-ulm.de; andreas.trasser@uni-ulm.de; hermann.schumacher@uni-ulm.de).

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TABLE I
COMPARISON OF RECENT mm-WAVE PLLs

Ref.	Technology f_T/f_{max} (GHz)	Tuning Range	Division Ratio	Loop Bandwidth	PN @1MHz	Spur (dBc)	Output Power (dBm)	DC mW	Chip Size mm^2
[1] *TMTT* 12	0.18μm BiCMOS 200/180	90.9 - 101.4 (10.9%)	768	4 MHz	-92	-52	-	140	1.9
[2] *TMTT* 11	65nm CMOS -/-	70 - 78 (10.8%)	1024 to 1984	100 KHz to 1 MHz	-83	-49	-	65	0.16 [1]
[3] *JSSC* 11	65nm CMOS -/-	58 - 63 (8.3%)	1620 to 1984	4 MHz	-95	-67 to -58	-10	80	-
[4] *RFIC* 11	0.13μm BiCMOS 230/-	92.7 - 100.2 (8.3%)	64	45 MHz	-102	-60	3	570	1.1 x 1.1
[5] *TMTT* 11	90nm CMOS -/-	60.2 - 62.4 (3.6%) 81.3 - 83.3 (2.4%)	768 1024	700 KHz	-70 -72.5	-36 -52	-9.5 -7.34	106.6 109.9	1.5 x 0.75
[6] *JSSC* 11	0.13μm BiCMOS 230/280	86 - 92 (6.7%) 80 - 100 (22.2%) [2]	16	1 MHz to 10 MHz	-100	-	-3	1150 to 1250 [3]	1.7 x 1.1
[7] *JSSC* 09	0.18μm BiCMOS 200/180	75.67 -78.5 (3.7%)	768	4 MHz	-103.5	-47.8	-17.8	75	1 x 0.8
[8] *ISSCC* 09	45nm CMOS -/-	57 - 66 (14.6%)	512 - 8184	1 MHz	-75	-42	-	78	0.99 x 0.83
This	**0.8μm SiGe HBT 80/90**	**64 - 84 (27%)**	**64**	**50 MHz**	**-106**	**-37**	**-2.4@64 GHz -8.1@84 GHz**	**432 to 517 [4]**	**1 x 1.1**

[1] core area, [2] total range of two VCOs under differential biasing conditions, [3] with two VCOs and programmable division ratios (/16, /32/, /64, /128), [4] depending on the loop filter supply voltage.

locking range and fast settling time, and an analog PLL without a charge pump.

The circuit was first discussed briefly in [9]. This paper is an extended version, describing the design, simulation, and characterization in more details.

II. TECHNOLOGY OVERVIEW

For realizing the PLL circuit, we used an SiGe HBT technology [10] from Telefunken Semiconductors GmbH. The process requires only 22 masks with 0.8-μm minimum feature size, and therefore, is very cost effective. Two types of npn transistors are available with minimum geometric emitter size of 0.8×1.4 μm^2 (electrically active emitter size of 0.5×1.1 μm^2). The selectively implanted collector (SIC) npn transistor has an $f_T/f_{\max}$ of 80/90 GHz and a BV_{CEO} of 2.4 V. The non-SIC transistor improves the BV_{CEO} to 4.5 V, with a reduced f_T of 50 GHz. One type of lateral pnp (LPNP) transistor is also available, but not suitable for RF purposes. Four types of resistors, metal–insulator–metal (MIM) and nitride capacitors, as well as varactor diodes are provided. The process offers three metal layers for passive elements and interconnections. Two types of silicon substrate (1000 and 20 $\Omega \cdot$ cm) are available. The low-resistivity substrate is chosen for this study.

III. PLL CIRCUIT DESIGN

The block diagram of the PLL circuit is shown in Fig. 1. It is an analog PLL incorporating a phase detector (PD) and active loop filter (LF). Compared to the commonly used digital PLL employing a phase frequency detector (PFD) and charge pump, the analog PLL can operate at much higher frequencies, enabling a smaller frequency division ratio in the PLL, and therefore, lower phase noise.

A. VCO and Doubler

The signal generation is realized by a VCO and a frequency doubler, which is a modified version of the work reported earlier [14]. Fig. 2 shows the schematic of the VCO and frequency doubler. The VCO is a differential Colpitts VCO with a cascaded common base stage as the output buffer. It provides two differential outputs to drive the frequency doubler and divider in parallel. Large transistors (0.5×30 μm^2) are used in the VCO core and output buffer because they can generate more output power and have smaller base resistance (compared to small transistors), facilitating oscillation at higher frequency and resulting in lower phase noise [11]. The inductors and all matching networks are realized with thin-film microstrip lines (TFMLs). The oscillation frequency is tuned through varactor diodes.

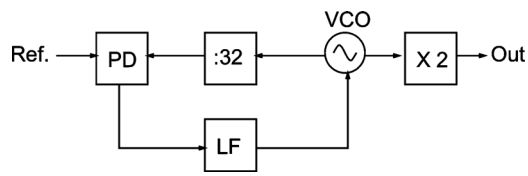


Fig. 1. Block diagram of the PLL circuit.

The oscillation frequency of the VCO can be calculated as

$$f_{\mathrm{osc}} = \frac{1}{2\pi\sqrt{L_B C_{\mathrm{eq}}}} \tag{1}$$

where L_B is the base inductance and C_{eq} is the equivalent capacitance of C_{VAR}[1] in series with the transistor base–emitter junction capacitance C_{be}.

To have a wide frequency tuning range, C_{VAR} should be much smaller than C_{be}. However, a very small C_{VAR} cannot produce sufficient negative impedance to start the oscillation. Therefore, in this design, C_{VAR} is in the same range as C_{be} (about 350 fF), as a compromise between wide tuning range and sufficient negative impedance. Three diodes with the smallest size (20-μm strip length and 1.8-μm strip width) are connected

[1] C_{VAR} is the equivalent capacitance of the varactor diodes in parallel with the 800-μm TFML. The capacitance is mainly determined by the varactor diodes, as the TFML is a very large inductor (close to an open at the frequency range of operation) and has little influence on the capacitance.

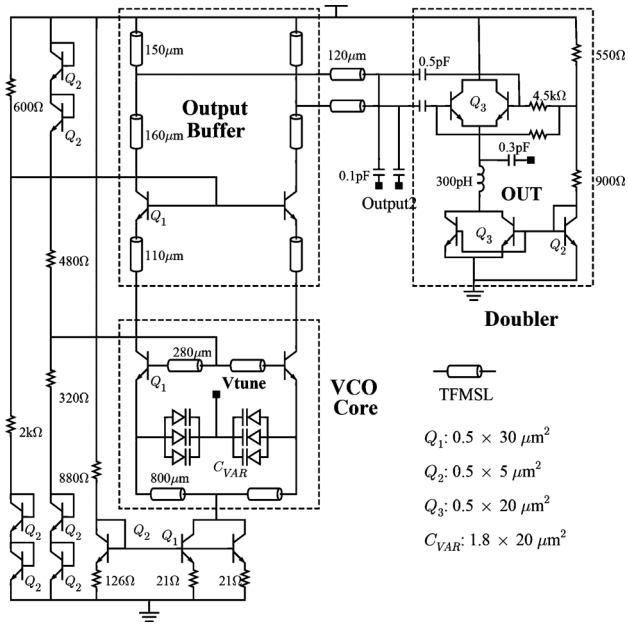


Fig. 2. Schematic of the VCO and frequency doubler.

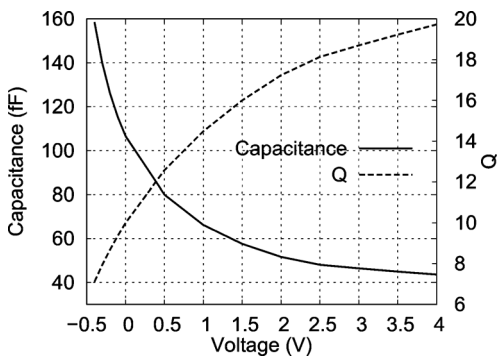


Fig. 3. Capacitance and quality factor of a single varactor diode (at 30 GHz).

in parallel to improve the quality factor. The capacitance of a single varactor diode changes from 43 to 107 fF, when the dc voltage across the varactor varies from 4 to 0 V. The quality factor at 30 GHz changes from 20 to 10, as shown in Fig. 3. The capacitance can be further increased to 158 fF with slight forward biasing $(-0.4\ \mathrm{V})$. This is helpful to achieve a wider tuning range, although the phase noise gets slightly worse. In this design, the slightly higher phase noise of the free-running VCO is not critical because it is well suppressed within the loop bandwidth and already decreases to a sufficiently low level at high offset frequencies (outside the loop bandwidth, >50-MHz offset).

The oscillation frequency can be continuously tuned from 31 to 42 GHz. Since the frequency divider requires only a very small input power, the VCO output is modified such that most of the power (5 dBm) is delivered to the frequency doubler and about 0 dBm to the frequency divider.

The frequency doubler is a push–push type, based on an emitter coupled pair (ECP), as shown in Fig. 2. This type of frequency doubler can provide higher conversion gain, compared to the passive frequency doublers, and it requires less chip area than the nonlinearity type of frequency doublers because no specific filter and matching networks is needed at the input and output. Frequency doublers based on the push–push topology have been reported [12], [13], operating at relatively low frequencies (compared to $f_{\max}$). In this study, the frequency doubler is operated at frequencies close to $f_{\max}$. Therefore, the topology is modified to have better performance in the designed frequency range. The output is taken from the common emitter, with a 300-pH inductor as the load, which provides higher conversion gain than a resistive load (as in [12]). The ECP is biased for class-A operation using a current source. Compared with class-B operation (as in [13]), the conversion gain and output power is higher at high input levels (>0 dBm). With 7-dBm input power, the conversion gain peaks at 30-GHz output (-5 dB) and slowly decreases to -10 dB at 80 GHz. Further details of the VCO and frequency doubler are provided in [14].

B. Frequency Divider

Frequency dividers are also important building blocks in modern PLLs. They decrease the input frequency from the VCO so that the PLL can operate at much lower frequencies. However, the in-band phase noise of the locked signal will be increased by a factor of $20\cdot\log(N)$, where N is the frequency division ratio. Therefore, a small frequency division ratio is preferred to obtain a lower phase noise. In this study, a division ratio of 32 (for fundamental VCO) is chosen, which lowers the reference signal to a relatively low frequency (around 1.1 GHz) and still provides good phase-noise performance.

The divide-by-32 frequency divider consists of five divide-by-2 stages. To get a wide tuning range PLL, the frequency divider should operate properly over the complete frequency tuning range of the VCO. The dc power consumption should also be minimized. Therefore, each divide-by-2 stage is designed and optimized separately balancing maximum operating frequency and power consumption.

The first divider stage is the most critical one because it operates at the highest frequency. The maximum VCO output frequency is 42 GHz so the first divider stage should operate at least up to 42 GHz (better up to higher frequency to keep some safety margins). Static frequency dividers based on master–slave D-flip-flops (DFFs) cannot operate at this frequency range due to the high ratio of operating frequency and f_T. Injection-locked frequency dividers (as used in [2] and [3]) can operate at higher frequency, but they all rely on introducing additional phase shift to an oscillator to achieve locking [15], therefore usually have limited operating frequency range. In this design, a dynamic frequency divider is used as the first stage. It is based on the regenerative concept [16], as shown in Fig. 4(a). The output of the mixer, after passing the low-pass filter and amplifier, is fed back to one input of the mixer. When an input signal at frequency f_{in} with a certain power is applied to the other input of the mixer, the divider will sustain an oscillation within the loop at frequency $f_{\mathrm{in}}/2$, provided that the higher mixing products ($3f_{\mathrm{in}}/2$, $5f_{\mathrm{in}}/2$, etc.) are filtered out by the low-pass filter. The operation of the dynamic divider relies on the mixer and low-pass filter, which can have very wide bandwidth so the dynamic frequency divider can operate over a

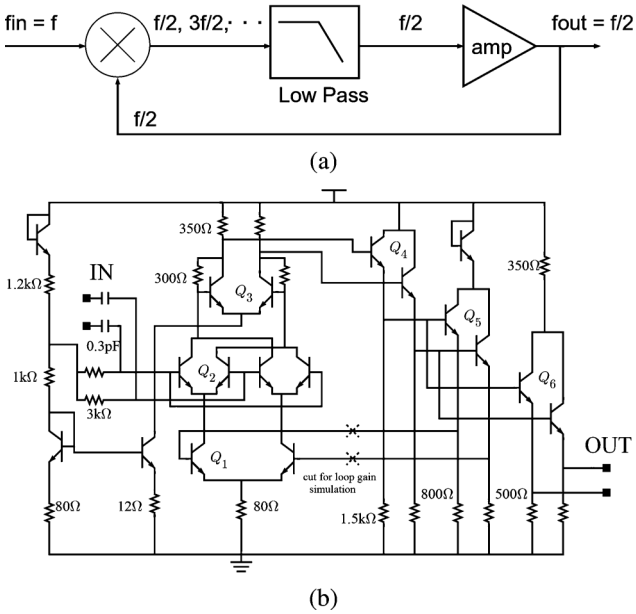


Fig. 4. (a) Regenerative frequency divider principle. (b) Schematic of the dynamic divider (first stage). All transistors have the same electrically active size of $0.5 \times 5\ \mu\text{m}^2$.

much wider frequency range than the injection-locked dividers. Fig. 4(b) shows the schematic of the dynamic divider, consisting of a Gilbert-cell mixer core (Q_1, Q_2), a transimpedance amplifier (TIA) stage (Q_3) and emitter-followers (EFs) as low-pass feedback (Q_4, Q_5) and output buffer (Q_6).

The transimpedance stage increases the mismatch in the loop, leading to wider bandwidth and much better performance (with respect to maximum operating frequency, safe broadband operation, and high sensitivity), compared with a single resistor as the load [17]. Small transistors ($0.5 \times 5\ \mu\text{m}^2$) are used in the mixer core and TIA for low current consumption. The maximum operating frequency of the dynamic divider is determined by the open-loop gain. To calculate the open-loop gain, the divider feedback loop is cut at the output of the second EF (Q_5), as indicated in Fig. 4. One input signal at frequency f_o is injected into the divider from the input port (base of Q_2) and another signal at frequency $f_o/2$ is injected into the base of Q_1.[2] The open-loop gain can be calculated as the power gain from the input at Q_1 to the output at Q_5. Fig. 5 shows the simulated open-loop gain under small-signal driving condition.[3]

The maximum operating frequency of the dynamic divider is twice the frequency at which the open-loop gain drops to 1. By adjusting the resistors in the TIA and EFs, the open-loop gain can be maximized. In this design, the maximum operating frequency is intentionally reduced from 70 to 50 GHz to save dc power consumption (by increasing the load resistor in the TIA and reducing the current in the EFs). The dynamic divider stops dividing at low frequencies (<10 GHz) because the third harmonic in the mixer output signal is not sufficiently suppressed in the feedback loop [17]. Therefore, it is not suited for frequency division at very low frequencies.

[2]Dummy EFs (same as Q_4–Q_6) are inserted before Q_1 and the output of Q_5 is terminated with a dummy mixer core to represent the same matching conditions in the closed loop.

[3]As the signal level at Q_1 increases, the loop gain slowly decreases due to nonlinearity of the transistors.

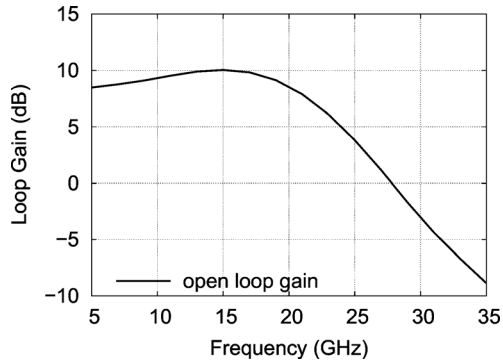


Fig. 5. Simulated open-loop gain of the dynamic divider.

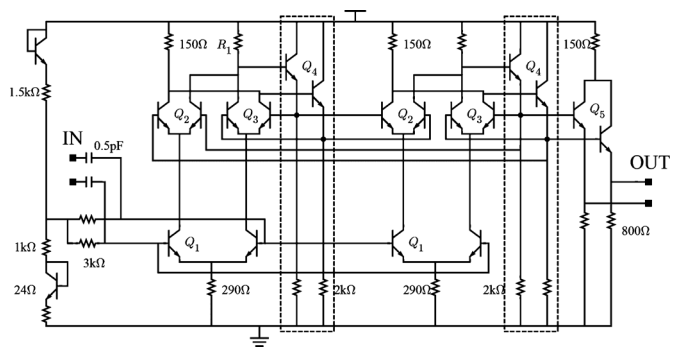


Fig. 6. Schematic of the static divider (second stage). Q_1: $0.5 \times 1.1\ \mu\text{m}^2$. Q_2, Q_3: $0.5 \times 2\ \mu\text{m}^2$. Q_4, Q_5: $0.5 \times 5\ \mu\text{m}^2$.

The second stage is a static frequency divider based on master–slave DFFs, as shown in Fig. 6. The DFFs are built using emitter-coupled-logic (ECL) (Q_1 being the clock, Q_2, Q_3 being the latches). The EF (Q_4) provides the dc level shift (for proper biasing of Q_2, Q_3) and increases the speed (maximum operating frequency) of the divider. Q_2, Q_3, Q_4, and R_1 are the most critical elements that determine the speed of the static divider, as analyzed in [18] and [19]. By choosing the third smallest transistor ($0.5 \times 2\ \mu\text{m}^2$) for Q_2, Q_3, and 100 Ω for R_1, the speed of the divider can be maximized (about 34 GHz). However, such high speed for the second divider stage is not necessary. Therefore, the speed is reduced to 28 GHz by increasing R_1 and decreasing the current in Q_1 and Q_4. The dc power consumption is reduced by 50%.

The static divider can operate down to very low frequencies (megahertz range, limited by the on-chip capacitor). Therefore, it is also used for the following three stages. Since they operate at much lower frequencies, the speed of the following stages is further reduced to save dc power consumption. The EFs in the DFFs (indicated via the dashed box) are omitted, the current in Q_1 is reduced, and R_1 is increased to compensate the decrease of voltage swing due to the lower current. The output buffer (EF) is only added at the last output stage.

The operating frequency range and input and output power of each stage are designed carefully so that the divider chain can operate properly over the complete frequency range with low power consumption and sufficient output power. Fig. 7 shows

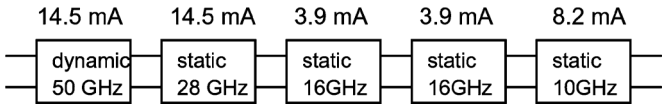


Fig. 7. Block diagram of the divide-by-32 frequency divider with the maximum operating frequency and dc power consumption (under 3.5-V supply) of each stage.

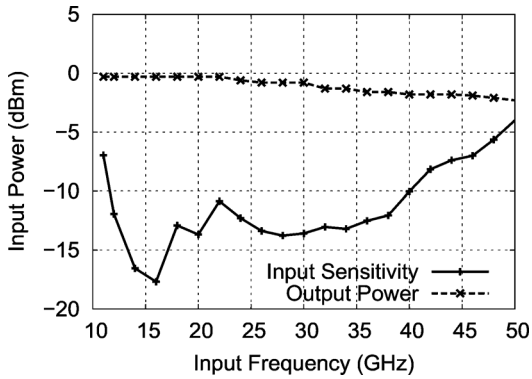


Fig. 8. Measured input sensitivity and output power of the divide-by-32 frequency divider.

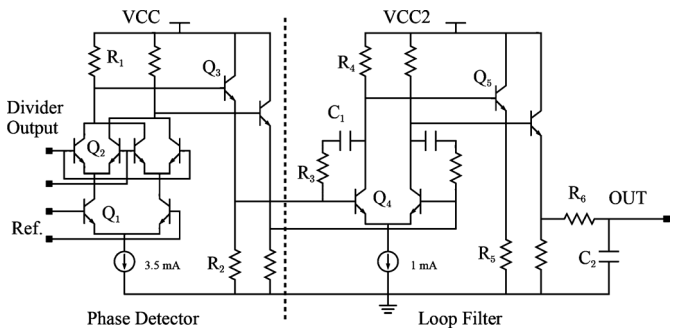


Fig. 9. Simplified schematic of the PD and active LF. All transistors have the same size of $0.5 \times 5\ \mu\text{m}^2$. R_1: 550 Ω, R_2: 800 Ω, R_3: 30 Ω, R_4: 2.5 kΩ, R_5: 1.2 kΩ, R_6: 400 Ω. C_1, C_2: 1 pF.

the block diagram of the divider chain with the maximum operating frequency and dc power consumption (under 3.5-V supply) of each stage. A standalone frequency divider has been realized for characterization. Fig. 8 shows the measured input sensitivity and output power. The divider chain can divide from 11 GHz up to 50 GHz, covering the complete tuning range of the VCO. The required input power (<-8 dBm) is well below the available power from the VCO and the output power is about -2 dBm, which is sufficient to drive the PD.

C. PD and LF

The PD is based on a Gilbert-cell mixer with resistive load, as shown in Fig. 9. The EF (Q_3) provides the dc level shift so that the PD can drive the following LF directly. The divider output is connected to the switching quad of the mixer core and the reference signal is connected to the transconductance stage.

When the two input signals are different in frequency (at the initial phase of the locking process), the PD operates as a mixer and generates a low-frequency signal, which tunes the VCO frequency toward the reference frequency. When the two input signals have the same frequency, but differ in phase (by $\Delta\phi$), as in the locked state, a dc voltage shift (ΔV) is produced at the output, fixing the VCO frequency at the reference frequency (multiplied by the division ratio N).

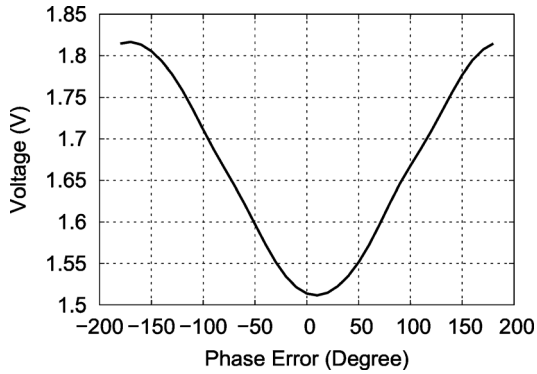


Fig. 10. Simulated PD output voltage versus phase error.

Fig. 10 shows the simulated output voltage of the PD versus the input phase error. The gain of the PD (K_D), defined as $\Delta V/\Delta\phi$, is mainly determined by the load resistor (R_1) and the reference signal power. As will be shown in Section IV, K_D influences the PLL loop gain and noise contribution from the PD, and thus needs to be chosen carefully. In the current design, the load resistor is 550 Ω and the PD gain is about 0.1 (with -15-dBm reference signal power).

In addition to the dc voltage shift, the output of the PD also contains ac signals, which are mixing products of the two input signals. These ac signals will modulate the VCO and generate spurs (reference spurs) around the locked signal, and must be sufficiently suppressed. The suppression of the ac signals on the tuning node (and hence, the spur signals at the PLL output) is determined by the LF attenuation at the spur frequencies (harmonics of the reference frequency), which can be controlled by the LF bandwidth. To have high spur suppression, a small bandwidth (low cutoff frequency) is preferred. However, a small LF bandwidth directly leads to small loop bandwidth, and hence, small frequency locking range and longer settling time of the PLL, so a compromise between spur suppression and locking range must be considered when choosing the filter bandwidth. In this design, a relatively wide bandwidth is chosen because wide locking range is the main design goal and the reference spurs are less critical since they are far from the locked signal.

The LF is also shown in Fig. 9. It is based on a feedback amplifier and passive *RC* filter with an EF in between for dc level shift. The amplifier amplifies the small control signal from the PD and performs low-pass filtering (though feedback) together with the *RC* filter. The bandwidth and attenuation (at high frequency, e.g., at 1 GHz) of the filter, which influence the PLL loop bandwidth and reference spur suppression, are mainly determined by the feedback (R_3, C_1) and the *RC* filter (R_6, C_2). Fig. 11 shows the simulated ac power gain of the filter. The 3-dB bandwidth is 47 MHz, which is a compromise between wide locking range (wide loop bandwidth) and spur signal suppression (smaller bandwidth).

The free-running VCO can be tuned from 31 to 42 GHz, which corresponds to a voltage tuning from 0.6 to 6 V. In order to lock the VCO to a wide frequency range, the LF output must be able to cover a wide voltage range. Since the output

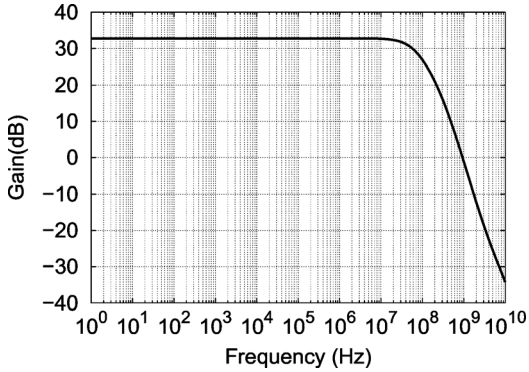


Fig. 11. Simulated ac gain of the LFs with different bandwidth.

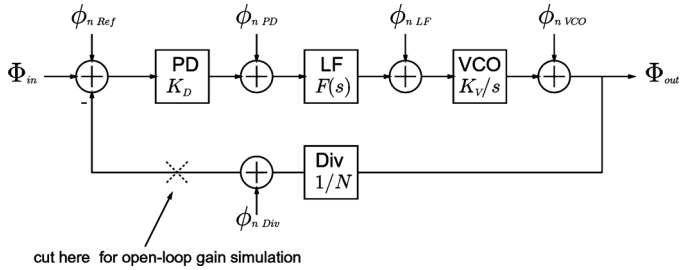


Fig. 12. Linear model of the PLL. The loop is cut at the output of the divider for open-loop gain simulation.

voltage swing of the PD is very small (0.13 V peak-to-peak at 30 MHz), the LF must provide sufficient gain to have a large output voltage swing, which also increases the gain of the PD and helps to suppress the noise contribution from the PD and LF, as will be shown in Section IV. The gain of the LF can be easily adjusted by changing the load resistor (R_4) and biasing current. With a load of 2.5 kΩ, the LF has 33-dB gain and 2.3-V (peak-to-peak) output voltage swing. This allows a maximum frequency tuning range of 4 GHz that is wider than the locking range determined by the loop bandwidth. Due to the high voltage swing, the non-SIC transistors (with 4.5-V BV_{CEO}) are used in the LF design.

The locking range of the PLL is limited by the loop bandwidth and covers only part of the VCO tuning range (about 3 GHz around the free-running frequency). Therefore, the usable frequency range of the VCO is limited. To cover the full tuning range of the VCO, the locking range can be shifted by adjusting the supply voltage of the LF ($VCC2$). The biasing current of the filter is fixed so that a change of the supply voltage only shifts the dc voltage level at the output node. As a result, the free-running frequency of the VCO, and hence, the locking range, can be shifted, while the loop response remains the same. By changing $VCC2$ from 2 to 8 V in steps of 1 V, the PLL can lock to different frequency bands, covering almost the whole tuning range of the VCO, as will be shown later in Section V.

IV. PLL Simulation

To assist and optimize the design of the PLL, different simulations have been performed. The PLL behavior in the locked state (loop gain, loop bandwidth, phase noise) is simulated in the frequency domain, based on a linear model, as shown in Fig. 12. The transient response of the PLL (locking time) is simulated in time domain using transient simulation (ADS), based on real circuit models.

A. Loop Gain Simulation

In the locked state, the PLL can be modeled by a linear model in the frequency domain, as shown in Fig. 12, where K_D, K_V, $F(S)$, and N are PD gain, VCO gain, LF transfer function, and frequency division ratio, respectively.

The open- and closed-loop gain are two important PLL design parameters, defining the PLL loop stability and bandwidth. The open-loop gain is the product of all the transfer functions in the loop $(K_D \cdot F(s) \cdot K_V / N \cdot s)$. To simulate the open-loop gain, the loop is cut at the output of the frequency divider, as shown in Fig. 12. The PD, VCO, and frequency divider are replaced with ideal behavioral models. The complete circuit model of the LF is used in the simulation since a behavior model could not be extracted. The simulation is performed in ADS using ac simulation. After feeding an input signal, the open-loop gain can be calculated as the gain from the input to the divider output.

The stability of the loop can be evaluated from the amplitude and phase of the open-loop gain. The phase margin[4] is usually used to define the stability of the PLL. In this PLL design, one effective way to control the phase margin is to tune the load resistor in the LF (R_4 in Fig. 9). Fig. 13(a) and (b) shows the simulated magnitude and phase of the open-loop gain for different load resistors. As the load resistor (R_4) decreases, the phase margin increases and the loop becomes more stable. However, decreasing R_4 also reduces the loop bandwidth and locking range. A 2.5-kΩ load resistor is used in the current design, which gives a good compromise between loop bandwidth and stability.

The closed-loop gain (also called the transfer function)

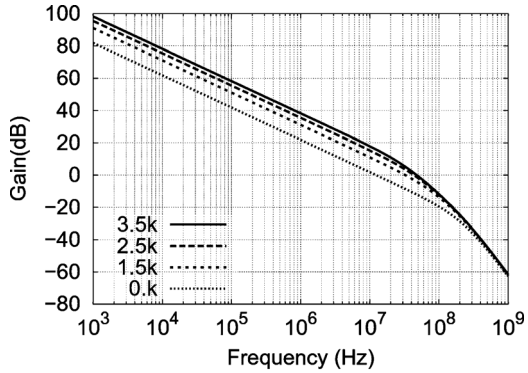
$$H(s) = \frac{N \cdot K_D \cdot F(s) \cdot K_V}{N \cdot s + K_D \cdot F(s) \cdot K_V} \tag{2}$$

defines the phase relation between the input and output. The performance of the PLL (locking range, spur suppression, etc.) is mainly determined by the closed-loop gain. Fig. 13(c) shows the simulated closed-loop gain for different load resistors.

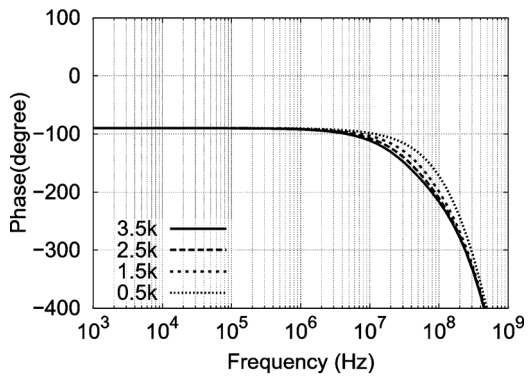
B. Phase-Noise Simulation

Phase noise is an important characteristic of a PLL. Ideally, the output phase noise should be the same as the phase noise of the reference signal plus $20 \cdot \log(N)$, where N is the frequency division ratio, as indicated in the closed-loop gain simulation. However, the noise of other loop components also contributes to the final output phase noise. Each component has its own transfer function. In the locked state, the PLL can be modeled as a linear system, where the total output noise is the sum of each noise source (from each component) multiplied by its own transfer function. In order to achieve the lowest possible phase noise, the noise from other loop components should be lower

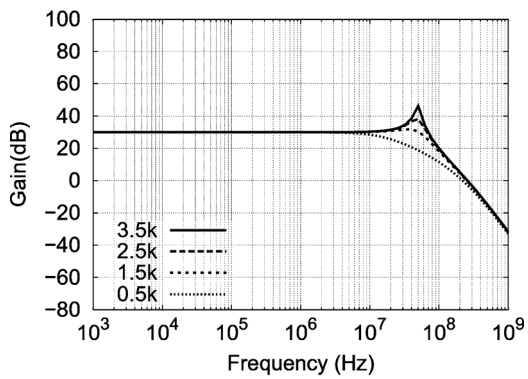
[4]The phase margin is the phase difference between 180° and the phase of the open loop gain at the frequency where the magnitude of the open loop gain equals 1.



(a)

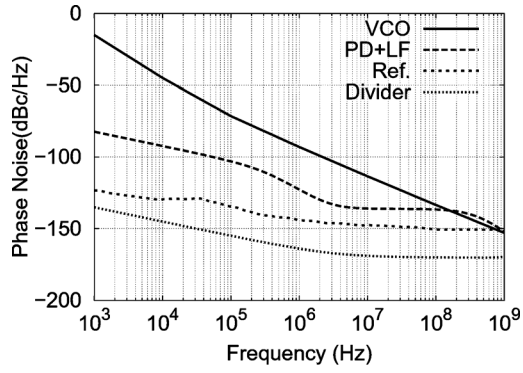


(b)

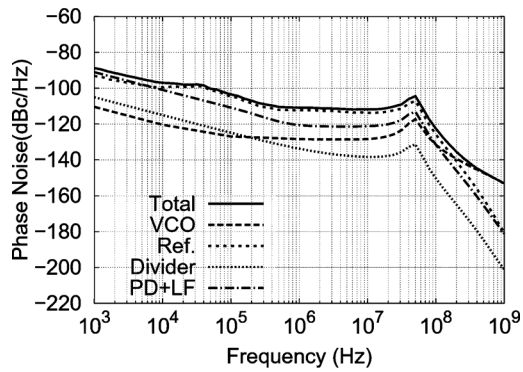


(c)

Fig. 13. Simulated: (a) amplitude and (b) phase of the open-loop gain and the simulated (c) closed-loop gain for different LF load resistor.



(a)



(b)

Fig. 14. (a) Phase noise of individual loop components for simulation. (b) Simulated phase noise and contributions of individual loop components.

than the reference noise. The phase noise is simulated (using ac simulation) based on the model in Fig. 12, where the noise contributions of the individual components ($\Phi_{n\mathrm{Ref}}$, $\Phi_{n\mathrm{PD}}$, etc.) are added separately. The noise is represented by the root mean square (rms) noise voltage at each frequency. The simulated noise data of the PD, LF, frequency divider, and the measured noise data of the VCO, reference signal (1-GHz signal from Agilent signal source E8254A), as shown in Fig. 14(a), are used. The PD and the LF are treated as one circuit and their noises are combined.

The simulated total phase noise and contributions from the loop components are given in Fig. 14(b). The in-band phase noise is mainly dominated by the reference signal and the out-of-band noise is dominated by the VCO. The noise from the PD and LF is well suppressed due to the high gain in the LF. The divider phase noise is much lower and has almost no influence on the output phase noise. The minimum in-band phase noise is mainly determined by the contribution from the PD and LF, which is about -120 dBc/Hz at 1-MHz offset.

C. Transient Simulation

PLL locking is a nonlinear and dynamic process, which cannot be modeled using the linear model in Fig. 12. Therefore, the complete PLL circuit (VCO, divider, PD, and LF) is simulated in the time domain using transient simulation. Fig. 15 shows the simulated tuning voltage of the VCO when locking to a 1.1-GHz reference signal. The locking time is less than 100 ns.

V. Measurement Results

Fig. 16 shows a photograph of the PLL IC. The chip is very compact and occupies an area of only 1.1×1 mm^2, including the bonding pads.

The circuit is characterized on-wafer. The output is connected through a ground–signal–ground (GSG) probe to a V-band mixer (Agilent 11970V), which extends the frequency range of the spectrum analyzer (Agilent 8563E). A signal generator (Agilent 8254A) is used to generate the reference signal, which is connected through a GSG probe to the input of the PD (the second input is grounded by the ground of the probe). The VCO and frequency doubler are biased with a 4-V supply and draw 60-mA current. The frequency divider and PD are biased with a 3.5-V supply and consume 54-mA current (45 mA for

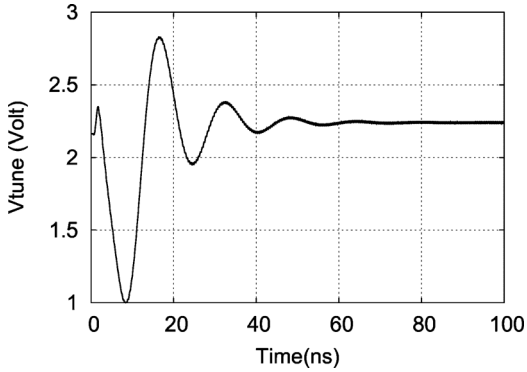


Fig. 15. Simulated tuning voltage of the VCO versus time when locking to a 1.1-GHz reference signal.

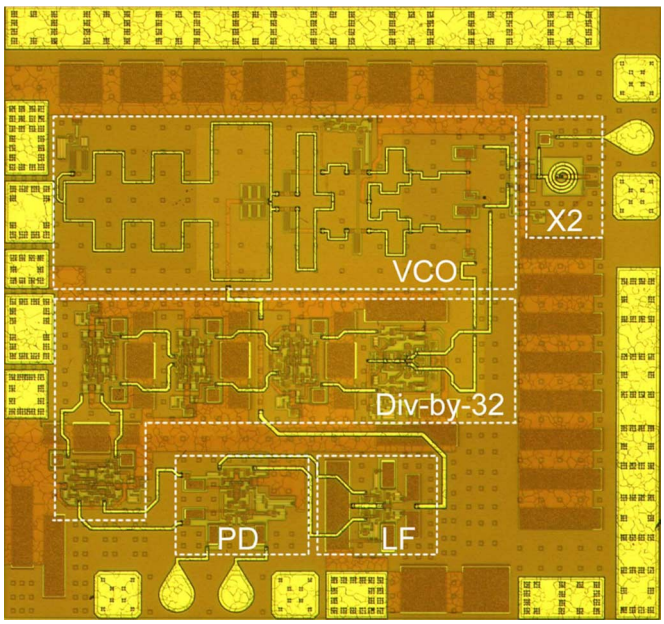


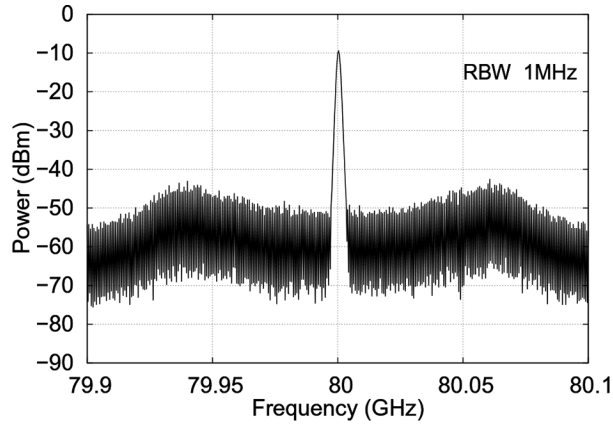
Fig. 16. PLL chip photograph. The chip size is 1.1×1 mm^2.

a divider). The supply voltage of the LF varies from 2 to 8 V with a current change from 2 to 11 mA (due to the output EF).

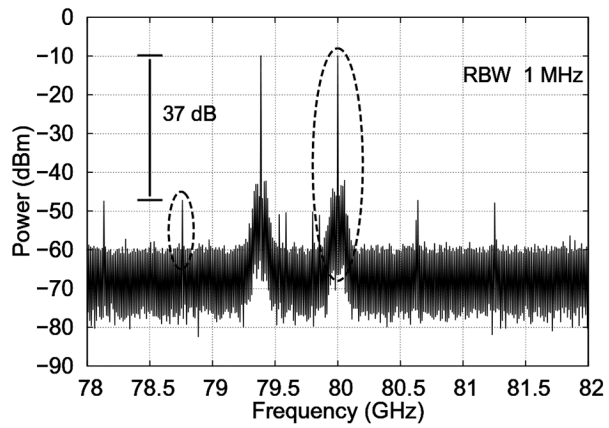
A clean locked spectrum is observed at the output. Fig. 17 shows the locked spectrum at 80 GHz with different span. The filter is biased at 6 V. The reference signal is at 1.25 GHz, with a power of -15 dBm. The suppression of the reference spur is 37 dB. Fig. 18 shows the measured phase noise at different frequencies. The measurements are very close to the simulation results (6 dB are added to simulation results because of frequency doubling). At 1-MHz offset, the measured phase noise is -106 dBc/Hz. The rms phase error (integrated up to 100 MHz) is 4.4°, which is calculated from the measured phase-noise data using the following equation [20]:

$$\sigma_\phi = \frac{180}{\pi}\sqrt{2 \cdot \int_a^b L(f) \cdot df} \tag{3}$$

where σ_ϕ is the rms phase error in degrees, $L(f)$ is the measured phase noise power relative to carrier (in scalar units), and a and b are the lower and upper limits for integration.



(a)



(b)

Fig. 17. Locked spectrum at 80 GHz with: (a) 200-MHz and (b) 4-GHz span. The spectrum at 79.4 GHz in (b) is an artifact of the harmonic mixer.

With a 4-V supply at the LF, the PLL can lock from 69.8 to 76.9 GHz, which is limited mainly by the loop bandwidth. By changing the LF supply voltage, the PLL can lock to different frequency bands, as shown in Fig. 19, covering the complete frequency range from 64 to 84 GHz.

The output power of the PLL is given in Fig. 20. At 64 GHz, the measured output power is -2.4 dBm. Due to the increased conversion loss of the doubler, the output power decreases to -8.1 dBm at 84 GHz.[5] The leakage of the fundamental signal at the output is below -20 dBm over the whole tuning range, as shown in Fig. 20.

Table I compares this study with other fully integrated V/W-band PLLs. This work achieves the widest frequency tuning range and lowest in-band phase noise.

VI. Conclusion

This paper has presented the design, simulation, and characterization of a mm-wave PLL circuit that achieves the widest frequency tuning range (64–84 GHz) among all reported mm-wave PLLs. The circuit is realized in a low-cost 80-GHz SiGe HBT technology, yet still delivers a satisfactory output power of -2.5 dBm at 64 GHz and -8.1 dBm at 84 GHz. The measured phase noise (-106 dBc/Hz at 1-MHz offset) is

[5]The output power above 75 GHz is underestimated due to the higher conversion loss of the V-band mixer.

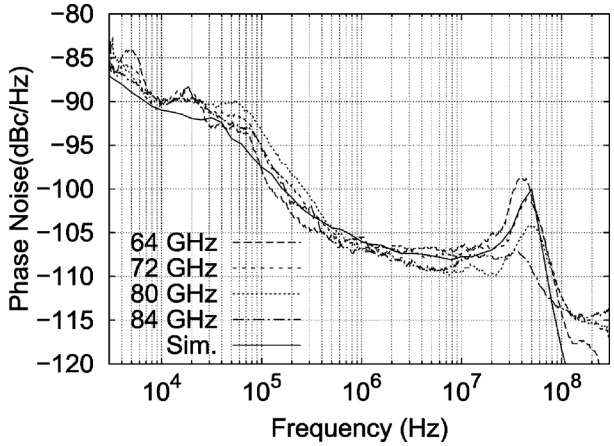


Fig. 18. Measured phase noise at different frequencies in comparison with simulation. 6 dB is added to the simulation because of frequency doubling.

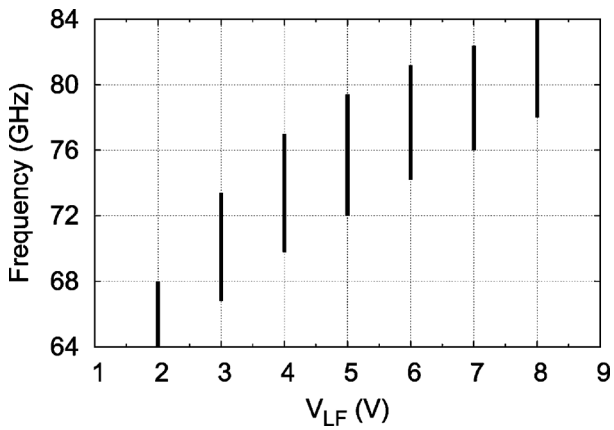


Fig. 19. Measured locking range at different LF supply voltages.

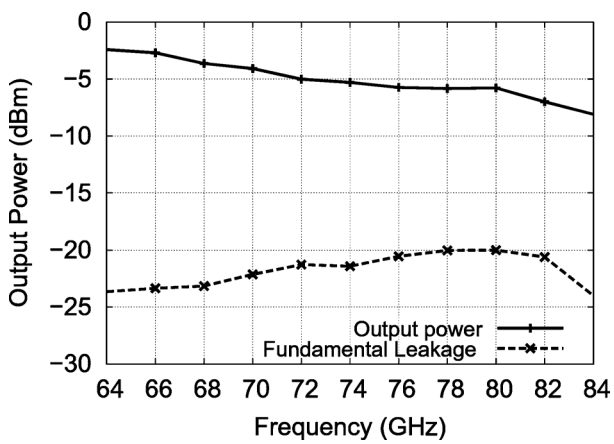


Fig. 20. Measured power of the frequency-doubled signal and leaked fundamental signal at the output of the two PLLs.

the lowest reported in-band phase noise for PLLs in similar frequency ranges. The circuit is well suited as a V/W-band signal source for low-cost applications.

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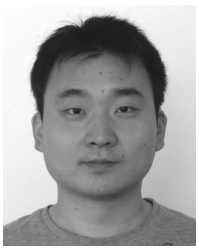

Gang Liu (S'07–M'12) received the B.E. degree in electronics engineering from Shandong University, Shangdong Province, China, in 2005, the M.Sc. degree in communications technology from Ulm University, Ulm, Germany in 2007, and is currently working toward the Ph.D. degree at Ulm University.

He is currently with the Institute of Electron Devices and Circuits, Ulm University. His research topics mainly involve design and characterization of RF/mm-wave front-end circuits and passive elements and modules, as well as their applications in wideband wireless systems.

Andreas Trasser received the Ph.D. degree from RWTH Aachen, Aachen, Germany, in 1989.

In 1990, he joined the Institute of Electron Devices and Circuits, Ulm University, Ulm, Germany, where he currently is a Member of the Academic Staff and a Lecturer. His research interests are mainly focused on the design of analog circuits.

Hermann Schumacher (M'93) received the Dr.-Ing. degree (Doctorate) in engineering from RWTH Aachen, Aachen, Germany, in 1986.

From 1986 to 1990, he was with Bellcore, Red Bank, NJ. He then joined Ulm University, Ulm, Germany, as a Professor with the School of Engineering and Computer Engineering. He is currently the Director of the Institute of Electron Devices and Circuits, Ulm University, and the Director of the Communications Technology international M.Sc. program. His research interests range from compound semiconductor devices for microwave and mm-wave applications to high-frequency microsystems, including low-cost mm-wave communication solutions and impulse-radio ultra-wideband techniques for biomedical sensing.