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Technology and Characterization of InAlN/GaN FETs

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von

Mohammed Alomari

aus Dayr Yusef

Gutachter:	Prof. Dr.-Ing. Erhard Kohn Prof. Dr.-Ing. Andrei Vescan
Amtierender Dekan:	Prof. Dr.-Ing. Klaus Dietmayer

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To My parents and family, and to my Coco

Acknowledgments

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Abstract

In this work the lattice matched $In_{0.17}Al_{0.83}N$/GaN heterostructure was investigated. The work started by establishing the main features of this heterostructure in a HEMT configuration through the investigation of the DC, small signal and large signal characteristics of planar HEMTs. The study included heterostructures with variable barrier thicknesses, but still thinner than what is conventionally used in AlGaN/GaN HEMTs. Using these heterostructure a barrier scaling study combined with static simulations revealed an initially low surface potential, which is combined with the high polarization discontinuity of this heterostructure, thus yielding HEMTs with high current densities and high aspect ratios. Current densities above 1 A/mm and up to 2.4 A/mm could be achieved in this work and the HEMTs demonstrated high cut-off frequencies, scaling with the gate length, up to an f_t= 61 GHz and f_{max}= 112 GHz for 0.1 µm long gates. In addition, the high thermal stability of the heterostructure was established through a series of storage and operating tests at temperatures above 500 °C and up to 1000 °C. This allowed the optimization of a thermal oxidation process to reduce the HEMT gate leakage but most importantly as an efficient preparation for surface passivation. The oxidation process was investigated by using actual HEMT structures, with the corresponding DC, small signal and large signal analysis, and also dedicated structure to investigate the effect of localizing the oxidation process around the gate area, which is the area of interest for power operation. This passivation scheme yielded a lag free device at 4 GHz with output power density of 11.6 W/mm at a drain voltage of 20 Volts, so far the highest reported for this heterostructure. In addition, relying on the initial experiments indicating the heterostructure stability, nanocrystalline Diamond overgrowth experiments were conducted for efficient heat extraction from the device, as was evaluated using thermal simulations. The Diamond deposition conditions were optimized to yield films with high thermal conductivity reaching 1000 W/mK in the vertical direction of heat flow toward the position where the heat sink would be placed. These conditions were restricted to deposition temperatures above 700 °C, with bias enhanced nucleation also conducted above 700 °C, with slow deposition rate of around 0.1 µm/hour. A series of experiments were conducted to verify the heterostructure stability under these conditions by fabricating devices after growth and complete removal of the overgrown Diamond film. After establishing the heterostructure stability, a series of experiments progressed toward obtaining a fully Diamond coated HEMT by growth experiments on gateless HEMTs and the subsequent optimization of the ohmic contact, and the growth on gateless HEMTs with different passivation and the subsequent optimization of the passivation deposition process, to reach finally a fully processed Diamond coated HEMT with 1 µm Diamond film thickness. This was done using two different Diamond nucleation techniques, namely the bias enhanced nucleation and the nanoparticle seeding. The first Diamond overgrown GaN HEMTs operating at frequencies above 1 GHz were demonstrated, keeping a relatively high current density above 1 A/mm. The optimization of this

process also enabled continuous operation at very high temperatures above 500 °C and up to 1000 °C, thus reaching with this heterostructure to limits beyond the best achieved with any other semiconductor. Moreover, another approach of combining Diamond with GaN through direct heteroepitaxy of AlGaN/GaN HEMT structure on single crystalline Diamond was investigated, and achieved through a dedicated effort from the growers, enabling the demonstration of the first ever reported GaN HEMT on Diamond substrates.

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List of abbreviations

2DEG Two Dimensional Electron Gas

2DHG Two Dimensional Hole Gas

ALD Atomic Layer Deposition

AlGaN Aluminium Gallium Nitride

AlInN Aluminium Indium Nitride

AlN Aluminum Nitride

BEN Bias Enhanced Nucleation

FEM Finite Element Method

FET Field Effect Transistor

GaAs Gallium Arsenide

GaN Gallium Nitride

hcp Hexagonal-Closed-Packed

HEMT High Electron Mobility Transistor

HF-CVD Hot Filament Chemical Vapor Deposition

HR-XRD High Resolution X-Ray Diffraction

HfO_2 Hafnium Oxide

InGaN Indium Gallium Nitride

InN Indium Nitride

InP Indium Phosphide

ISFET Ion Sensitive Field Effect Transistor

LDMOS Laterally Diffused Metal-Oxide-Semiconductor

LED Light Emitting Diode

LM-InAlN Lattice-Matched Aluminium Indium Nitride

MBE Molecular Beam Epitaxy

MESFET Metal Semiconductor Field Effect Transistor

MISFET Metal Insulator Semiconductor Field Effect Transistor

MOCVD Metal Organic Chemical Vapour Deposition

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MOVPE Metal Organic Vapour Phase Epitaxy

MP-CVD Microwave Plasma Chemical Vapour Deposition

NCD Nanocrystalline Diamond

PAE Power Added Efficiency

PCVD Plasma Chemical Vapour Deposition

RIE Reactive Ion Etching

RTA Rapid Thermal Annealing

SiC Silicon Carbide

Si_3N_3 Silicon Nitride

SiO_2 Silicon Oxide

TEM Transmission Electron Microscopy

TBR Thermal Boundary Resistance

ZrO_2 Zirconium Oxide

List of symbols

$V_{Built-in}$ Built-in voltage

$\triangle E_c$ Conduction band offset

a_0 Length of the basal hexagon (at equilibrium) in a hexagonal lattice

c_0 Height of the hexagonal prism (at equilibrium) in a hexagonal lattice

C_{GD} Gate-drain capacitance

C_{GS} Gate-source capacitance

$C_{barrier}$ Barrier capacitance

$d_{barrier}$ Barrier thickness

E_g Bandgap

E_{Br} Break down field

E_F Fermi level

E_c Critical field

f_{max} Maximum oscillation frequency

f_t Cutt-off frequency

g_m Transconductance

I_{DS} Drian-source current

J_T Tunniling current density

L_G Gate length

P^{tot} Net polarization

P_{pz} Piezoelectric polarization

P_{sp} Spontaneous polarization

q Elementary charge

R_C Contact resistance

R_{on} On-resistance

R_{sheet} Sheet resistance

R_{GS} Gate-source resistance

$T(E)$ Transmission probability

u_0 Anion-cation bond length (at equilibrium) along the c-axis of a hexagonal lattice

V_{Br} Break down voltage

V_{DS} Drain-sorce voltage

V_{GS} Gate-sorce voltage

V_{knee} Knee voltage

V_p pinch-off voltage

W_G Gate width

N_s Sheet charge density

μ Electron mobility

ν_e Electron velocity

ϕ_{SB} Contact potential

ϕ_s Surface potential

$\sigma_{pol,interface}$ Excess bound sheet charge density

σ_P Polarization induced bound sheet charge density

υ_{sat} Saturation velocity

ε_r Dielectric constant

ϵ_j Strain in direction j

e_{ij} Piezoelectric coefficients along the direction j

1

INTRODUCTION AND THESIS OUTLINE

Silicon semiconductor devices have replaced many conventional electrical parts in the past four decades in a wide spectrum of applications ranging from military applications to civil applications and consumer products. Although silicon is expected to remain as the dominant semiconductor of choice in many applications, wide band gap semiconductors (usually defined as having a band gap larger than 1.7 eV), like GaN, SiC, and Diamond are being investigated as a replacement for silicon technology in some applications, where silicon is reaching its physical limit. These limits are imposed by an increased market need for electronics that are faster, more thermally stable, more robust and more miniaturized and compact, in an era that witnesses the wide spread application of wireless communications like in radars and base stations, and energy conversion like lightening, and optical communication, and information transmission, while at the same time trying to reduce the overall energy consumption and losses.

These needs can be met using wide bandgap semiconductors, the properties of which are summarized in table 1 and compared to Si and GaAs. The difference in the crystal structure (Diamond-cubic for Si and single crystal Diamond, hexagonal Wurtzite (hcp) or zinc blind for GaN and SiC, and zinc blind for GaAs) and the composition gives rise to different widths of the bandgap, dielectric constants, electron and hole mobilities and saturation velocities and thus fundamentally different electronic properties. But in general, the properties listed address the fundamental needs mentioned earlier. for example, the wide bandgap of GaN, SiC and Diamond allows for a higher break down voltage (V_{Br}) enabling the application of higher supply voltages, which makes these materials attractive for high power applications [15]. Moreover, the larger bandgap makes these materials less susceptible for thermal noise (if the material can be grown with a low trap concentration) and allows operation at higher temperatures [16]. For high frequency applications the product of mobility and saturation velocity is essential. This makes InP and GaAs prime candidates for high frequency applications but limited to low voltage applications due to their relatively low breakdown field. In addition, the higher thermal conductivities of GaN, SiC and Diamond allow better thermal management for high power applications, where device self-heating is coupled with output power. Thus GaN, SiC and Diamond seem to provide the best compromise for achieving high power/high frequency operation, power switching and high temperature applications.

Based on the arguments above, it is clear that Diamond (in its single crystal form) is expected to outperform the other materials. However, the maturity of the technology for the relevant semiconductor has to be taken into account. For example, silicon is still the dominant semiconductor of choice for electronics due to its long research history, the maturity of its material growth and fabrication technology, in addition to its ability to form a stable native oxide. Diamond has been intensively studied and is being used in many

	E_g [eV]	μ [cm^2/Vs]	v_{sat} [10^7 cm/s]	E_{Br} [MV/cm]	κ [W/cmK]	ε_r
Si	1.12	1400	1	0.3	1.3	11.9
GaAs	1.42	8500	1.2	0.55	0.55	12.9
GaN (hcp)	3.4	1200	1.3	5	1.3	9.5
6H-SiC	3	400	2	3	4.9	9.7
Diamond	5.43	4500	1.6	1	22	5.7

Table 1: Basic material parameters of GaN, SiC and Diamond compared to Si and GaAs. After [9, 10, 11, 12, 13]

non-electronic applications in its polycrystalline form as hard coating material but the use of Diamond in electronic applications is limited by the lack of a large area substrate. The difficulty to grow single crystalline Diamond on foreign substrates like silicon and the difficulty of doping seem to have slowed down its advance in the electronics industry[17]. SiC faces a similar limitation due to its high wafer cost compared to GaN. GaN on the other hand has reached a fairly advanced maturity in terms of material growth technology and understanding the atomic surface behavior [18] pushed by the intensive research to use the material as an efficient light emitting source. The main factor driving the wide use of GaN in optical application is the ability to grow ternary and quaternary GaN based alloys, referred to as the III-nitride group, thus enabling the engineering of the bandgaps and quantum wells and thus varying the wavelength of the emitted light, from blue, as first demonstrated in an LED by Nakamura et. al. in 1994 [19], to even ultra-violet ranges [20, 21].

Along with the mastery of growth, III-nitride alloys of GaN, AlN, and InN (in Wurtzite structure) are attractive for electronic applications due to the unique property of obtaining large polarization fields, which promotes the ability to form heterostructures with large carrier densities at the interface as a two dimensional electron gas (2DEG) with high mobilities, as will be discussed in section 2.1. GaN based heterostructures, like the traditionally used AlGaN/GaN, having a high breakdown voltage and a large carrier density with high mobility, made it firstly ideal for high frequency/high power applications, as HEMT devices, the basics of which will be described in section 2.3.2, and now also in power switching and high temperature electronics. The ultimate performance of such heterostructures will be gained when both ends of the III-nitride alloys are used, namely employing an AlN barrier on a GaN buffer (AlN/GaN HEMT structure), the main reason being that this heterostructure has the highest polarization induced carrier density at the interface. This will be discussed in details in section 2.1. Starting from GaN or InN this can be achieved by increasing the Al-content, thus following either an Al-GaN line or Al-InN line. Along the latter, one encounters the AlInN alloy with 83% Al-content, which is lattice matched to GaN. This material is the focus of the work presented here and will be denoted LM-InAlN throughout this work.

Many demonstrations of such GaN based HEMTs (AlGaN/GaN, AlInN/GaN and AlN/GaN) have already shown the capability to exceed what is achieved by Si technology [22] in terms of output power and operation frequency, particularly beyond what is reached by Silicon LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) power amplifiers and above 2 GHz. High output power densities at operation frequencies above 1 GHz [23, 24, 25], up to 40 W/mm [26] have been demonstrated. Moreover, the on-resistance (R_{on}) - breakdown voltage product is approaching the physical limit of SiC [27, 28, 29, 30, 31] proving the suitability of GaN HEMTs for power switching applications. High current gain cut-off frequency and maximum oscillation frequency (f_t and f_{max}) in the GHz regime can be routinely achieved due to a high channel mobility and high transconductance and the relatively high device aspect ratios that can be achieved. A recent example is a LM-InAlN/GaN HEMT with f_t of 300 GHz [32], so far the highest reported f_t for a GaN HEMT. Based on the high polarization fields and high breakdown fields in GaN heterostructures a natural super-junction breakdown voltage of 9000 V was demonstrated [33]. In addition, these heterostructures are expected to operate more reliably than Si in harsh environment like elevated temperatures above 200 °C, or in chemical sensing environments that are aggressive to Si.

But despite this impressive performance, stability issues are not usually reported and GaN based HEMTs still did not establish their presence commercially due to stability and reliability issues [25, 34, 35] intrinsic to the HEMT structure. Mainly these are the surface charge stability issues like current collapse (discussed in section 2.5.1) and the device self-heating at high output powers (discussed in section 2.5.2). Due to their intrinsic nature, these limitations can not be completely eliminated but rather the onset of their effects on the device can be pushed further beyond the targeted operating range. To achieve this, several technological solutions are proposed. For example, using a cap layer for surface passivation or to growing the HEMT device on highly thermally conductive substrates like SiC [11], and lately by direct growth on Diamond substrates [36] as will be shown in this work, or via hybrid integration by wafer bonding to Diamond substrates [37, 38], for a better thermal management of the device. However, to apply more advanced and unconventional solutions, like what will be presented in this work, a proper choice of the heterostructure material is essential.

The heart of this work is the development of a processing technology for overgrowing high performance LM-InAlN/GaN HEMTs with nanocrystalline Diamond films, for heat spreading purposes. The work presented here has been part of a larger effort in the European community (through the EU projects Ultra GaN (http://www.ultragan.eu/) and Morgan (http://www.morganproject.eu/)) to investigate the potential of this heterostructure. The work involved a high level of cooperation with the growth teams, and a constant feedback with the characterization teams, in order to optimize the heterostructure for subsequent Diamond growth. The heterostructure growth was performed by several groups, namely, Ecole Polytechnique Federal de Laussan in Switzerland (EPFL), Alcatel-Thales III-V labs in France (III-V Labs), AIXTRON in Germany and FORTH in Greece. The small signal and large signal characterization was performed in the Institute D'electronique, de Microelectronique et de Nanotechnologie (IEMN) in France. Material

analysis using high resolution TEM was conducted partly in the Materialwissenschaftliche Elektronenmikroskopie Department at Ulm University (Z. E. Elektronenmikroskopie) and partly in the Research Institute for Technical Physics and Materials Science (MFA) in the Hungarian Academy of Sciences in Budapest. The thermal characterization of the grown nanocrystalline Diamond films was conducted by the University of Glasgow (GLG).

The other side of the technology, namely the optimization of the overgrown nanocrystalline Diamond films for heat spreading purposes, was conducted in the Institute of Electron Devices and Circuits (EBS) in Ulm University by M. Dipalo and S. Rossi. The work presented here is the result of a common optimization of both technologies.

The application of the Diamond overgrowth technology is allowed by the exceptional properties of the heterostructure. The LM-InAlN/GaN with 83% Al-content is very close to the sought-after AlN/GaN heterostructure, which is difficult to grow due to the high stress between the AlN barrier and the GaN buffer. In the LM-InAlN/GaN 2DEG densities up to 2.6 x 10^{13} cm^{-2} can be achieved, enabling high power densities at moderately low drain voltages. However, the most attractive feature of this heterostructure is its ceramic-like stability, first demonstrated in 2006 by short time HEMT operation at 1000 °C in vacuum [39]. This high thermal stability is invested in this work in applying novel solutions for the surface passivation problem (or current collapse) using thermal oxidation, and thermal management for high power applications by combining monolithically integrated polycrystalline Diamond heat spreader by direct growth on top of a completely prefabricated HEMT. Both processes are performed at temperatures above 700 °C , not suitable for the other heterostructures, like the commonly used AlGaN/GaN, and require optimization of several aspects of the HEMT design, like the barrier thickness, the metallization schemes used and the HEMT passivation. The thesis outline will thus follow the rout taken to optimize, apply and characterize these technologies.

Firstly, an introduction to the III-nitride heterostructure, and specifically of GaN based HEMTs, will be presented to illustrate the role of polarization charges and surface counter charges in the formation of the 2DEG. This is followed by outlining the basic model of GaN HEMTs. These sections will serve as a guide to discuss the technological limitations of GaN HEMTs (device scaling properties), as well as intrinsic limitations (current collapse and self heating). After that, an argument will be presented of why the LM-InAlN/GaN HEMT can be a very good compromise in terms of high performance and high stability, even when using a simple planar device fabrication technology as in this work. After describing the fabrication technology used here and identifying the basic HEMT properties, through modeling and scaling experiments, experimental evidence of the high thermal stability of this heterostructure is presented together with a first insight into failure mechanisms for high temperature storage or operation.

As mentioned before, the HEMT high thermal stability will be utilized in applying a thermal oxidation/nitride passivation scheme efficient to suppress current collapse effects. After characterization and optimization of the oxidation process the passivation scheme was applied to a power HEMT. This enabled using the full current density of the device (2.4 A/mm as characterized by pulsed DC conditions) for power operation at 4 GHz, yielding a record output power density of 11.6 W/mm at relatively moderate drain voltage of 20 V.

This passivation scheme also proved to be crucial in stabilizing the HEMT surface, specially around the gate region, and thus allowed high continuous large signal operation at high temperatures above 500 °C and up to 1000 °C in vacuum, never achieved before for any other semiconductor. This opens new possibilities for electronics to extend its presence to harsher environments, which could not be accessed before.

This optimization also paved the way to applying an advanced heat spreader configuration, using the high thermal stability of polycrystalline Diamond deposited on top of a fully fabricated HEMT. The harsh polycrystalline Diamond growth conditions are difficult to be applied on other heterostructures, even bare and before the fabrication of the HEMT, without compromising the heterostructure properties. These growth conditions will be described after presenting a theoretical evaluation of the advantages of using this configuration. Finally the optimized technological steps leading to the first demonstration of a Diamond coated HEMT operating in the GHz regime will be described. The technology developed also served as a base for a Diamond-GaN ISFET for harsh chemical applications, owing to the inertness of Diamond, as presented in [40, 41, 42].

Together with the demonstration of the world premier high frequency GaN HEMT directly grown on single crystalline Diamond, also demonstrated in this work in cooperation with EPFL, both technologies present an ultimate solution to heat management issues in high power HEMTs if combined.

Finally an outlook concerning possible alternatives for passivation and fabrication technology, which enables an even higher HEMT thermal stability (required for example to grow thicker Diamond films on top of the HEMT), are presented followed by a summary and conclusion of the work.

2

GaN BASED HETEROSTRUCTURES: ADVANTAGES AND CHALLENGES

In this chapter the advantages and challenges of GaN based HEMTs will be discussed. The advantages of using GaN HEMTs for high power and high frequency applications originate first from the basic physical properties it possesses by belonging to the wide bandgap semiconductors class. The III-N group in particular has the unique property of obtaining large polarization fields due to its crystal structure as will be discussed in section 2.1, which promotes the ability to form heterostructures with large carrier densities as will be discussed in section 2.2. GaN based heterostructures, having a high breakdown voltage and a large carrier density with high mobility, makes them ideal for high frequency/high power applications, power switching applications and high temperature applications, as HEMT devices, the basics of which will be described in section 2.3.2. However, the devices performance is limited below the ideal expectations imposed by the actual material properties. Section 2.4 will discuss these limitations briefly as a preliminary for the solutions presented in this work.

2.1 III-N group electronics

The III-nitrides material group GaN, AlN and InN can crystallize in the Wurtzite crystal structure or zincblende crystal structure. But in contrast to cubic III-V semiconductors like GaAs and InP, which retain a thermodynamically stable zincblende structure, III-nitrides retain the thermodynamically stable Wurtzite structure under ambient conditions. Fig. 1a shows a schematic of the hexagonal Wurtzite lattice of III-nitrides defined by the lattice parameters a_0 (the length of the basal hexagon), c_0 (the height of the hexagonal prism) and u_0 (the anion-cation bond length along the c-axis) where the subscript "0" indicates values at equilibrium. The ideal Wurtzite crystal is composed of two hexagonal lattices shifted ideally by a ratio of $c_0/a_0 = (8/3)1/2 = 1.633$ and $u_0 = 3/8$. This will result in symmetrical tetrahedrons (each atom is bonded with four nearest neighbors atoms) of equal side lengths and equal angles (Fig. 1b). This unit cell lacks the inversion symmetry (non-centrosymmetric) which means that each plane is composed of the same atom type (cation or metal) while the next plane is composed of nitrogen atoms (anions) and gives rise to polar crystal surfaces, which has either the metal face consisting of group-III elements (Ga, Al or In) polarity designated (0001) or nitrogen face polarity designated $(000\bar{1})$.

In both cases of polarity the small atomic radius and the high electronegativity of the nitrogen atom shifts the negative charge centroid towards it and away from the metal thus creating a local polarization. This occurs along the c-axis bond and the basal plane bonds. If the crystal structure has inversion symmetry and an ideal c_0/a_0 ratio of 1.633 (called the ideality factor) the resultant polarization vectors will compensate each other. The III-nitrides with its non-centrosymmetry however deviate from this ideality factor,

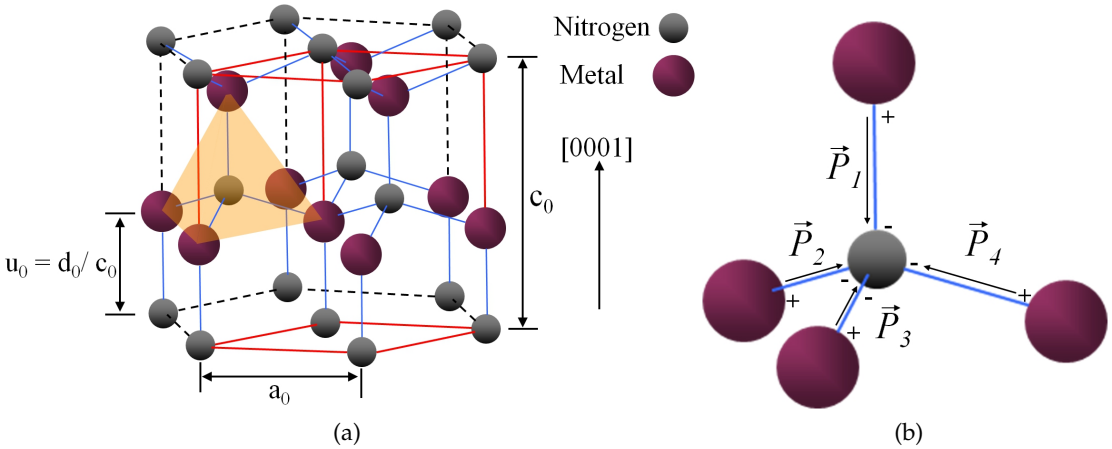


Figure 1: A schematic of (a) the ideal hexagonal lattice of III-nitride and (b) the tetrahedron shaded in (a) with the polarization vectors induced by the difference in electronegativity of the constituent nitrogen and metal atoms.

with GaN being the closest by a c_0/a_0 ratio of 1.625, thus resulting in a net polarization along the c-axis. This polarization occurring at equilibrium is referred to as spontaneous polarization (P_{sp}). The degree of the strength of this polarization depends on the c_0/a_0 ratio. Bernardini et al. presented a calculation of the spontaneous polarization in relation with the lattice parameter [43]. The different cation and ionic radii of Ga, Al and In gives rise to different a_0 and c_0 lattice parameters and thus different lattice parameter u_0, or a non ideal factor, resulting in binary alloys with different bandgaps and different spontaneous polarization values. The same is true for ternary alloys (In_xGaN_{1-x}, In_xAlN_{1-x}, ...) and quaternary alloys ($In_xAl_{1-x}GaN$) where the bandgap and spontaneous polarization is extrapolated through Vegard's law as a first approximation. Ambacher et al [1] presented an extensive review of the III-nitrides properties taking into account the bowing parameters. The empirical formulas presented in this review will be adopted here. Figures 2a and 2b show the relation between the composition of the alloy and its lattice parameters for a crystal with Ga face polarity. It is worth noting that an AlInN alloy with 83% Al content has the same lattice constant a_0 as GaN, or in other words it is lattice matched to GaN in the plane of growth direction [0001]. This alloy ($Al_{0.83}In_{0.17}N$) will be referred to throughout the text with "LM-InAlN". The variation in the lattice parameters leads to a variation in the bandgap (Fig. 2c) and the spontaneous polarization values (Fig. 2d). The negative sign of polarization indicates that the polarization vector points towards the substrate, from Ga atom to N atom, opposite to the [0001] direction. It is to be noted that all III-nitride alloys have a negative spontaneous polarization.

The change in the lattice parameters can also occur without changing the composition of the alloy but by exerting external mechanical forces in form of strain and hence altering

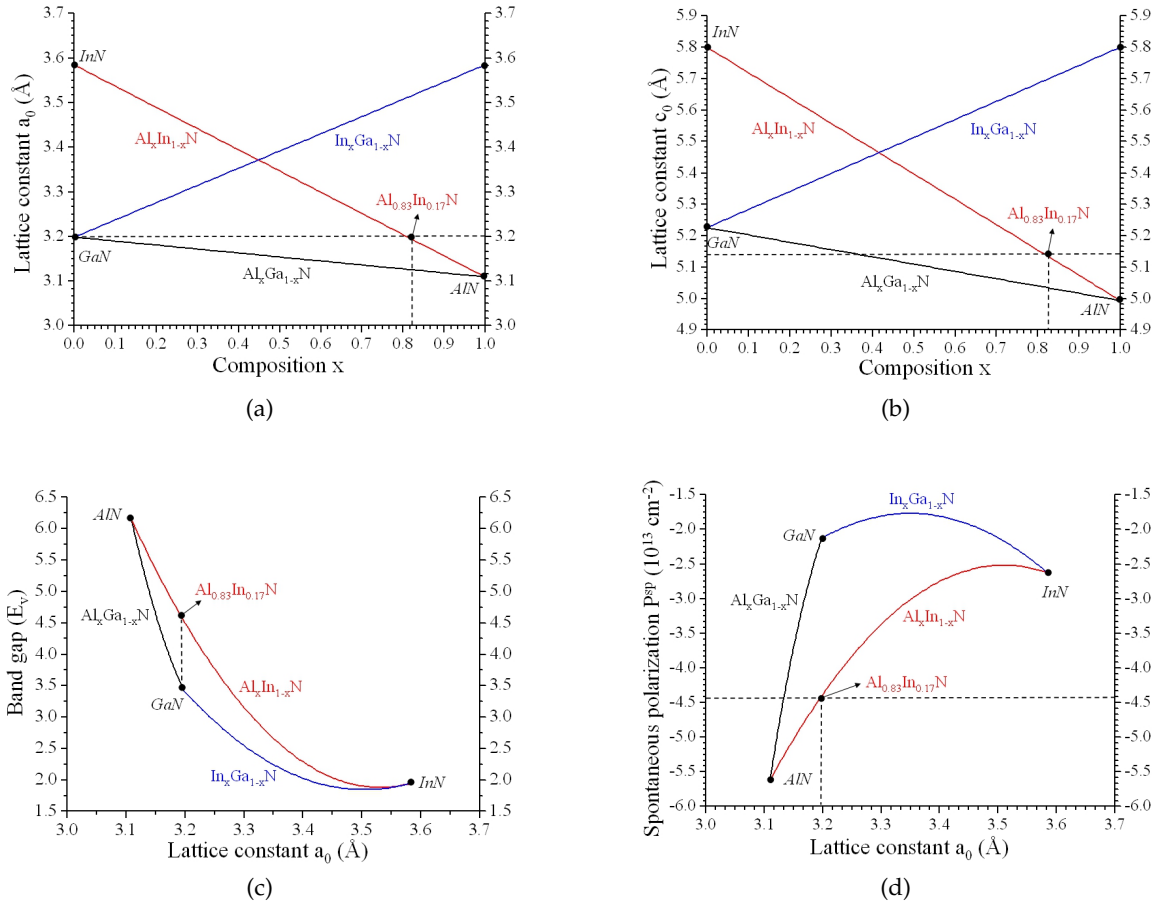


Figure 2: (a) Lattice constant a_0 and (b) c_0 in dependence of alloy composition. A LM-InAlN alloy with 83% Al content has the same lattice constant a_0 as GaN. (c) Alloy bandgap in dependence of the lattice constant a_0 and (d) the spontaneous polarization in dependence of a_0. After [1].

the net polarization by adding the piezoelectric polarization vector (P_{pz}). P_{pz} is described by Hook's law as in equation 2.1:

$$P_i^{pz} = \sum_j e_{ij}\epsilon_{ij} \tag{2.1}$$

Where e_{ij} are the piezoelectric coefficients and ϵ_j is the strain in direction j. Neglecting the shear strain and employing the non zero piezoelectric coefficients (e_{33}, $e_{31}$and e_{15}) the piezoelectric polarization along the c-axis is then described by equation 2.2:

$$P_3^{pz} = e_{33}\epsilon_{33} + e_{31}(\epsilon_1 + \epsilon_3) \tag{2.2}$$

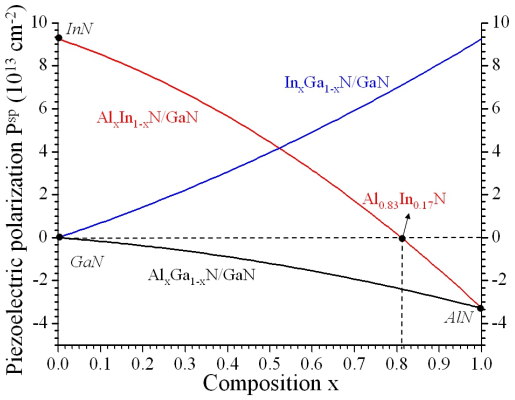


Figure 3: Theoretical values of the piezoelectric polarization (P^{pz}) for III-N alloys grown on relaxed GaN buffer.

Where $\epsilon_3 = (c - c_0)/c_0$ is the strain along the c-axis and $\epsilon_1 = \epsilon_2 = (a - a_0)/a_0$, with a_0 the lattice constant of the relaxed alloy and a the lattice constant of the strained heteroepitaxially grown alloy. The strain along the c-axis is connected to the strain along the basal plane by the elastic constants c_{13} and c_{33} through equation 2.3:

$$\epsilon_3 = -2\frac{c_{13}}{c_{33}}\epsilon_1 \tag{2.3}$$

Thus the piezoelectric polarization along the c-axis can be written in terms of the strain in the basal plane only as equation 2.4:

$$P_3^{pz} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) \tag{2.4}$$

Since e_{31} is always negative and e_{33}, c_{13} and c_{33} are always positive [43] then for a tensile stress ($a > a_0$) P^{pz} is always negative and for compressive stress ($a < a_0$) P^{pz} is always positive. The theoretical calculations of the piezoelectric polarization for III-N alloys grown on relaxed GaN buffer is shown in Fig. 3. The piezoelectric polarization of LM-InAlN on GaN is implicitly zero.

The net polarization (P^{tot}) in an alloy is then the summation of the spontaneous polarization and the piezoelectric polarization as in equation 2.5:

$$P^{tot} = P^{sp} + P^{pz} \tag{2.5}$$

2.2 Gan based heterostructures for HEMT applications

The advances made in the growth methods and techniques of III-nitride alloys allowed an advanced stage in engineering materials with parameters like bandgap, polarization,

dielectric constant, thermal conductivity, etc... , tailored for specific applications. However, the ability to grow heterostructures of III-nitride based materials remains a corner stone for electronic applications, specially power electronics. The built-in spontaneous and piezoelectric fields induced by the difference in the lattice constants between the host substrate and the grown alloy on top, should by theory give rise to high 2-Dimensional Electron (or hole) Gas (2DEG or 2DHG) at the heterostructure interface, without the need of external doping, and thus high lateral breakdown field.

2.2.1 *The formation of 2DEG*

To explain the formation of a 2DEG in III-nitride HEMTs the most commonly used GaN based heterostructures will be used as an example. In these examples a III-nitride alloy (usually called a *barrier*) is grown pseudomorphically on top of a relaxed GaN buffer. Both layers are assumed to be undoped and grown with Ga-face polarity. Variations on this configuration (different buffer, N-face polarity) will however follow the general rules presented here and details can be found in [1, 44, 45, 46].

The gradient of P^{tot} in GaN or its alloys (see Fig. 4) leads to a polarization induced bound sheet charge density (σ_P) to preserve charge neutrality given by:

$$\sigma_P = -\nabla.\overrightarrow{P} \tag{2.6}$$

Holes would then accumulate at the Ga-face and electrons at the N-face. This is illustrated in Fig. 4.

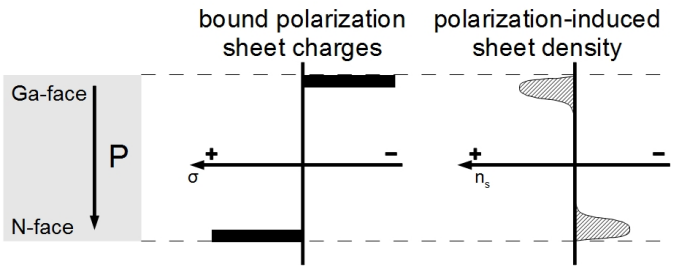


Figure 4: Schematic of the formation of polarization induced bound sheet charge density in polar GaN. The source of these charges is not considered at the moment.

Similarly if two III-nitride materials are grown pseudomorphically then an abrupt change in the polarization would occur at the interface (assuming a smooth interface) leading to an excess bound sheet charge density at the interface ($\sigma_{pol,interface}$) as depicted Fig. 5 and given by equation 2.7 (represented here for an alloy grown on relaxed GaN buffer):

$$\sigma_{pol,interface} = P^{tot}_{GaN} - P^{tot}_{alloy} \tag{2.7}$$

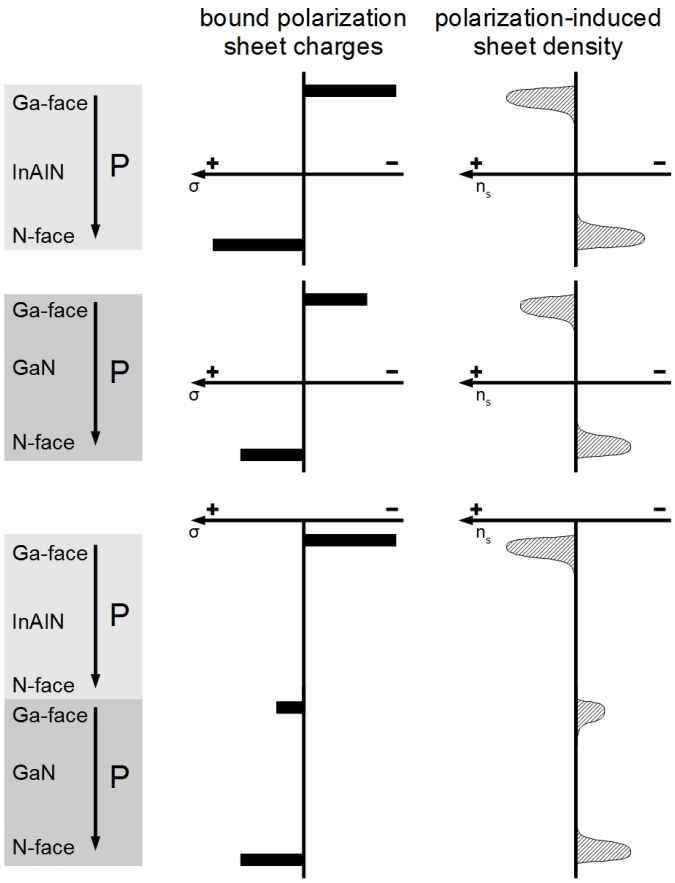


Figure 5: Schematic of polarization-induced interface charge in pseudomorphically grown heterostructure.

where $P_{GaN,alloy}{}^{tot}$ is given by equation 2.5.

To preserve charge neutrality, a counter charge of the same magnitude but with opposite sign should form at the interface either as a 2DEG in the buffer, if it has a smaller bandgap, or 2DHG in the barrier if the barrier has the smaller bandgap, and mirrored by a surface counter charge. The generated sheet charge density (N_s) would then be the difference in the total polarization of both materials (also shown in Fig. 5). However, this represents the maximum N_s that can be obtained for a heterostructure with ideal crystals, without taking into account the influence of the barrier thickness (i.e. the surface counter charge and consequently the surface potential), nor the source of the counter charges or the electrons in the channel. Before discussing these effects, it is worth looking at the expected generated N_s for different barriers grown on GaN buffer (with Ga-face polarity). This is shown in Fig. 6, based on the calculations presented earlier in Figures 2d and 3 and Equations 2.5 and 2.7 after [1]. It is noted that the sheet charge density can be a 2DEG or 2DHG depending on the polarization discontinuity between the GaN buffer and the barrier. In addition, large N_s values are theoretically predicted for $(Al,In)_xGa_{1-x}N$ alloys with increasing the Al-content, like in the case of LM-InAlN (approximately 2.7×10^{13} cm^{-2})

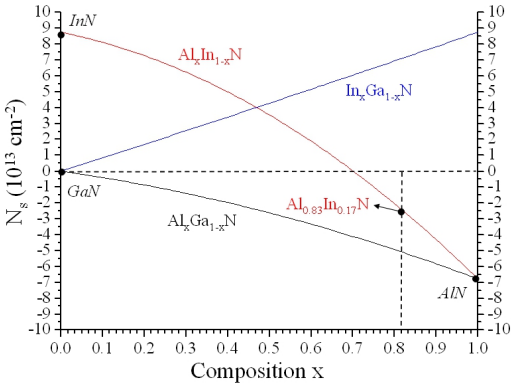


Figure 6: Theoretical maximum 2DEG sheet charge density (N_s) for III-N alloys grown on relaxed GaN buffer with Ga-face polarity in dependence of alloy composition.

and AlN (approximately 6.8×10^{13} cm^{-2}) as a 2DEG moving in the GaN side of the interface with high mobility (as suggested in table 1) and thus high current values can be achieved.

Considering first the general case of a GaN HEMT band diagram as sketched in Fig. 7, an analytical expression of N_s [47] can be written as:

$$N_s = \sigma_{pol,interface} - \left[\frac{\varepsilon_{barrier}}{d_{barrier} \cdot q} \left(\phi_s + E_F(N_s) - \triangle E_{c_{barrier/GaN}} \right) \right] \tag{2.8}$$

where $d_{barrier}$ is the barrier thickness, q the elementary charge, $E_F(N_s)$ is the energy difference between the Fermi level and the conduction band at the bottom of the 2DEG, $\triangle E_{c_{barrier/GaN}}$ is the conduction band offset between the barrier and the GaN buffer and ϕ_s is the surface potential. The energies are in Volts. The charge concentration and polarization discontinuity are in cm^{-2}. It should be noted that ϕ_s is a result of the surface counter charge (relative to N_s) thus controlling this charge is a key factor in optimizing the HEMT design, as will be discussed in section 2.3.1.

For a free surface (no gate contact and gate modulation), this apparent N_s (in the presence of a surface potential ϕ_s) is generally less than the polarization discontinuity. In this case, N_s as a function of the barrier thickness is dependent mainly on the state of ϕ_s, which in turn can be either unpinned or pinned.

If ϕ_s is unpinned as depicted in Fig. 7, N_s be independent of $d_{barrier}$. Thus N_s will be constant and equal to $\sigma_{pol,interface}$ (representing the maximum theoretical value), if the voltage drop across the barrier is zero (flat barrier conduction band) as sketched in Fig. 9a. This however will occur only if the surface counter charge is eliminated. On the other hand, taking into consideration the effect of the surface counter charge (and thus ϕ_s), N_s will be constant and equal to equation 2.8, provided that the value of ϕ_s is known for one barrier thickness (see Fig. 7).

On the other hand, ϕ_s can be pinned and thus N_s becomes a function of the barrier thickness. In this case the maximum N_s can not be reached but can only be approached for very thick barriers. This barrier scaling behavior is observed for most GaN HEMTs

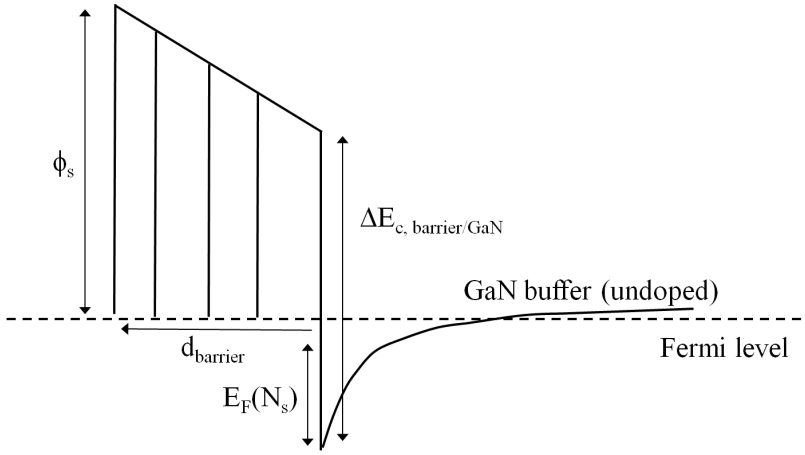


Figure 7: Band diagram of a GaN based HEMT with barrier of thickness $d_{barrier}$ and an unpinned surface potential ϕ_s. In this case N_s is constant and independent of the barrier thickness, and its value is expressed by equation2.8, provided that ϕ_s is known. The case of a pinned surface potential is described in Fig. 9c

like AlGaN/GaN, AlN/GaN and as will be shown in this work, for LM-InAlN, and initially prevented the use of very thin barriers to achieve enhancement mode devices without sacrificing the N_s. For better understanding of this behavior and to introduce an explanation of the source of electrons and the counter charge and surface potential pinning, the next section will present theoretical modeling of this behavior using experimental data of LM-InAlN/GaN heterostructures used in this work.

2.3 Lattice matched InAlN/GaN heterostructure barrier scaling properties

In planar HEMT technology $d_{barrier}$ is a main defining parameter of the HEMT performance, controlling the channel density if the surface potential is pinned as discussed above (see also Fig. 9c). There is no way to ascertain that the surface potential is pinned for a bare, unprocessed heterostructure. Most likely, surface potential pinning occurs once the heterostructure is subjected to the processing environment, which normally includes the use of bases or weak acids, contact deposition and annealing etc..., which alters the original surface states distribution, through, for example, weakly bonded oxygen-Ga(Al, In) species at the surface. However, this processing routine is necessary to measure N_s as a function of the barrier thickness through, for example, Hall measurement. A recent method introduced lately to directly measure the surface potential via Kelvin probe microscopy [48] becomes difficult if ϕ_s is small. Eventually, fabricating the HEMT will include fabrication steps similar to to the ones used for conducting the Hall measurement, and thus modeling the barrier scaling properties using experimental Hall data will be the closest to the actual state of the surface of the fully fabricated HEMT.

2.3.1 *Estimation of the heterostructure surface potential*

In the case of LM-InAlN/GaN heterostructures used here, HEMTs with a total barrier thickness ranging from 3 nm to 33 nm including the 1 nm AlN spacer were grown and characterized (using HRXRD) by EPFL. N_S as a function of $d_{barrier}$ was measured by Hall measurements. ϕ_s of the as-grown heterostructures was estimated based on these data. The heterostructure is simulated using a 2D Poisson-Schrödinger equation solver, fitted to the experimental Hall data of N_S vs. $d_{barrier}$ data. To account for the source of electrons in the channel and the surface counter charge effects, a surface donor model was used (as was also presented for the AlGaN/GaN case in [2]). In this model, surface states (surface donor-like traps), being either electronic or a chemical redox couple on the surface, act as a source of electrons for the channel. The surface potential is thus dominated by these surface state properties, namely their energy level and density. Static simulations were conducted using the commercial *Atlas* Poisson-Schrodinger equation solver from Silvaco [49]. An example of the simulation input file is shown in the appendix with comments on the simulation.

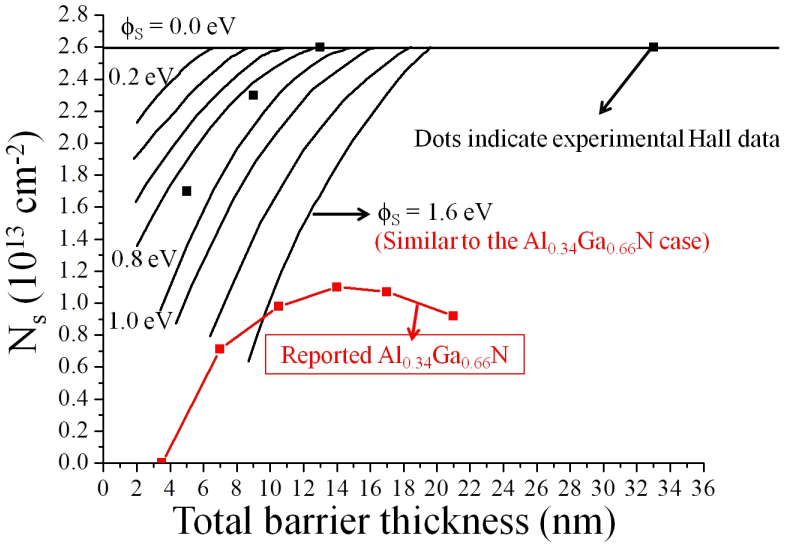


Figure 8: Experimental Hall N_s values vs. $d_{barrier}$ compared to calculated values using different surface potential levels ϕ_s. Also shown in the graph data for the AlGaN/GaN case from [2].

To calculate the band diagram and the resulting 2DEG of the LM-InAlN/GaN free surface with variable $d_{barrier}$, the bandgaps of the LM-InAlN and GaN, the conduction band offset and the polarization discontinuity have to be defined. Experimental Hall data for N_S vs. $d_{barrier}$ were used for fitting. The simulations proceeded as the following:

The bandgaps of InAlN and GaN are set to 4.65 eV and 3.42 eV respectively [1]. The AlN spacer was not included in the simulations but its 1 nm thickness was added to the InAlN barrier thickness. Gonschorek et al. showed that the AlN spacer does not play a role in the formation of the 2DEG if it is below a certain thickness (2nm in this case), which

the 1 nm AlN is, and the main contributor to the 2DEG is the polarization discontinuity with the InAlN barrier, taking into account an effective conduction band offset ~ 0.8 eV between the LM-InAlN and GaN [50, 51]. This value was thus used for these simulations. In addition only 100 nm of the GaN buffer below the InAlN interface is simulated, and a doping density of 1 x 10^{16} cm $^{-3}$ in both materials is added to simulate the unintentional doping reported by the growers.

The value of the polarization discontinuity is set according to the experimental values shown in Fig. 8. As can be seen in the figure, N_S increases up to a barrier thickness of 12 nm where it reaches a value of 2.6 x 10^{13} cm^{-2} and remains constant up to 33 nm, the maximum barrier thickness which was grown. Since the maximum N_s which can be reached in the heterostructure equals $\sigma_{pol,interface}$, this value of 2.6 x 10^{13} cm^{-2} is set as the polarization discontinuity, which is very close to the reported theoretically calculated value [1]. $\sigma_{pol,interface}$ can be set directly in the simulator but without a counter charge on the surface the simulator will assume a 2DEG density at the GaN side of the interface to preserve charge neutrality. This results in the calculated equilibrium band diagram shown in Fig. 9a where the 2DEG density is constant regardless of the barrier thickness, which is not the case found experimentally for a free surface and can be reached only with external gate bias, under the gate metal only, in the absence of any surface states. This case then also represents the HEMT at fully opened gate (barrier flat band condition). Thus a negative counter charge on the InAlN surface of the same magnitude should be added. In this case (shown in Fig. 9b) a constant voltage drop of 3.2 V/nm across the barrier (equivalent to $\sigma_{pol,interface}$) exists thus simulating the polarization field. However, without any source of electrons added so far, no N_S will form regardless of the barrier thickness. Even if all the dopants in the buffer and barrier (doping density of 1 x 10^{16} cm $^{-3}$ in both the InAlN and GaN layers are assumed as reported by the growers) are ionized and driven to the approximately 2.2 nm wide quantum well of the channel (assuming equilibrium as in Fig. 9a) they will amount only to less than 1 x $10^{10}cm^{-2}$ thus the doping can not be the source of electrons in the 2DEG.

The surface donor-like traps which are the source of electrons in this model are then added, not distinguishing the type of the traps, whether electronic or ionic (for example due to desorption of chemical species on the surface). The important parameters here are the traps energy level below the InAlN conduction band edge and the traps density. Here only discrete, single energy level traps are simulated. The traps on the surface could have a distribution of energies, if for example different species are adsorbed on the surface, but so far no evidence supporting this or information about the distribution width exists. Thus this case was not simulated. The trap energy was varied between fully ionized (0 eV, being located at the conduction band edge of InAlN) and 1.6 eV below the conduction band edge (similar to the AlGaN case [2]) in steps of 0.2 eV. The barrier thickness was varied between 2 nm and 33 nm in steps of 0.3 nm. These configurations are limited by the mesh density allowed in the simulator.

For very thin barrier thickness (approximately less than 1 nm for the LM-InAlN/GaN as can be estimated from the Hall measurement data) the surface traps with energies larger than zero are below the Fermi level and are not ionized yet so no source of electrons for

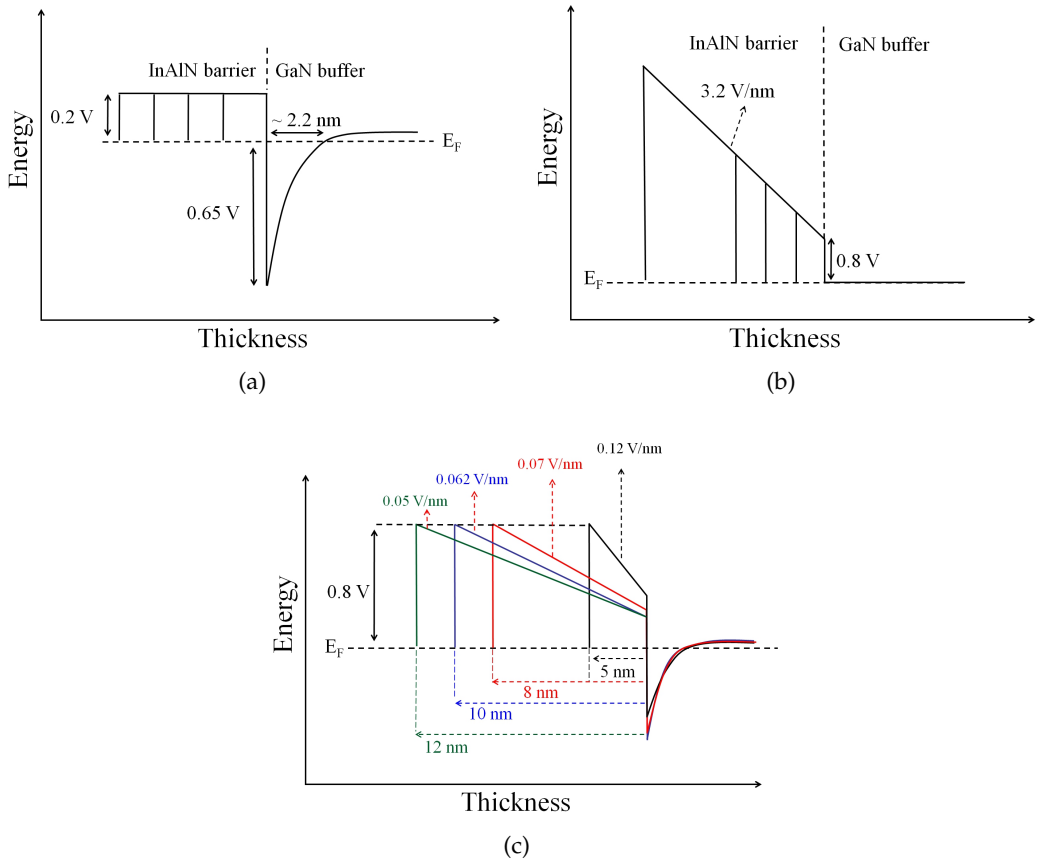


Figure 9: Simulated LM-InAlN/GaN band diagrams for the case of (a) a fully undepleted surface resulting in a flat band in the barrier (b) fully depleted surface or no source of electrons to provide for the channel, resulting in a flat band in the buffer (c) with limited density of donor like surface traps, equal to the polarization discontinuity, at an energy of 0.8 eV below the conduction band.

the channel exists and no 2DEG is formed. The band diagram of this case is as shown in Fig. 9b. However, the constant electric field in the barrier will decrease with increasing barrier thickness and to keep the conduction band discontinuity constant, the relative position of the Fermi level will drop, or in other words the traps will become closer to the Fermi level, and at a certain thickness the traps will cross the Fermi level, and the ionized electrons are driven to the channel by the polarization field partially screening the polarization and leaving behind a positively charged trap. ϕ_s will then be pinned to the trap energy level. For AlGaN/GaN the $d_{barrier}$ where the channel starts to form is estimated to be around 3 nm [2]. It is very difficult to estimate this value for the InAlN case since even for barriers as thin as 2 nm the channel is already formed [52]. At such very thin barriers it is not clear whether the 1 nm AlN spacer starts to play a role in forming the channel. Quantum confinement effects have to be included in the simulations.

Since the trap energy is assumed to be a single level, all the traps will be ionized at once when the mentioned barrier thickness is reached, and ϕ_s becomes pinned. Now, if the surface trap density is infinite, N_s will increase with increasing $d_{barrier}$ (according to equation 2.8), up to the value when N_s equals $\sigma_{pol,interface}$. Until this point the surface potential will be pinned to the trap energy level. But increasing the thickness further will cause more electrons to move to the channel and thus more screening of the polarization occurs, until the equilibrium case shown in Fig. 9a is reached. However, beyond this point any further increase in the barrier thickness will lead to more traps to be ionized. But without the driving force of the polarization field, N_s will start to drop, a case comparable to the GaAs case. This was not observed in the experimental Hall data up to thicknesses of 33 nm.

To account for this behavior, an additional assumption, in contrast to standard models, is added by considering a limited trap density equal to the polarization charge discontinuity. This assumption will lead to a similar N_s dependency as the case of infinite trap density, but with a lower increase rate for the same surface potential, up to the value when N_s equals $\sigma_{pol,interface}$. Increasing the barrier thickness further than this point will decrease the voltage drop across the barrier but no increase in N_s will occur since there are no more available donor traps, and N_s will remain constant. The simulated data of N_s vs. $d_{barrier}$ superimposed on the experimental data are shown in Fig. 8 and compared to the $Al_{0.34}Ga_{0.66}N$ /GaN case presented in [2]. A surface trap energy between 0.8 eV and 1.0 eV gives the best fit to the experimental data thus indicating a surface potential of the free surface which is significantly lower than the reported 1.6 eV for $Al_{0.34}Ga_{0.66}N$ or 1.9 eV for AlN. As can be also seen in the figure, due to the lower surface potential and the higher polarization discontinuity the LM-InAlN/GaN heterostructure can provide higher N_s values, compared to the AlGaN/GaN, even for very thin barriers, which enables high current HEMTs with high aspect ratio. The simulated band diagrams of barriers with 5 nm, 8 nm, 10 nm and 12 nm are shown in Fig. 9c.

Although this model, using the assumption of a limited trap density equal to the polarization discontinuity, can fit the observed experimental data, it does not specify the nature of the surface traps or why they are limited to the density of the polarization discontinuity. However, it maybe speculated that the trap formation needs a force, which must be internal, and linked to the polarization field. It is worth noting that this assumption was also used to explain the case of AlN/GaN barriers in [53] where the surface trap density was found to be very close to $\sigma_{pol,interface}$ and a physical atomic arrangement model was suggested to explain this behavior.

So far, only a free surface case is considered in the simulations, where ϕ_s can not be modulated. However, ϕ_s can be modulated using a gate bias but this still does not apply to the free surface area between the contacts. And thus the direct implication of the surface potential pinning is the introduction of a current limiter. The depletion of N_s with decreasing the barrier thickness is in turn the natural way to obtain an enhancement mode HEMT, as will be shown in the next section. Excessive barrier downscaling will eventually cause the loss of N_s. Moreover, the surface traps responsible for the surface potential can not be eliminated, otherwise no channel will form. The surface depletion

can however be mitigated by using a heterostructure with an initially higher polarization discontinuity, thus despite the surface depletion, a fairly large N_s value can still be obtained for relatively thinner barriers. This is done by increasing the Al content as (discussed in section 2.1) and the case presented here for the LM-InAlN/GaN (see Fig. 8) is certainly in that direction, aiming ultimately to use an AlN barrier. Another possibility is to have a heterostructure with an initially low surface potential, which also applies to the case of LM-InAlN/GaN compared to AlGaN/GaN. Thus the LM-InAlN barrier presents a good compromise between the surface potential, the polarization discontinuity and the barrier thickness that can be used. Other technological solutions can also be employed to mitigate the surface depletion effects, as will be presented later (see section 3.3.1). However, the existence of surface traps near the gate high field region in the HEMT also causes an intrinsic limitation to the HEMT power performance known as current collapse, which can not be eliminated but the onset of its effect relative to the operating voltage and frequency can be delayed, allowing higher operating voltages and frequencies. Before discussing the intrinsic HEMT limitations, and to better understand the barrier downscaling effect on the HEMT performance, it is necessary first to introduce the basic HEMT model, from which the HEMT technological and intrinsic limitations are discussed.

2.3.2 *Basic model of GaN HEMTs*

The basic level analysis of the I-V characteristics of a HEMT (although basically a Metal Semiconductor Field Effect Transistor (MESFET)), maybe similar to a Metal-Oxide-Semiconductor FET (MOSFET) using a gradual channel approximation [54] taking into account two variations:

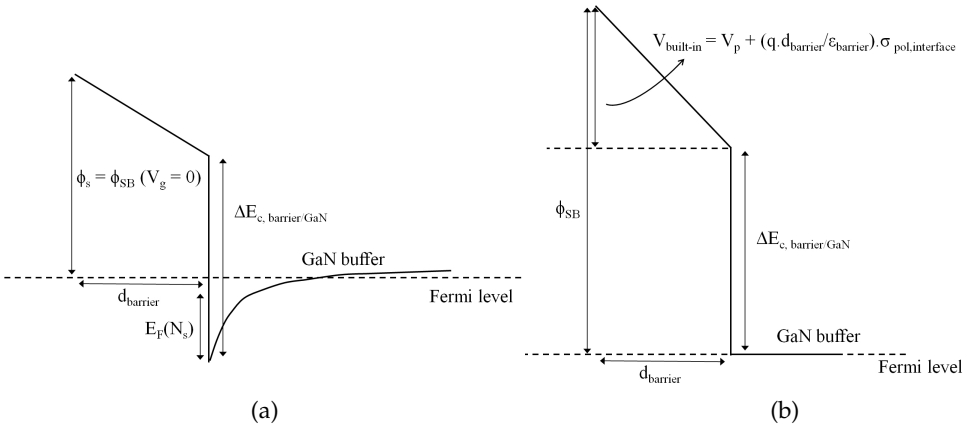


Figure 10: Schematic of HEMT band diagram under the gate (a) in case of no applied gate voltage ϕ_s equals the contact potential ϕ_{SB}, and (b) ϕ_s is controlled by the gate voltage, as shown here for the case of a pinched-off channel.

- The capacitively coupled gate modulates the channel charge carriers by altering the built-in field in the barrier according to equation 2.8. However, under the gate ϕ_s

equals the contact potential ϕ_{SB} (if no gate voltage is applied, see Fig. 10a), and is controlled by the gate voltage (V_g), in which case ϕ_s in equation 2.8 is written as:

$$\phi_s = \phi_{SB} - V_g \tag{2.9}$$

In contrast to MOSFETs, the gate voltage can not be forward biased more than the barrier flat band condition shown in Fig. 9a without excessive leakage currents, specially if thin barriers are used, due to tunneling leakage currents.

- The pinch-off voltage (V_p) is defined for the case that N_s equals zero ($V_p = V_g \mid_{N_s=0}$)(see also Fig. 10b). This can be derived by replacing equation 2.9 in equation 2.8 and setting it to zero noting that $E_F(N_s)$ equals zero at pinch-off, yielding:

$$V_p = V_{Built-in} - \frac{q \cdot d_{barrier}\sigma_{pol,interface}}{\varepsilon_{barrier}} \tag{2.10}$$

where $V_{Built-in}$ is the built-in voltage, and is equal to $\phi_{SB} - \frac{\triangle E_{c_{barrier/GaN}}}{q}$, and is defined by the gate and heterostructure material parameters. Thus V_p for a given GaN HEMT can be changed by changing $d_{barrier}$ as will be shown later in chapter 3 for LM-InAlN/GaN HEMT.

Now the drain-source current (I_{DS}) dependence on applied drain and gate voltages (V_{DS} and V_{GS}) following the gradual channel approximation as in a MOSFET, can be written as:

$$I_{DS} = \mu C_{GS}\frac{W_G}{L_G}\left[(V_{GS} - V_p)\cdot V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.11}$$

where C_{GS} is the gate-source capacitance, which equals the barrier capacitance ($C_{barrier}$) in case of HEMT, and given by:

$$C_{GS} = \frac{\varepsilon_{barrier} W_G L_G}{d_{barrier}} \tag{2.12}$$

where W_G and L_G are the gate width and gate length respectively. Here, the term $d_{barrier}$ neglects the 2DEG charge centroid and quantum capacitance, but needs to be corrected to the effective $d_{barrier}$ in case of a very thin barrier.

The saturation drain current (I_{DSS}) independent of V_D can be obtained by deriving equation 2.11 with respect to V_D and setting it to zero yielding:

$$I_{DSS} = \mu C_{GS}\frac{W_G}{L_G}(V_G - V_p)^2 \tag{2.13}$$

and thus the transconductance (g_m) in the saturation region has no saturation velocity (υ_{sat}) limit and is a function of $1/L_G$, expressed by:

$$g_m = \frac{dI_{DSS}}{dV_G} = \mu C_{GS}\frac{W_G}{L_G}(V_G - V_P) \tag{2.14}$$

However, these equations represent the long channel approximation and are valid only in the constant mobility regime where the electron velocity is below the saturation velocity ($v < v_{sat} = \mu E_c$), where E_c is the critical field in the channel approximated by $E_c = \frac{V_c}{L_G}$. Due to the high mobility in GaN HEMTs, the saturation velocity can be reached even for small drain biases and hence the device will operate in the velocity saturation mode. I_{DSS} can be then written using a two-piece linear approximation [55, 56], ignoring hot electron overshoot and phonon scattering, as:

$$I_{DSS} \approx W_G C_{GS} (V_G - V_p) v_{sat} \tag{2.15}$$

and the transconductance is not a function of L_G , and expressed by:

$$g_m = W_G C_{GS} v_{sat} \tag{2.16}$$

thus the linear dependence of the transfer characteristics on V_G, in contrast to long-channel devices. Moreover, the cut-off frequencies of the device, neglecting extrinsic parameters, can be approximated by [54]:

$$f_t \approx \frac{g_m}{2\pi (C_{GS} + C_{GD})} \tag{2.17}$$

and

$$f_{max} = \frac{g_m}{2\pi C_{GS} \sqrt{4(R_S + R_i + R_G)(g_d + g_m(\frac{C_{GD}}{C_{GS}}))}} \tag{2.18}$$

which for the case of small resistances can be reduced to:

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi R_G C_{GD}}} \tag{2.19}$$

As in GaAs HEMTs, the natural way to increase the device cut-off frequencies is to aggressively scale down the device dimensions [57, 58] in addition to better channel confinement [59, 60, 61, 62]. As can be seen from equations 2.17 and 2.14 and neglecting the parasitic capacitances, f_t is an inverse function of L_G. Thus reducing L_G would yield higher f_t. However, this approach is limited by the short channel effects known for MOSHEMTs [54], where the fringing field capacitance can not be neglected anymore and the gradual channel approximation becomes invalid. In the case of GaN HEMTs, which reach saturation velocity at fields around 14 kV/s (and thus velocity overshoot also starts to play a role), the lateral field at the drain side makes the effective gate length asymmetric, and in total larger than the metallurgical gate length [63]. Thus to keep the internal field distribution the same, down scaling of the barrier is also required maintaining a certain aspect ratio L_G / $d_{barrier}$. In other words, getting the gate closer to the channel. This effect has been simulated for AlGaN/GaN HEMTs in [64] and observed experimentally in [65] where

a universal minimum aspect ratio of 15 was found to be a limit to avoid short channel effects, despite the multiple sample sources and barrier thicknesses. For power amplifiers, increased operation frequency has another limitation on the output power due to current collapse effect that will be discussed separately in section 2.5.1.

For linear operation of a class-A amplifier the output power (P_{out}) can be estimated as [66]:

$$P_{out} = \frac{1}{8} I_{DS_{max}} \left(V_{DS_{|V_{Br}}} - V_{knee} \right) \tag{2.20}$$

Where V_{knee} is the knee voltage defined at the onset of current saturation and the factor $\frac{1}{8}$ is due to undistorted sinusoidal current waveform of the class-A amplifier.

In the case of hard gate overdrive conditions (well into saturation and well into pinch-off) the microwave current waveform is that of a half wave rectifier, and the output power is given by [66, 67]:

$$P_{out} = \frac{1}{4} I_{DS_{max}} \left(V_{DS_{|V_{Br}}} - V_{knee} \right) \tag{2.21}$$

Before discussing the power performance of GaN HEMTs, it is necessary to describe the breakdown mechanisms, in on-state and in off-state. In the on-state, the breakdown occurs through an increased gate leakage current. The gate leakage mechanisms in GaN HEMTs are dominated by trap-assisted tunneling, specially when using thin barriers (approaching the tunneling limit). These traps can be located at the barrier/GaN interface, or in the barrier due to un-intentional barrier doping or can be due to defects. A detailed analysis of the gate leakage mechanisms is given in [68]. Here only short outline of the most important phenomena will be given. Considering the case of a single barrier heterostructure, a general expression of the tunneling current between the gate contact and the source contact across the barrier, conducted by the 2DEG is given by:

$$J_T = q n v_e T(E) \tag{2.22}$$

Where J_T is the tunneling current density, n is the electron concentration, v_e is the electron velocity and $T(E)$ is the transmission probability. Although this case is simplified (since actual HEMT structures contain an AlN spacer, thus resembling a double barrier), equation 2.22 is sufficient to describe the main features of the gate gate diode characteristics shown in Fig. 11. It should be noted that the asymmetry of the forward bias and reverse bias characteristics is not considered in this schematic.

In forward bias direction, increasing the gate voltage modulates the barrier height, going from a trapezoidal shape to a flat band condition in the barrier. $T(E)$ in eqn. 2.22 will then decrease (i.e. the tunneling electron wavefunction sees an effectively thicker barrier), but is counter balanced by an increase in the electron concentration in the channel (due to accumulation). However, since v_e increases with voltage (constant mobility regime), J_T

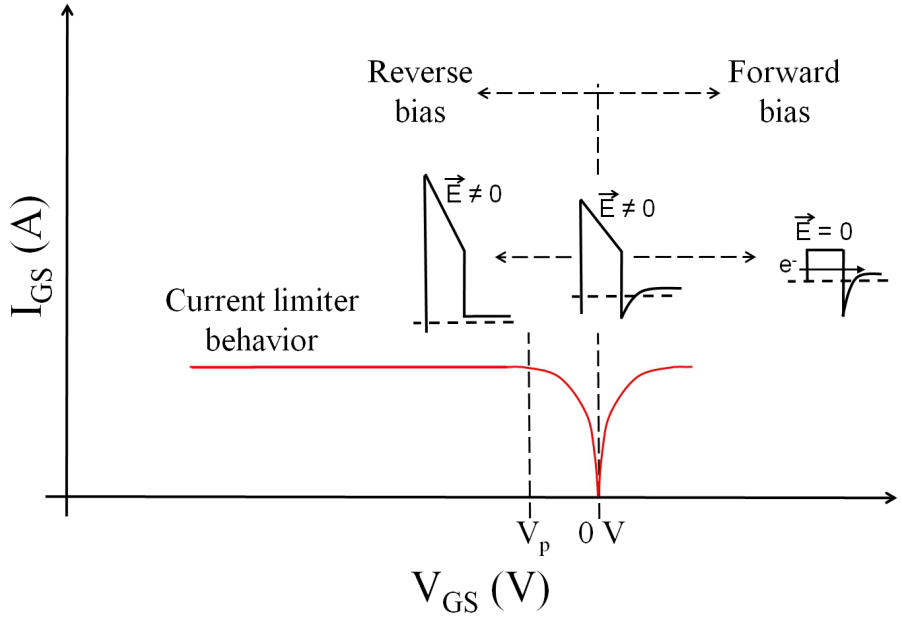


Figure 11: Schematic of gate diode characteristics for a single barrier HEMT. The leakage current in the forward direction follows a tunneling mechanism, and similarly in the reverse bias direction up to channel pinch-off, where the characteristics resemble a current limiter.

will eventually increase, until sufficiently high enough leakage current destroys the gate contact.

When reverse biasing the gate, the same behavior is expected (but here *T(E)* will be increasing, counter balanced by a decreasing electron concentration) and the reverse leakage current will increase up to the point where the channel is pinched-off. Naturally, due to its tunneling nature, the leakage currents will also scale with the barrier thickness as will be shown in section 3.3.1.

Up to pinch-off, the on-state breakdown and reverse bias leakage current are vertical field phenomena. Once the channel is pinched-off, the lateral fields can not be ignored anymore, and the surface properties will dominate the HEMT behavior. After pinch-off, the diode characteristics exhibit a current limiter behavior, and the leakage current is conducted laterally at the surface of the barrier, through hopping mechanism. At this stage, off-state breakdown will occur through an avalanche mechanism, occurring at the high field region at the gate edge toward the drain.

If power is to be maximized, a maximum of $I_{DS_{max}}.V_{Br}$ should be targeted. However, according to the lateral spreading model [17], since $I_{DS_{max}} \propto N_s$ and $V_{Br} \propto \frac{1}{N_s}$, then a constant power density is expected independent of N_s. Thus for a given heterostructure configuration, maximizing V_{Br} is a key to maximizing power. One would expect then relatively small breakdown voltages for GaN HEMTs (with its high N_s), as in the case of GaAs. However, this is not the case observed, and indeed high breakdown voltages up to 1200 V have been demonstrated [69]. Clearly, to get a high breakdown voltage in the lateral mode, the channel between the gate and drain has to be depleted. This occurs by

neutralizing the surface donor charge, and consequently the channel charge, by lateral charge injection. But in this case, injection should be fast enough to follow the applied signal voltage, otherwise the HEMT power performance will suffer from the current collapse phenomena. This topic will be discussed separately in section 2.5.1.

The previous sections present a discussion on the importance of the barrier thickness and the surface states as limiting factors to the HEMT performance. The limitations faced by GaN HEMTs can be divided into two categories, technological limitations and intrinsic limitations. The technological limitations can be addressed by several technological solutions and design modifications, like recesses, barrier or buffer doping, cap layers, field plates, gate dielectrics, which can be applied to all polar heterostructures regardless of the composition. On the other hand, the intrinsic limitations, namely the current collapse and self heating, apply to all heterostructures (regardless of it composition) and can not be eliminated but rather compromised. However, controling these two intrinsic limitations rely on two basic rules, controlling the high field region near the gate, by optimizing the surface electronic conditions, and designing an efficient heat management solution.

2.4 Technological limitations: Barrier scaling, thermal and chemical limitations

The barrier scaling effects (in the case of a pinned surface potential) on the GaN HEMT performance according to the previous sections represent most of the technological limitations and can be summarized as the following:

- $I_{DS_{max}} \propto N_s \propto d_{barrier}$ and $V_p \propto \frac{1}{d_{barrier}}$ (see equations 2.8,2.10 and 2.15).
- $f_t \propto \frac{1}{d_{barrier}}$ (see equations 2.16 and 2.17)
- $P_{out} \propto I_{DS_{max}}.\, V_{Br}$ (see equation 2.20).

Thus it is a conflict in design rules to aim at maximizing P_{out} and f_t using the same barrier thickness and planar HEMTs design. In this case the maximum P_{out} and f_t product can be achieved by choosing a thin barrier of an alloy with a high polarization discontinuity and at the same time a low surface potential. As was seen before, the LM-InAlN provides such an advantage. For other heterostructures like AlN and AlGaN the technological limits are addressed by using the thickest possible barrier, thus minimizing the surface potential effect, and at the same time employing a gate recess to maximize the transconductance and the cut-off frequencies, in addition to controlling the high field region using field plates.

Indeed these solution have been applied to many GaN HEMT designs, like using AlN as a barrier material [70, 71, 72, 73, 74], maximizing V_{Br} by spreading the high field near the gate region using a T-gate or a slanted gate [75, 76, 77, 78, 79] and by reducing parasitic leakage currents in the buffer [80]. The buffer leakage can be suppressed through the optimization of buffer growth conditions yielding highly insulating buffers [81, 82, 83, 84, 85, 86]. In addition, suppressing other leakage paths is also important, like suppressing the leakage current of the Schottky contact on the Mesa edge of the HEMT [87, 88, 89] and improving the mesa isolation of the devices [87, 90, 91]. Reducing V_{knee} is also essential in terms of power. This can be done by reducing the gate-source resistance

(R_{GS}) by reducing the gate-source distance and by reducing the contact resistance (R_c). Due to the tunneling nature of the ohmic contacts [92, 93] a contact recess could be employed [74]. Another approach used was the selective doping of the access regions [94], or using an n^+-GaN cap [95] or ohmic contact region regrowth [96, 97].

Additionally, a recess can be employed as mentioned before. Indeed a low damage recessing process (to avoid nonlinearities in R_C and g_m [98] and undesired kink effects [99]) have been applied to AlGaN/GaN devices in [100] yielding an f_t of 70 GHz and an f_{max} of 300 GHz. Gate recessing was also employed on LM-InAlN/GaN gaining a record g_m of 800 mS/mm [101]. However, even without recesses, using a thinner barrier but with a lower surface potential (like LM-InAlN) or a higher polarization discontinuity (like AlN) could increase the frequency performance of the device using planar technology only and still maintaining current densities above 1 A/mm. An f_t of 210 GHz could be achieved with a dielectric free passivated LM-InAlN/GaN HEMT [102], an f_t of 144 GHz for LM-InAlN/GaN on Si substrate [103], an f_t of 205 GHz for LM-InAlN/GaN on SiC substrate [104] demonstrating the benefit of a thinner barrier. The frequency limit was even pushed further to an f_t 300 GHz using the LM-InAlN [32] still using a planar technology.

These approaches however have their own limitations. Mechanically, increasing the Al-content increases the piezoelectric polarization (see Fig. 3), which leads to an increase in barrier strain and strain relaxation and a drop in the electron mobility. For example, in AlGaN/GaN this occurs when the Al content exceeds $\sim$ 30% [105]. An exception of course is lattice matched case of LM-InAlN. In addition, due to the stress in the barriers it is not possible to grow thick barriers infinitely without inducing defects or cracking. For MOCVD-grown AlN/GaN for example, barriers thicker than 1 nm already show inhomogeneities [51] and no barriers thicker than 4 nm where reported until recently [106] using MBE growth in addition to in-situ Si_3N_4 passivation to preserve the growth of relatively thick barriers up to 8 nm [106], with promising electrical performance [27, 71, 72, 73, 107]. Even if strained barriers were used at a thickness below the critical thickness of strain relaxation, other effects could still be present due to the presence of the stress. Joh et al. [108, 109] proposed a device degradation mechanism for the non-recoverable damage caused by reversed gate bias, which was later correlated with the intrinsic stress in the barrier through inverse-piezoelectric forces that increases with reverse gate bias until defects and traps starts to generate causing increased gate leakage [110, 111].

Recessing such relatively thick barriers introduces additional challenges, which are two-fold. Firstly, the main concern with recessing (either the barrier or the passivation or the gate dielectric) is causing damage to the polarization of the heterostructure, through a change in stoichiometry by preferential etching. This is seen seen frequently with many recessing and etching recipes [112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122]. Secondly, since gate leakage current in GaN HEMTs in the forward bias are dominated by tunneling mechanism, gate leakage currents will increase. Although leakage currents can be reduced by increasing the Schottky barrier height [68] either by using a metal with a higher barrier height [123, 124] or by increasing the barrier height through changing the surface potential using plasma or wet chemical treatment [125, 126, 127, 128, 129]. This approach however has only a small influence. Another approach is to use a gate dielectric [130] to

form a MOSHEMT [70, 131, 132, 133, 134, 135, 136] but this would increase the the total barrier height again, contrary to the aim. Another approach commonly used for planar AlGaN/GaN structures to suppress gate leakage is adding a (In)GaN cap layer on top of the barrier [137, 138] but here recessing is not possible.

The thermal and chemical limitations are also considered technological since they also can be avoided by choosing a proper heterostructure design, and depend largely on the device operation environment. The chemical stability limitations will present itself, if the HEMT devices will be used as sensors for chemical signals or if the HEMT is subjected to chemically and thermally harsh environment during processing, like Diamond overgrowth. For example, in chemical applications of GaN [139, 140, 141, 142, 143] the barrier itself is not used as the direct sensing component but as an amplifier of the signal provided by the gate as in the case of the Hydrogen sensor presented in [144] or the Ion-Sensitive-FET (ISFET) presented in [40], and the free surface of the device will be protected by a stable passivation. Still the chemical stability of the other HEMT components, like the ohmic and gate contacts metals and the passivation layer, has to be controlled.

The thermal limitations appear during high power operation at room temperature (self heating effects as will be discussed later in section 2.5.2), or if the device is operated at high temperature. The degradation of the device heterostructure can then occur due to reaching a chemical stability limit in non-vacuum conditions or even by surface decomposition in vacuum conditions [145] at elevated device temperatures. In the case of self heating thermal management is the key solution, but in the case of high temperature operation the heterostructure used has to be apriory thermally stable at the operation temperature. Simultaneously, the contact metallization and passivation material should also be thermally stable at the operation temperature.

In addition, and as will be presented in this work for HEMT overgrowth with nanocrystalline Diamond in chapter 4, some technological solutions to intrinsic problems, like the self heating issue discussed in section 2.5.2, require high temperature processing for extended times, thus presenting a high temperature storage stress, often in a chemically active atmosphere. As was discussed in chapter 1, the high thermal conductivity of Diamond is implemented in designing efficient heat management systems, but up to now all attempts have been concentrated on hybrid integration of Diamond and GaN. Direct growth methods, whether growing GaN on Diamond or growing Diamond on GaN, has its own limitations as will be discussed in details in chapter 4. Specifically, growing highly thermally conductive Diamond films on GaN is very thermally and chemically demanding, due to the harsh Diamond growth conditions at temperatures above 700 °C in a hydrogen-radical rich environment required to obtain highly thermally conductive nano Diamond films (see chapter 4). Although this approach presents an optimum heat management solution (as will be shown in chapter 4), it can not be applied to all GaN heterostructures due to the harsh growth environment, which may lead to GaN decomposition [146]. This approach has been successfully applied to the LM-InAlN in this work thanks to the heterostructure high thermal stability. This high thermal stability is mainly due to the absence of stress, and consequently defects in the barrier acting as Ga diffusion paths to the surface, which is known for its chemical instability.

2.5 Intrinsic limitations: Current collapse and device self heating

All of the above mentioned limitations can be addressed by choosing a proper heterostructure and device design. What can not be avoided however, are the intrinsic limitations presented next, which are the main concern for device reliability.

2.5.1 *Main power limitation: Current collapse*

It is always seen that the power performance of the devices falls short of the predicted values of the equation 2.20 and the DC-characteristics of the device, even after optimizing the power related technological parameters described in section 2.4. This is due to the current collapse phenomenon (called also dispersion effects or lag effects) [147, 148, 149, 150, 151, 152]. This phenomenon is inherit in GaN devices since all will have a polarization counter charge residing on the surface, responsible for the channel sheet charge density.

As discussed in section 2.3.2, high breakdown voltages in planar GaN HEMTs can be reached only by eliminating the surface donor charge, in the free surface area between gate and drain. This may occur by lateral charge injection into the surface traps, through a hopping mechanism. However, this will cause current collapse, also known as drain-lag, if the injected charges can not follow the applied voltage frequency swing.

Fig 12 shows a schematic of IV-characteristics of a HEMT in on-state and off-state when the device is operated in DC or RF along a load line between V_{knee} at on-state and V_{BR} at off-state. When the device is in off-state with a high lateral field near the gate edge [153, 154], charge injection into surface states occurs, and trapping of electrons in the donor-like surface traps in the free region next to the gate disturbs the charge neutrality balance thus reducing the sheet channel charge density in that region (see inset at point B in figure) creating a virtual gate [155]. The charge injection mechanism is most likely a hopping mechanism [147, 148], rather than a Pool-Frenkel mechanism, which has an exponential behavior and will not lead to high breakdown voltages as observed in GaN HEMTs. The injection is temperature and field dependent and can be described by an RC element as shown in inset (B) Fig. 12.

This situation can be described as two transistors acting as two current sources, connected in series by a slow gate connection of lateral conduction, and the operation of this dual gate transistor is limited by the current source with the lower output current.

The amount of injected charge depends on the applied voltages (mainly the gate-drain voltage) and on the mobility of the electrons on the surface, which follows a hopping mechanism [147, 148]. This effect of surface charging has been observed experimentally using direct methods like Kelvin probe microscopy [48, 156, 157, 158, 159] and indirectly using other methods like pulse measurements and dual gate measurements. Although some authors refer also to bulk trapping as the cause of current collapse it is more likely the the charging effects occurs on the surface based on two critical observations: firstly, any modification of the surface by passivation or surface treatment alters the current collapse characteristics of the device and secondly, it was shown that GaN/InGaN/GaN do not suffer from charge instabilities, at the chosen test conditions, since the counter charges are

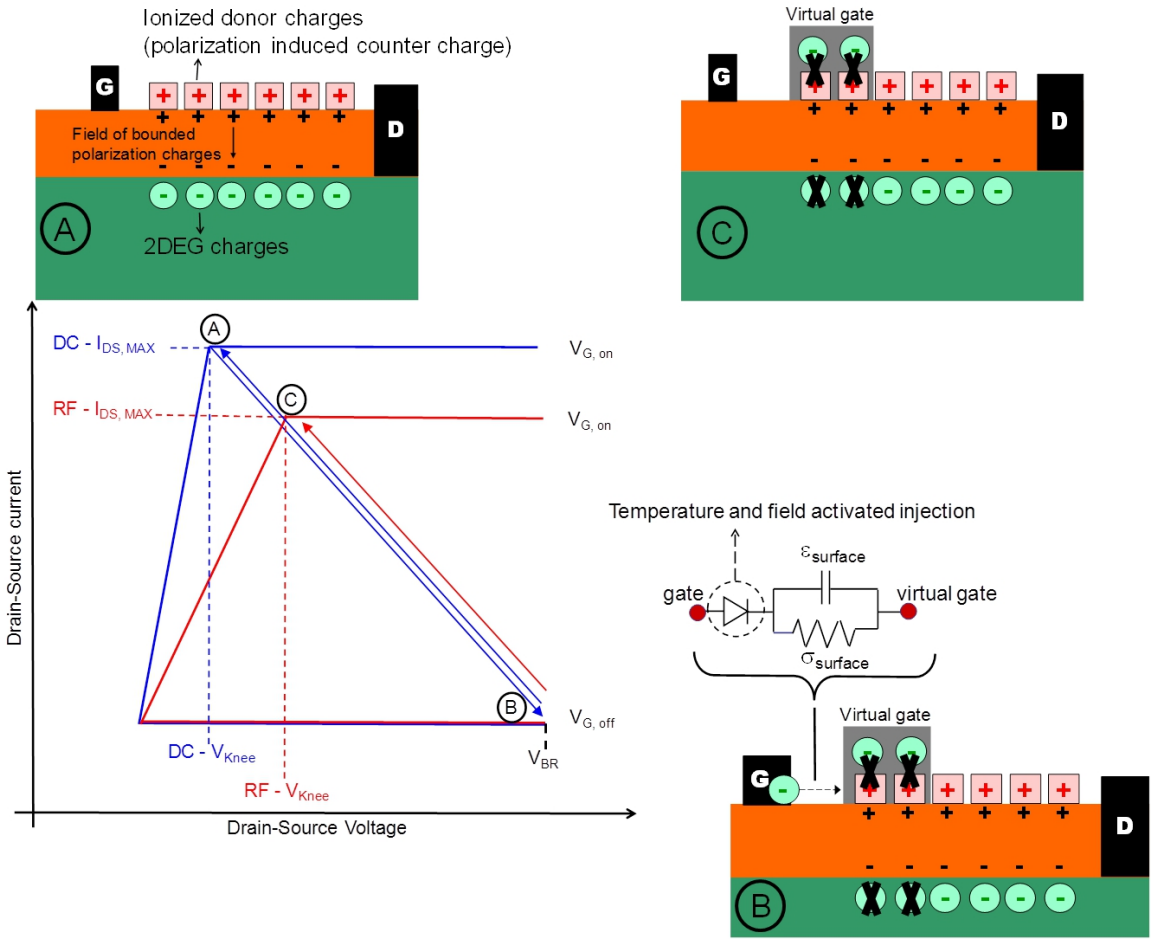


Figure 12: Schematic of I-V characteristics of GaN based HEMT under DC operation and under current collapse conditions. The insets show the surface configuration that leads to the current collapse, due to lateral charge injection in the surface donor traps.

in the bulk and not on the surface [156]. However, in this configuration a recess is needed to obtain a blocking gate contact.

Now, when going back to the on-state the biases and fields are reversed. But for the virtual gate to follow, the surface donor traps have to be discharged again, which is controlled by the RC time constant of the charging path. In DC operation time periods are large enough to allow the full trapping and detrapping to occur and the device will go back to the state depicted at point A. If the RC time constant of the charging/discharging element is larger than the applied frequency, the modulation of the virtual gate lags behind that of the actual gate. Then, the virtual gate will not be removed and the device will suffer from current collapse, as depicted at point C in the figure, with lower maximum current and an increased V_{knee} thus providing output powers below expected values. The current collapse will not occur if the traps are fixed but then the advantage of high breakdown voltage will be lost.

This phenomenon is not observed for the small signal case, and not reflected on f_t or f_{max}, but appear only during power operation mode. Current collapse can also be detected in switching operation and by large signal pulsing experiments. In these experiments pulses on the gate and drain voltages are provided in widths typically in the 100 ns range (corresponding to frequencies up to 10 MHz) where the trapping phenomena is usually observed. A dual gate method to quantify the amount and location of the injected charges was developed by Neuburger et. al [160] using an MOS electrode near the gate region to detect the injected charges. This method was applied to the passivation schemes developed in this work by P. Herfurth in [161] and some relevant results will be shown here also. Moreover, the dual gate method was extended further to study the device instabilities by C. Ostermier in [123]. In addition to these measurements, an observation of the dynamic load lines at RF operation superimposed on the DC characteristics of the device can show the losses suffered from the current collapse.

Thus, to reduce the current collapse effect lateral charge injection must be controlled. This can be done by making the injected charges inaccessible to the surface using passivation [153, 162]. Here injection will still occur since the surface traps should be present in order to form a channel but the charge centroid will be in the passivation and away from the surface depending on the type of passivation and the surface treatment before passivation. As will be shown in this work, for an efficient passivation the charges can be as away as 50 nm from the surface thus reducing greatly the effect of the virtual gate on thin-barrier devices (a barrier of 10 nm LM-InAlN is mostly used here). The use of a lossy dielectric can also increase the mobility of the injected charges and the current collapse will be shifted to frequencies higher than the operation frequency. Using field plates and gate recesses have also been shown to reduce this effect [163, 164]. However, the main factor in reducing the current collapse is to control the charging and discharging properties of the surface traps between the gate and drain. This process starts from the first fabrication steps and up to controlling the passivation deposition precursors [165], as will be shown in this work. Typically used passivation schemes for GaN HEMTs are PCVD Si_3N_4 [23, 26], in-situ or ex-situ MOCVD Si_3N_4 [31, 107, 166, 167, 168]. In addition, used as both passivation and gate dielectric ALD-Al_2O_3 [125, 169, 170, 171, 172, 173] and other high dielectric constant oxides (high-k oxides) [174, 175, 176] like ZrO_2, HfO_2 and MgO [134, 177, 178, 179, 180, 181] have been tested with varying degrees of current collapse reduction.

2.5.2 *Device self-heating*

Device self-heating is a major concern for GaN HEMTs due to its impact on the device performance and reliability. With increasing the device output power, the dissipated power eventually increases leading to an increase in the device temperature. Measurements and simulations have shown that self heating causes a reduction in mobility and drift velocities affecting both the output current and the operation frequency [182, 183, 184]. Moreover, the increased device temperature affects the reliability of the device through accelerated aging and accelerated electromigration of the device metallization leading to device failure

[185, 186]. Thus efficient heat dissipation and management is a key to enable reliable and efficient GaN HEMT power operation.

Several measurement techniques can be used to estimate the device temperature, like microphotoluminescence [186], scanning thermal microscopy [187], photo-current measurements [188], infrared thermography, micro-Raman spectroscopy and a combination of both [189]. It was shown that the high currents of the device can lead to very high device temperatures. It was reported that temperatures above 200 °C were reached in AlGaN/GaN HEMTs with dissipated power of 4 W/mm [185] and a channel temperature up to 700 °C was estimated, using lateral resolved microphotoluminescence, in InAlN/GaN HEMTs with drain bias of only 20 V due to the high current levels (around 2 A/mm) [186]. The device design and packaging plays an important role in the thermal management of the device. But all sources agree that the substrate plays the major role, since it is the major heat path component connected to the package heat sink, thus a substrate with a higher thermal conductivity is more efficient in managing the heat. The commonly used substrates are SiC, Sapphire and Si and it is routinely reported that SiC is the most efficient in terms of thermal management due to its superior thermal conductivity, which lead to the attempt to use Diamond substrates since the crystalline Diamond phase at RT has the highest known thermal conductivity. The substrate type determines the efficiency of heat extraction from the bottom of the device, but heat can also be extracted from the top of the device if the device is coated with a highly thermally conductive material like Diamond. An evaluation of those two approaches for heat dissipation (bottom and top heat dissipation) will be presented in chapter 4 together with the challenges presented in each case and the technological steps to realize it. But first an overview of the HEMTs used in this work, their fabrication technology and temperature stability tests are given in the next chapter.

3

LATTICE MATCHED InAlN/GaN HETEROSTRUCTURE FOR HEMT APPLICATIONS

The previous chapter introduced basic guidelines and limitations to GaN HEMT design and performance. These guidelines can be met by a proper choice of heterostructure and technology parameters. In this chapter the advantages of using InAlN/GaN in lattice matched configuration for HEMT application will be discussed. The chapter starts with summarizing the advantages of the LM-InAlN/GaN HEMT in connection to what was discussed earlier. The evidence for these advantages will be then built up in the following sections, after introducing the basic HEMT fabrication technology and scaling properties used mainly throughout this work.

3.1 Advantages and state-of-the-art of LM-InAlN/GaN HEMTs

The properties of LM-InAlN/GaN heterostructure combine together several advantages allowing a larger degree of freedom in device design to address generic applications using a simple planar technology and allows unconventional process to be applied without compromising the HEMT performance. The LM-InAlN/GaN heterostructure has the following advantages:

- A relaxed barrier with no stress, thus avoiding stress related degradation like what was presented by Joh et. al in [108, 109, 110] (see section 3.4). In fact it was shown that such stress related degradation mechanism are not seen in first experiments for the case of LM-InAlN [190].
- The absence of stress contributes greatly to the high mechanical/thermal stability of the heterostructure. This is the most prominent advantage of this heterostructure which enabled very high temperature storage/operation of the HEMT (discussed in section 3.4) above 500 °C and up to 1000 °C [191, 192, 193, 194, 195] and the application of high temperature processes like thermal oxidation at 800 °C, for surface passivation preparation to address the current collapse phenomena as discussed in section 2.5.1. This will be presented in section 3.5 and in [196, 197, 198]. The high thermal stability also allowed successful nanocrystalline Diamond (NCD) overgrowth at temperatures above 700 °C in H-radical rich atmospheres for heat dissipation purposes to address the self heating problem as discussed in section 2.5.2. This will be presented in chapter 4 and also appears in [40, 42, 199, 200]. Up to now, the processing/operation of HEMTs in this temperature regime is restricted to LM-InAlN.
- The high Al-content (83%) and the relatively low surface potential (below 1 eV) yielded high N_s values (above 2 x 10^{13} cm^{-2}) [50] and high I_{DS} (above 0.5 A/mm) for barriers thinner than 15 nm (discussed in sections 2.3.1 and 3.3.1 and appears

in [201]). This has enabled high aspect ratio devices with high cut-off frequencies (summarized below), and the ability to use gate dielectrics without compromising the aspect ratio [131, 132, 134, 169, 178, 179, 180], and high performance enhancement mode (E-mode) devices to be realized [52, 123, 202, 203].

- The high current densities allowed demonstration of high power densities at high frequencies (summarized below) and low drain voltages, promoting the LM-InAlN as a an alternative barrier material to the conventional AlGaN barrier [24, 39, 191, 204, 205, 206].

Indeed the interest in using this barrier for HEMT applications is evident in the increasing number of publications from several institutes and research groups. Although the technology optimization is not yet as mature as AlGaN/GaN case, key enabling technological parameters, like high quality crystal growth and efficient surface passivation have been developed. A time line summary of the state-of-the-art LM-InAlN/GaN, achieved worldwide on different substrates, in terms of frequency and power performance is shown in table 2. The results presented in this work are comparable to the state-of-the-art results, and the main task in this work concentrates on developing a technology of nanocrystalline Diamond overgrowth on HEMTs that is compatible with these applications.

3.2 Heterostructure growth

The heterostructure can be grown either by Metal Organic Chemical Vapor Deposition (MOCVD) or by Molecular Beam Epitaxy (MBE). Details of these techniques can be found in [215, 216].The main difference between the two techniques is that while MOCVD is an equilibrium process, where the GaN growth is conducted at high temperatures (typically 1050 °C), MBE is a non equilibrium process conducted at lower temperatures (max. 800 °C) but at a much slower growth rate [85, 217]. The difference in the growth temperature might prefer some substrates to others due to the lattice and thermal mismatch between GaN buffers and the typically used SiC, Sapphire or Si substrates. Table 3 summarizes these parameters.

The difference in thermal expansion coefficient and the thermal mismatch to the substrate causes cracking of the grown GaN, while the lattice mismatch causes rotated GaN domains. The growth on non-polar substrates (Si, Sapphire or Diamond) can cause mixed polarity and inversion domains [14, 217]. The dislocations affect the thermal conductivity of the buffer and the mixed polarity affects the polarization and in turn the sheet charge density. Thus using AlN would be the best choice but is limited by the availability of AlN substrates. Instead, AlN buffers grown at low temperature are used between the non polar substrate and the GaN buffer. A view to the state of the art data presented in table 2 shows clearly that the performance of GaN on SiC is superior to Sapphire and Si, but due to the relatively high cost of SiC substrates, growth techniques were optimized for GaN on Sapphire and recently good quality GaN on Si is being used. The unique case of GaN on single crystalline Diamond growth is discussed in section 4.3. The mismatch effects can be reduced by inserting an AlN nucleation layer grown at low temperature between the substrate

Year	Substrate	P_{out} (W/mm)	PAE (%)	V_{DS}, Freq. (V), (GHZ)	Passivation	L_G (µm)	f_t (GHz)	f_{max} (GHz)
2007 [207]	SiC	6.8	34	30 V, 10 GHz	PCVD Si_3N_4	0.25	-	-
2008 [208, 209]*	SiC	5	42	30 V, 10 GHz	PCVD Si_3N_4**	0.25	42	61
2009 [210]	Si	2.5	23	15 V, 10 GHz	PCVD Si_3N_4	0.1	102	104
2009 [194, 196]*	SiC	11.6	37%	20 V, 4 GHz	PCVD Si_3N_4**	0.1	61	112
2010 [104]	SiC	-	-	-	PCVD Si_3N_4	0.055	205	165
2010 [211]	SiC	10.3	51	30 V, 10 GHz	PCVD Si_3N_4	0.25	27	65
2010 [103]	SiC	-	-	-	PCVD Si_3N_4	0.1	144	145
2010 [212]	SiC	5.8	43.6	20 V, 35 GHz	PCVD Si_3N_4	0.16	79	113.8
2011 [102]	SiC	-	-	-	Dielectric free	0.06	210	55
2011 [213]	SiC	-	-	-	PCVD Si_3N_4	0.03	205	220
2011[214]	Sapphire	2.9	28	15 V, 18 GHz	PCVD Si_3N_4	0.225	52	110

Table 2: Time line summary of the state of the art LM-InAlN/GaN HEMT. It should be mentioned that all barriers used are thinner than 15 nm. *Performed in This work. **The $Si_3N_4$is combined with thermal oxidation.

	GaN	SiC	Sapphire	Si	Diamond (single crystal)
Thermal expansion coefficient ($10^{-6}K^{-1}$)	5.59	4.2	7.5	2.59	1.18
Lattice mismatch (GaN/substrate in %)	-	+3.5	-16	-17	26.4
Thermal mismatch (GaN/substrate in %)	-	+25	-24	+54	+300

Table 3: Lattice and thermal mismatch to substrates used for GaN growth. After [9, 14].

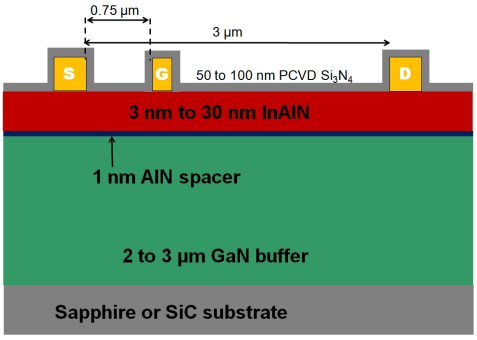


Figure 13: Cross section of the typically used heterostructure and device dimensions.

and GaN along with other techniques that can be found in [218, 219, 220, 221]. High GaN buffer insulation is usually achieved by Fe-doping or C-doping [81, 82, 84, 85, 86, 222, 223].

Most of the LM-InAlN/GaN heterostructures used here were grown by MOCVD on SiC and Sapphire. The GaN buffer thickness used is 2-3 µm grown on an AlN nucleation layer. As in AlGaN/GaN [224, 225] before the InAlN growth a thin 1 nm AlN spacer is introduced. This spacer reduces the alloy interface scattering thus increasing the mobility up to 2 fold [51, 83]. Mobilities up 1200 cm^2/Vs are reached, in the used heterostructures, compared to around 500 cm^2/Vs for heterostructures without the spacer which were previously used [226, 227]. The grown InAlN was originally used for optical applications (Bragg reflectors and in GaN based laser diodes [20]), but the growth optimization of both the barrier and the buffer insulation was gradual during this work. Fig. 13 shows a cross section of the typically used heterostructure in this work along with the device dimensions routinely fabricated. Barriers ranging from 3 nm to 30 nm were investigated but most of the work was performed using a 10 nm barrier on SiC substrate. The Al content varied slightly between 81% and 84% depending on the buffer template of supplier to achieve the lattice match configuration, confirmed by the growers using High Resolution X-Ray Diffraction (HRXRD). The defining features of the heterostructure and the device dimensions will be pointed out later.

3.3 HEMT basic fabrication technology and characterization

The early stages of the work concentrated on defining the potential and limits of InAlN/GaN heterostructures, with variable Al content and variable barrier thickness using a simple planar fabrication technology. This was used for comparison and qualification between the different heterostructures. Later on, a decision to concentrate on using the 10 nm barrier LM-InAlN/GaN (including the 1 nm AlN spacer) grown on SiC substrates was made. This choice was based on the heterostructure properties, which will be discussed in this chapter and the thermal stability under NCD growth that will be discussed in chapter 4.

The following is a summary of the standard HEMT fabrication steps used routinely. All fabrication steps are performed in a continuous routine and thus the choice of the technology is limited by the available technological facilities. Modifications of this process according to the technological needs will be mentioned in place. Except for the optical lithography resist developer, the use of acidic or basic solutions was avoided (unless intentionally applied as will seen shortly) to avoid changing the heterostructure properties through uncontrolled modification of the surface potential. The lithography process details and materials are listed in the appendix.

The mask set used enabled the fabrication of a matrix of devices with variable width (2 x 25 µm, 2 x 50 µm, 2 x 100 µm and 2 x 200 µm), variable source-drain distance (3 µm and 4 µm) and variable gate lengths (0.5 µm, 0.25 µm, 0.1 µm). Dedicated measurements structures (TLM structure, 4-point Van der Pauw, vertical diodes and open and short calibration pads for RF measurements) are also on the same mask set. Mostly used was the device dimensions shown in Fig. 13.

Device isolation was achieved by Ar- dry etching in a plasma sputter-etch chamber. Although removal of only the barrier is sufficient for device isolation, an etch depth of 250 nm to 400 nm was used to enable proper mask alignment in the next optical lithographic step. Ohmic contacts were patterned by lift-off optical lithography. The samples were then dipped for 15 minutes in HCl:H_2O solution (1:1 ratio and heated to 70 °C) for native surface oxide removal to ohmic metallization deposition. This step proved crucial in obtaining linear ohmic contacts routinely. Ti/Al/Ni/Au (30 nm/200 nm/40 nm/100 nm) metallization was deposited in an electron beam (E-beam) evaporator. After lift-off the ohmics were annealed in a Rapid Thermal Annealing (RTA) chamber in nitrogen atmosphere at 850 °C for 30 seconds. Due to the tunneling nature of the ohmic contact, provided by TiN surface defects generated at the annealing step [92], the contact resistance depends largely on the barrier thickness as will be seen later. However, it was found that long time annealing improved slightly the contacts resistance probably due to enhanced alloy mixing but this step was not usually used, since it requires a controlled process in a vacuum chamber to avoid surface oxidation [228]. Controlled surface thermal oxidation at 800 °C in O_2 atmosphere was performed on the LM-InAlN HEMTs for surface passivation purposes. This process will be discussed in detail in section 3.5. For quick heterostructure evaluation this step was skipped. E-beam evaporated 50 nm Ni / 100 nm Au gates were defined by E-beam lithography with the dimensions mentioned above. Devices were

passivated with PCVD Si_3N_4 films deposited at 300 °C with varying thicknesses between 30 nm and 200 nm using Silane and Ammonia precursors. Eventually the passivation process were varied according to the specific experiment as will be shown later. Contacts pads were opened in a Reactive Ion Etching (RIE) chamber using CF_4 plasma.

DC measurements and high temperature measurements were monitored to characterize the fabricated HEMTs. After technology optimization, selected microwave devices were characterized by small signal s-parameter, large signal load pull measurements and pulse measurements. High resolution TEM (HR-TEM) analysis were used to analyze specific structures like the thermally oxidized InAlN, the ohmic and gate contacts or the NCD overgrown HEMTs. This set of experiments was used to define the features of HEMTs with variable barrier thickness and variable passivation and metallization schemes.

3.3.1 *Barrier scaling properties*

Although the surface potential could be underestimated in the simulations presented in section 2.3, due to uncertainty in the conduction band offset value, the barrier scaling effects are present experimentally and affect the HEMT properties as will be discussed shortly.

The scaling properties with barrier thickness of the LM-InAlN/GaN HEMT used in this work are discussed in [192, 201, 229] but the main features of the barrier down-scaling will be presented here, since they will serve as guidelines in identifying degradation effects of the HEMT due to high temperature processes like the thermal oxidation of the barrier or the high temperature deposition of an NCD top heat spreader. Figures 14 and 15 summarize the barrier down-scaling effect on HEMTs grown on Sapphire substrates with 2 µm GaN buffer and 1 nm AlN spacer with variable LM-InAlN barrier thicknesses down to 3 nm. The planar device fabrication followed the steps described in section 3.3.

The dependence of $I_{DS,max}$ (with a fully opened channel with V_g = +2 V) on $d_{barrier}$ shown in Fig. 14 follows the trend of N_s dependence on $d_{barrier}$ shown in Fig. 8. The surface potential of the free surface can only act in the source/gate and gate/drain access regions mainly as parasitic current limiter on the FET open channel current. The reduction of N_s underneath the gate at fully opened channel is not expected, if no stress is added to the barrier, in particular for thin barriers. However, this correlation is still indirect and not quantitative. The insets of the figure show the DC-output characteristics of HEMTs with 15 nm barrier and 3 nm barrier. For thick barriers $I_{DS,max}$ is approx. 1.8 A/mm and decreases to 0.6 A/mm for the 3.0 nm barrier which is still significantly high. It can be also seen that current compression, indicating an N_s limit is not seen in the thin barrier device prior to forward gate breakdown. Thus, for thin barriers $I_{DS,max}$ is still gate barrier limited and not N_s limited. After PCVD Si_3N_4 passivation $I_{DS,max}$ increased specially for thin barriers indicating reduction the surface potential in the access regions (which also enhances the RF performance of the device as was discussed in section 2.5.1). In addition to the high aspect ratio, thin barriers can also provide a reduction in the contact resistance (see Fig. 15a). Moreover, V_P scales linearly with the barrier thickness (see Fig. 15b) and an enhancement mode of operation would be reached for a total barrier thickness of 2.0

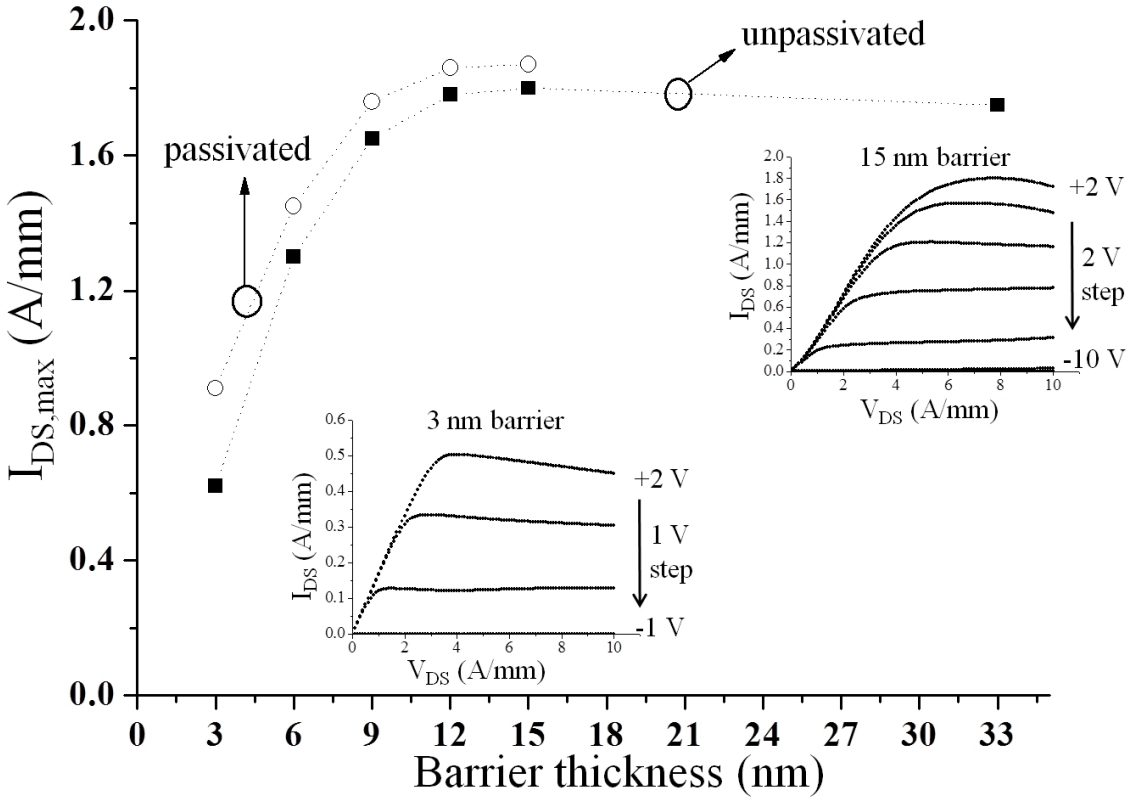


Figure 14: The barrier down-scaling effect on the HEMT characteristics causes a decrease in $I_{DS,max}$ and increase in g_m (not shown here). PCVD Si_3N_4 passivation seems to reduce the surface potential effect. However, due to the relatively small surface potential of LM-InAlN/GaN HEMT, fully functional devices can be obtained with barriers as thin as 3 nm.

nm, when using a Ni gate. Indeed, C. Ostermaier in [52] showed that this is the case by demonstrating an E-mode HEMT with a barrier thickness of 2 nm. The depletion of the access regions in this case was prevented using an n^{++}- GaN cap layer.

The drawback of aggressive barrier scaling discussed in section 2.4 would be the increase in the gate leakage current as shown in Fig. 15c. In this work a novel method of barrier thermal oxidation was used to obtain a high quality gate dielectric that allowed a reduction in the gate leakage current and at the same time served as an important step in surface preparation for efficient passivation. Since this process is performed at 800 °C, it requires a very high heterostructure thermal stability, which the LM-InAlN/GaN could provide. The heterostructure stability is discussed next in section 3.4.

The barrier scaling properties presented here lead to the choice of 10 nm barrier to be largely used for subsequent power HEMT fabrication. The 10 nm barrier is thick enough to provide a high N_s close to the maximum value but not too thick for a relatively low contact resistance and the device has a transconductance around 300 mS/mm which is sufficient

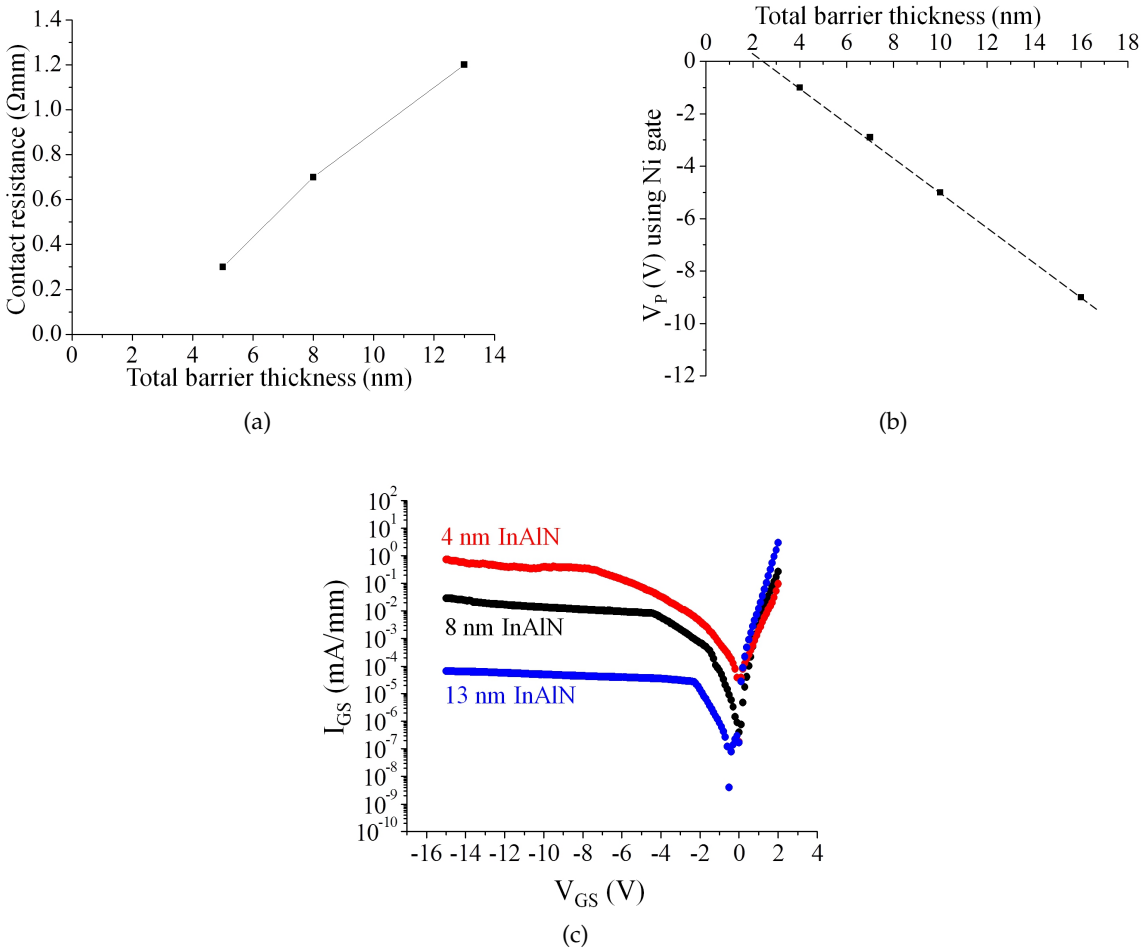


Figure 15: The barrier down-scaling also causes a (a) decrease in the contact resistance (b) decrease in the pinch-off voltage and (c) increase in the reverse gate leakage current.

for operation frequency in the GHz regime. The gate leakage and the surface passivation were optimized using the thermal oxidation method as will be discussed in section 3.5.

3.4 Thermal stability and high temperature operation of LM-InAlN/GaN HEMT

Since the demonstration of LM-InAlN/GaN HEMT short operation at 1000 °C in 2006 [39] the very high thermal stability of the LM-InAlN/GaN layer has been identified as one of its most attractive feature , which would indicate not only reliable operation at high power but would also enable the application of unconventional processes at high temperatures without degrading the device performance. It would also enable operation at very high temperatures above 600 °C not accessed so far by any other material. A lot of effort was spent in optimizing the device design for high temperature processing/application and the thermal stability of the HEMT was evaluated using storage or operation tests at high

temperatures. The HEMT properties developed in the previous sections along with direct observations with TEM cross sections was used to identify possible degradation mechanism in the HEMT structure. These guidelines are as the following:

- In a high temperature storage test, a change only in $I_{DS,max}$ indicates a modification of ϕ_s by a modification of surface state distribution at high temperature. If the HEMT is passivated and the change still occurs this means that the passivation should be modified for better protection of the surface. The change in ϕ_s can however be intentional like in the case of obtaining an E-mode LM-InAlN/GaN HEMT with a 5 nm barrier, by modifying ϕ_s through Fluoride plasma treatment localized under the gate, to decrease the density of the surface counter charge and consequently the sheet charge density. The results of this study will not be discussed here but can be found in [202].

- A decrease in the R_C indicates either diffusion of the contact metal in the barrier or enhanced alloy mixing. The later case is more probable since the barrier exhibits a ceramic-like stability and no metal diffusion either from the ohmic or gate contact was observed by HR-TEM cross sections. This was also shown for the HEMT operated at 1000 °C using a Ni gate, where intermixing of the Ni and Au contact metals occurred, but no diffusion of either metals in the barrier was seen in HR-TEM images.

- An increase in V_p would indicate gate sinking. This case was not observed as mentioned above, but could be confused with the case of modifying $\phi_s$under the gate like what was shown in [230].

If I_{DS}, or N_s, and V_p are preserved, this means that the basic properties of the heterostructure, namely the polarization and the barrier thickness, are preserved and the degradation seen in the HEMT characteristics is more likely due to either degraded ohmic or gate contact metallization or degraded passivation or both. This is demonstrated for example in the case of storage tests at high temperature. In this experiment PCVD-Si_3N_4 passivated HEMTs were stored under vacuum at temperatures from 500 °C to 1000 °C in steps of 100 °C for 30 minutes. The HEMTs were characterized after each heating step after cooling to room temperature. Fig. 16 shows the DC characteristics of the tested HEMTs (15 nm and 3 nm barriers) after cooling down from 1000 °C. As can be seen, even for the HEMT with 3 nm barrier the device characteristics are largely unchanged, which indicates very high thermal stability of the heterostructure. The change in the access resistance for the 3 nm barrier case is due to changes in metal alloying of the ohmic contact. But most importantly, the gate diode characteristics did not change (see Fig. 16c), nor the pinch-off voltage shifted, which (if occurred) could be easily seen in a barrier as thin as 3 nm.

This experiment indicates that the heterostructure is capable of handling process steps up to 1000 °C for elongated times in vacuum conditions. However, any alloying instability of the metals will usually lead to degradation effects, if the device is operated at high temperatures. Electromigration of soft metals, like in the ohmic contact metallization stack, namely Au and the non alloyed part of the Al film, will be amplified during operation at high temperatures. The flow of metal on the device surface can then short circuit the

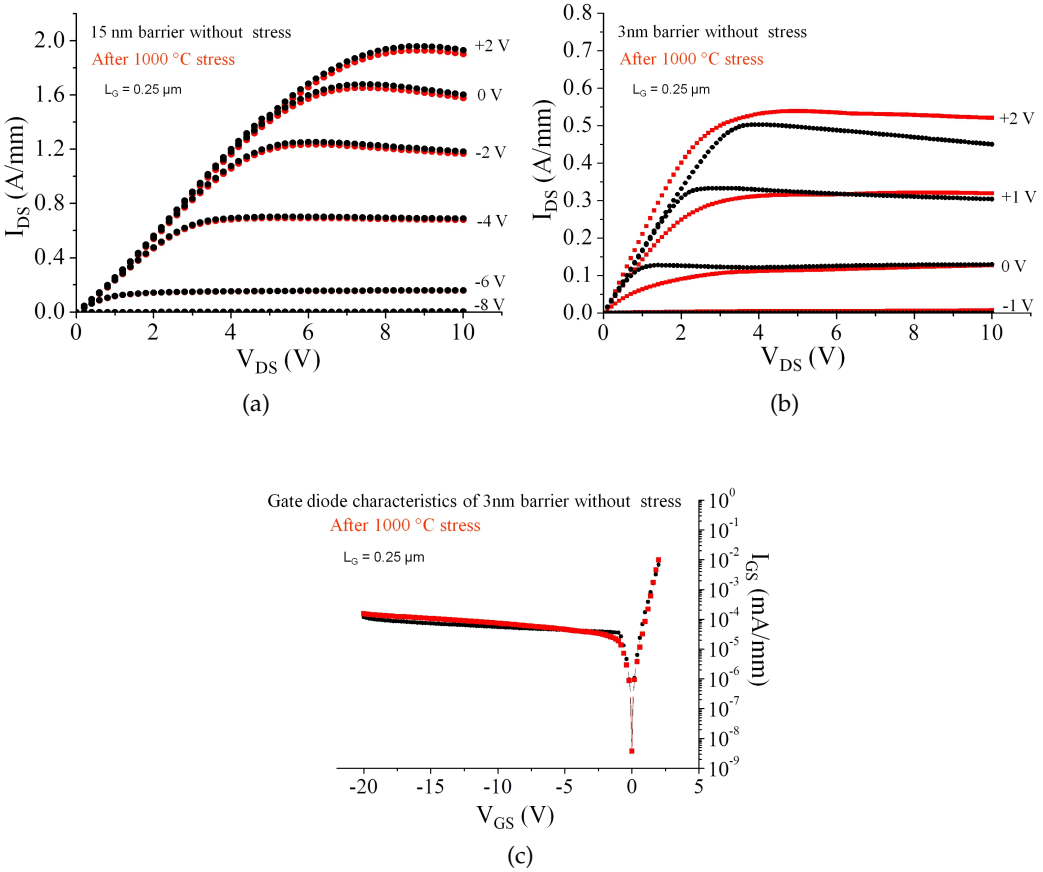
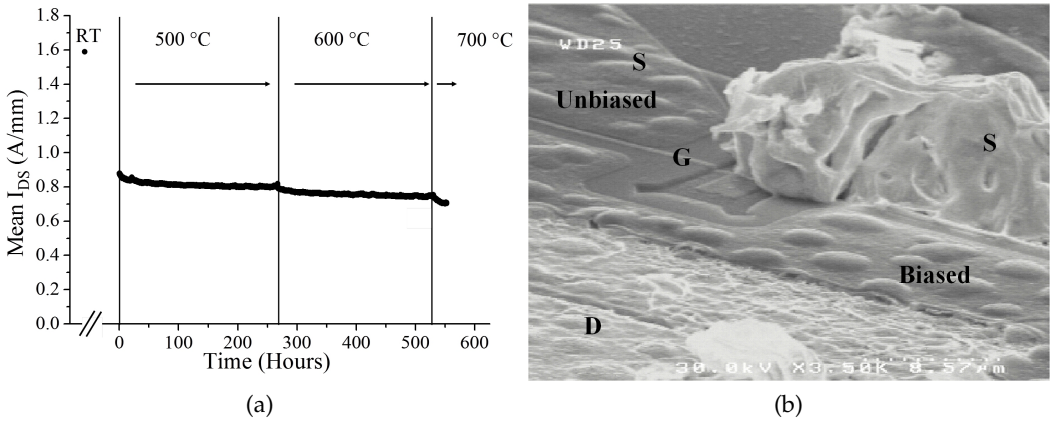


Figure 16: DC output characteristics of PCVD-Si_3N_4 passivated LM-InAlN/GaN HEMTs before and after 30 min. stress at 1000 °C in vacuum for (a) a 15 nm barrier (b) 3 nm barrier and (c) gate diode characteristics of the 3 nm barrier HEMT before and after the stress test.

source, drain and gate contacts. This is demonstrated for example in stability tests under 1 MHz large signal operation of the HEMTs with 10 nm barrier at temperatures from 500 °C in vacuum, in temperature steps of 100 °C increased after continuous operation for 250 hours and until failure. Measurement details can be found in [194, 231]. The HEMTs were processed with the standard routine, which means Ni/Au gate metallization was used for the gate, and has a 2-finger layout. Fig. 17a shows the mean HEMT current density recorded during the test period, for one finger. The tested HEMT operated for 250 hours at 500 °C followed by another 250 hours at 600 °C and failed suddenly after operating for 25 hours at 700 °C and did not show apparent degradation throughout the entire test period, as was shown by DC measurements performed periodically at the RT and the test temperature before each temperature change [228, 231]. The sudden failure of the device was due to metallization breakdown and melting that short circuited the device as can be seen in the SEM image in Fig. 17b. It is interesting to note that such degradation did not appear in the adjacent device (the unbiased second finger) which, along with other unbiased devices on the same tested sample, could be operated normally after cooling



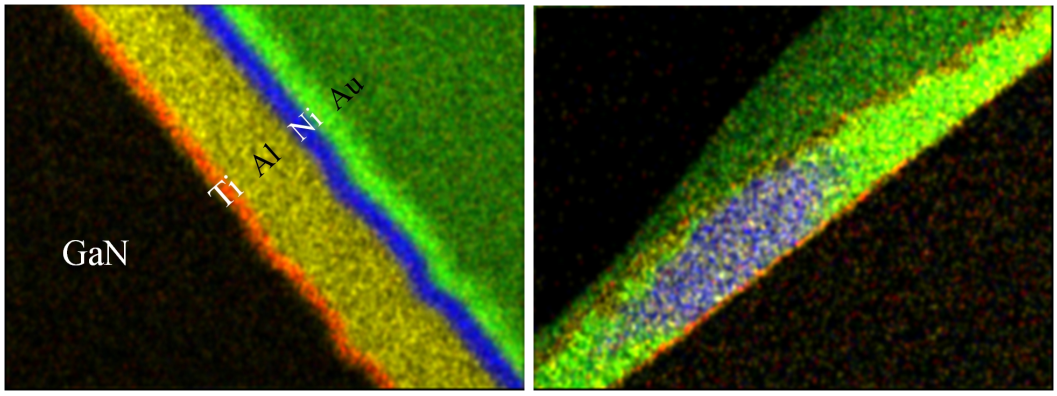
(a) (b)

Figure 17: (a) Long time operation test of 10 nm InAlN/GaN HEMT. The HEMT operated for 250 hours at 500 °C and 250 hours at 600 °C and 25 hours at 700 °C. (b) The sudden HEMT failure at 700 °C is due to metallization break and melting short circuiting the source and drain. The unbiased devices were not damaged and could be operated normally after the test.

down to RT. This supported the assumption that the main degradation mechanism of the HEMTs at high temperature is due to the metallization or the passivation but not the heterostructure itself. The presence of a ductile metal like Au is thus undesired and has to be replaced for high temperature operation, but in this case the gate conduction is compromised. HR-TEM images (see Fig. 18) showed that the non uniform alloying of Au starts as early as the ohmic contact annealing step. The same can be expected for the Ni/Au gate stack, if stored at high temperatures. A modification of the ohmic and gate contact for high temperature processing/operation was conducted in this work to enable the growth of NCD top layers and will be shown in section 4.1.3. These modifications also lead to an extended operation of the HEMT at even higher temperatures and up to 25 hours at 1000 °C. The details of these experiments will not be shown here but the results are reported in [194, 195, 228].

3.5 Thermal oxidation of InAlN

The exceptional high thermal stability of InAlN/GaN heterostructures enables to perform thermal oxidation at high temperature (above 800°C) resulting in extremely slow oxidation rates comparable to those seen in Silicon MOS-FET technology. The thermal oxidation process was conducted in an annealing oven in O_2 atmosphere at a temperature of 800 °C measured by a thermocouple mounted directly above the sample surface. The optimization of the oxidation temperature is described in detail in [68], where oxidation at temperatures between 600 °C and 900 °C was tested and a temperature of 800 °C was found to be the optimum. It should be mentioned that the optimum temperature differs with different oxidation furnaces, and should be optimized for each case. The experiments conducted here were all under the same conditions and were reproducible. In the FET, two oxidation



(a) (b)

Figure 18: TEM color-coded elemental maps (performed by E. Elektronenmikroskopie, Ulm) of the ohmic contact stack (a) before the annealing step and (b) after annealing at 850 °C for 30 seconds. Ti largely stays at the interface with the HEMT and Al disperses everywhere. Au and Ni on the other hand tend to segregate causing an excess of non alloyed metal which could later electromigrate at high temperatures specially for a ductile metal like Au.

schemes were used, namely the global oxidation scheme as proof of concept experiment, and the local oxidation scheme. In the global oxidation scheme the fabrication of the HEMTs proceeded as in section 3.3 up to the ohmic contact annealing step. Thereafter, oxidation was performed on the gateless HEMT, including the access region and the contact metals, followed by the gate lithography and passivation (see Fig. 19a). A modification was done on this fabrication routine, by processing the HEMTs up to the ohmics and then passivate them with PCVD Si_3N_4 and perform the oxidation in a localized area defined by a recess in the passivation (see Fig. 19b). This scheme will be denoted "local oxidation". A T-gate was aligned to the oxide recess opening followed by gate metallization to fabricate a MOSHEMT with thermally generated oxide (see Fig. 19c).

At first the nature of the formed oxide had been investigated by HR-TEM and High Angle Annular Dark Field (HAADF) STEM of the same TEM cross section in the Materialwissenschaftliche Elektronenmikroskopie Department in Ulm University, using a bare heterostructure oxidized for 10 minutes resulting in a 2 nm thick oxide layer as seen in the cross sections. Fig. 20 shows these cross sections, from which the identification of the heterostructure layers and the nature of the formed oxide are inferred. The HAADF-STEM analysis showed that the oxide is mostly Al_2O_3 with a high degree of crystallinity (see the HR-TEM insert in the image) which was the first indication of a high quality oxide. There is however an approximately 1 mono layer of Indium enriched material on top of the oxide, which on one hand shows that this oxidation temperature prefers the formation of Al_2O_3, and on the other hand can cause severe trapping effects at high operation frequencies if the Indium enriched layer acts as a fast metallic trap. After the oxidation, the surface was treated by HCl.

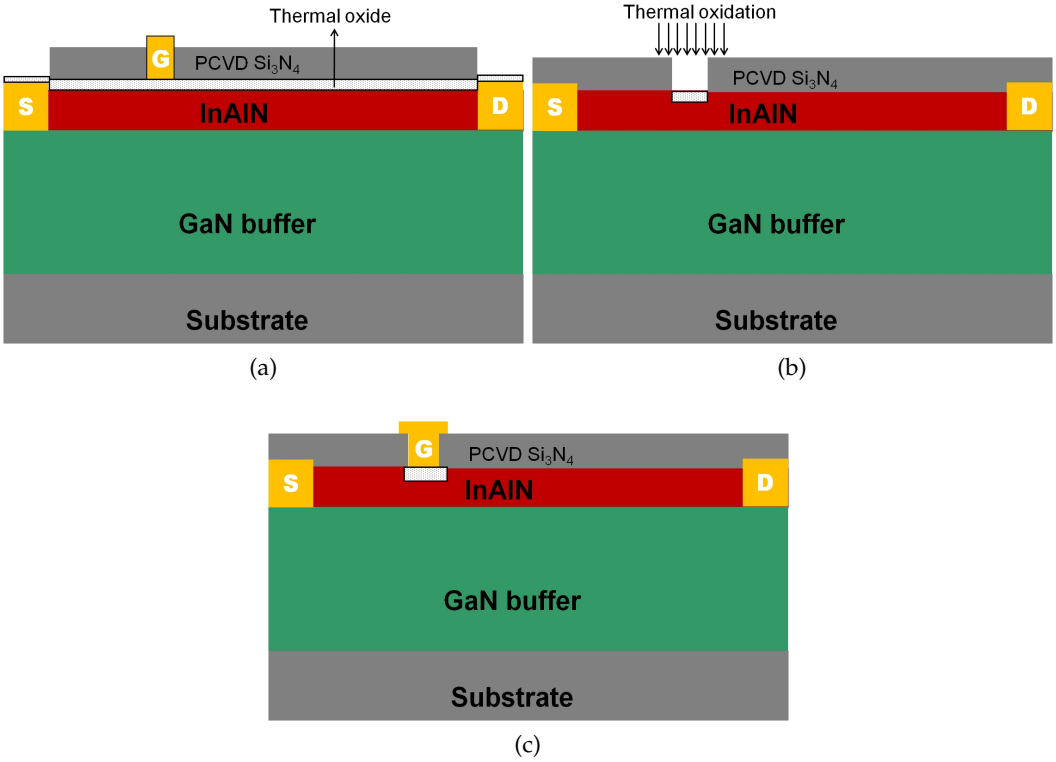


Figure 19: Cross section of (a) a MOSHEMT fabricated using a global oxidation scheme (b) local oxidation scheme used to characterize the effect of oxidation before gate deposition and (c) MOSHEMT with thermally generated oxide recess.

The quality of the thermally generated insulator was investigated firstly using structures fabricated using the global oxidation scheme. Oxidation was conducted for 2 and 5 minutes on separate pieces of the identical 10 nm barrier heterostructure, with identical device dimensions (0.25 µm x 50 µm). The as-grown LM-InAlN/GaN heterostructure had a mobility of 1000 $cm^2V^{-1}s^{-1}$ and an N_s of 1.6 x $10^{13}cm^{-2}$. A piece was left unoxidized for comparison and a set of DC measurement were conducted to evaluate the FET performance both before and after passivation. Fig. 21 shows the DC characteristics of the unpassivated devices. The effect of oxidation on the surface depletion is visible through the drop of the maximum current density with increased oxidation time. Likewise, an increase in the access resistances is also visible. The reduction of $I_{DS,max}$ can be explained by an increase in the surface potential and a decrease in the InAlN barrier thickness, as was shown in sections 3.3.1and 2.3.1 and can not be avoided using this global oxidation scheme.

A significant drop of the gate leakage is observed by increasing the oxidation time, up to 4 orders of magnitude after 5 minutes of thermal oxidation at 800°C (see Fig. 22a), which reveals a high insulator quality. This had a clearly visible effect on the 3-terminal breakdown defined at 1 mA/mm (see Fig. 22b). The 3-terminal breakdown of the HEMT was around V_{DS} = 80 volts, while the oxidized layers had no visible breakdown up to 100 volts. Biasing beyond this voltage has not been possible due to test equipment limitations.

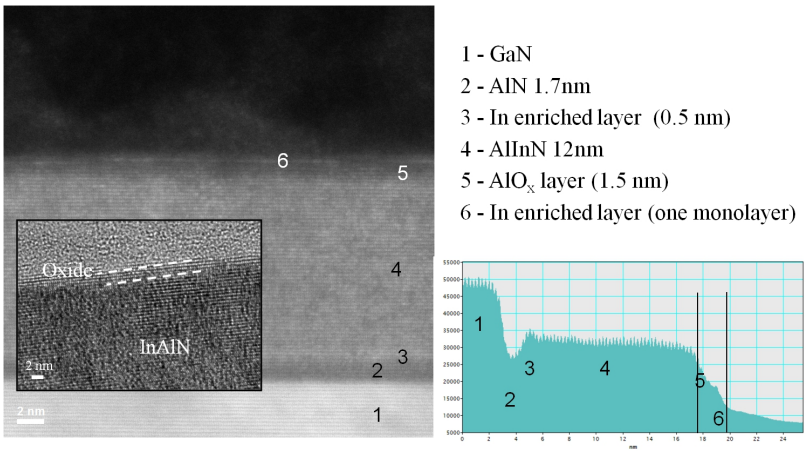


Figure 20: HAADF-STEM and HR-TEM cross sections (performed by E. Elektronenmikroskopie, Ulm) of initially a 15 nm barrier LM-InAlN/GaN oxidized thermally for 5 minutes at 800 °C. The HAADF-STEM elemental analysis (right insert) identifies the composition of the heterostructure after oxidation, and shows that the formed oxide is mostly Al_2O_3.

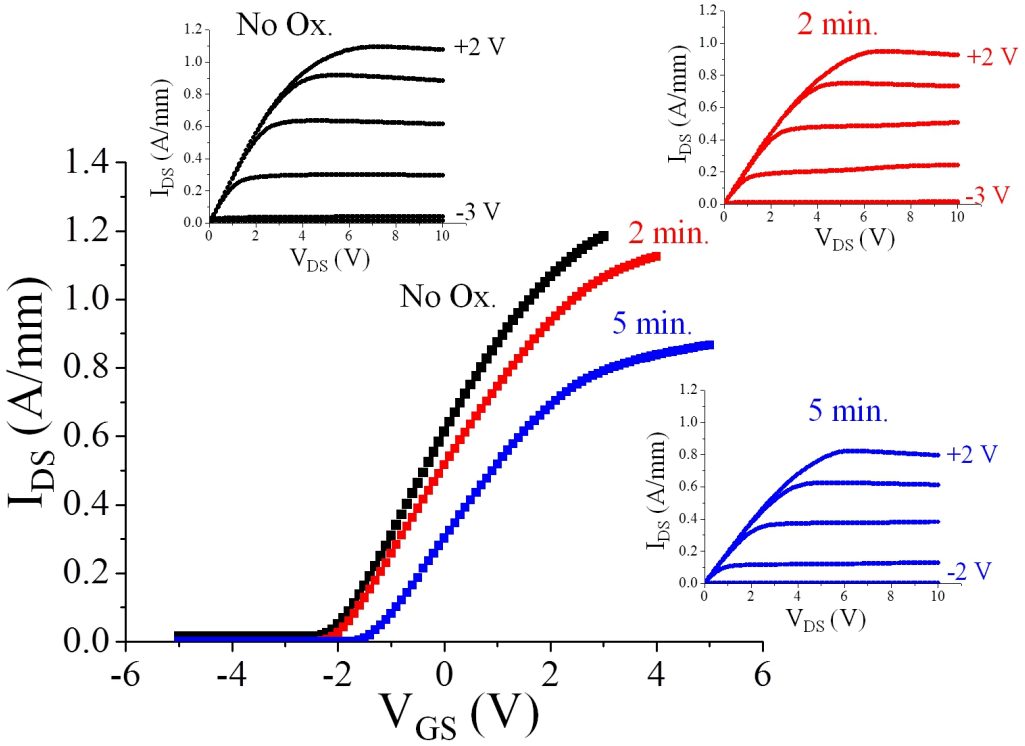


Figure 21: Transfer characteristics of 0.25 µm x 50 µm MOSHEMTs prepared by thermal oxidation compared to non oxidized HEMT. The insets show the output characteristics (V_g in 1 V steps) of the devices.

A shift in the turn-on voltage (see inset of Fig. 22a) of no more than 1 V for the longest oxidation time was also observed. The pinch-off voltage and transconductance have not been changed essentially by the short time oxidation treatment, which means that the barrier layer kept the same capacitance values and the same overall dielectric constant. The g_m of 300 mS/mm and the f_t of more 42 GHz of the passivated devices (the power performance of the passivated devices will be discussed in section 3.6) indicate also no degradation in the channel transport properties. However, the oxygen diffusion continues with time and the oxide layer thickness appears also to increase with time, leaving a thinner InAlN barrier layers. Therefore, for long oxidation times (5 minutes in this case) the sheet carrier density and thus the maximum drain current density are significantly reduced.

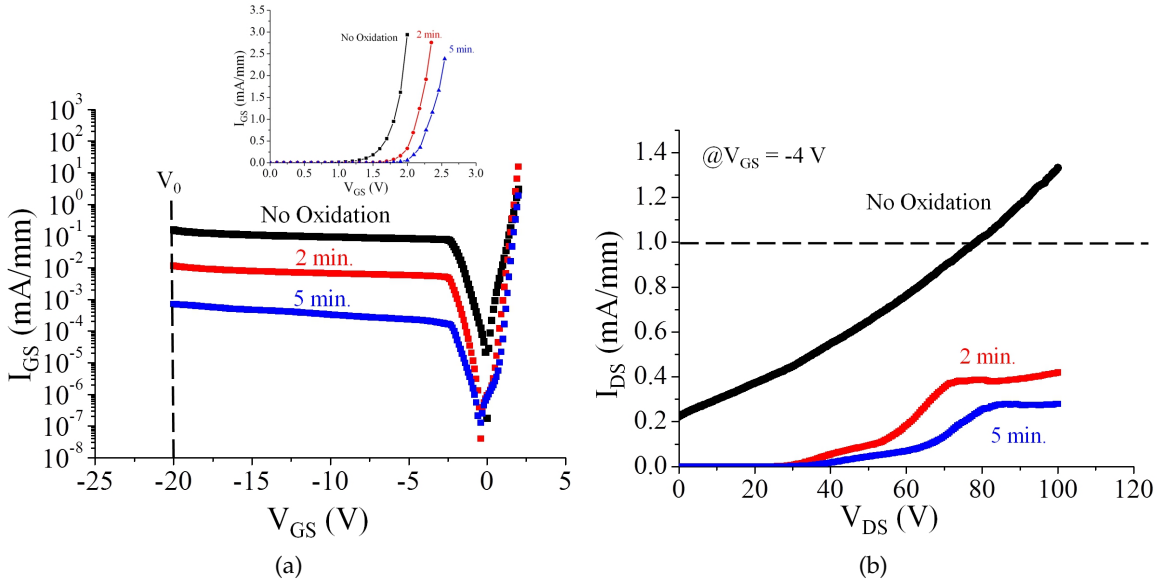


Figure 22: (a) Gate diode characteristics and (b) 3-terminal breakdown defined at 1 mA/mm of the HEMT and MOSHEMTs shown in Fig. 21. In addition to an increase in the gate turn on voltage, reduction in gate leakage current and increase in the 3-terminal breakdown of the devices were observed with increased oxidation time.

Using the diode characteristics shown in Fig. 22a enables the speculation of the oxidation mechanism to be diffusion limited. With such thin InAlN barriers it is expected that the dominant current leakage mechanism in a diode is the tunneling mechanism. As in the case of Silicon oxidation, insertion of a thin dielectric would reduce the leakage current (I_0) exponentially with the oxide thickness as described in equation 3.1 below [130, 232]:

$$I_0 \propto C_1 \frac{V_0}{d_{oxide}} \exp\left(-C_2 \frac{d_{oxide}}{V_0}\right) \tag{3.1}$$

where C_1 and C_2 are material related constants, d_{oxide} is the thickness of the oxide and V_0 is the voltage across the tunneling barrier. Moreover, the thickness of the oxide

for a diffusion limited oxidation mechanism is proportional to the square root of time as described in equation 3.2 below [233]:

$$d_{oxide} \approx \sqrt{Bt} \tag{3.2}$$

Where t is the oxidation time and B is the parabolic rate constant. From equations 3.1 and 3.2 the logarithm of the leakage current is linearly dependent on the square root of oxidation time. From Fig. 22a, recording the current values at a chosen gate source voltage (V_0), -20 V in this case, and plotting it with the square root of oxidation time reveals a linear dependence (see Fig. 23), which indicates a diffusion limited oxidation mechanism similar to the case of Silicon oxidation.

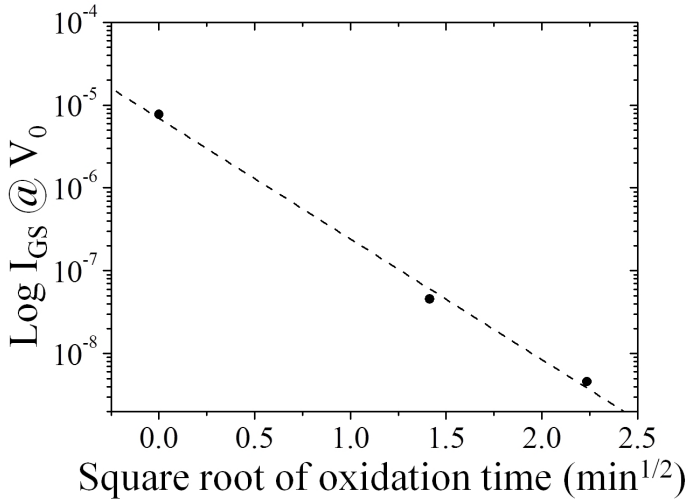


Figure 23: Dependence of leakage current (at V_g = -20 V) on the square root of oxidation time indicates an initially diffusion limited oxidation mechanism similar to the case of Silicon oxidation.

To correlate the effect of oxidation with the intrinsic properties of the heterostructure, namely N_s, the structure shown in Fig. 19b (local oxidation) was used, fabricated from a 10 nm barrier layer on GaN buffer on SiC substrate. The gateless device was oxidized for different times, while shielding the ohmic contact metals and the access region with a Si_3N_4 mask. The drop in the saturated current density (I_{DS}) relative to the saturated current density prior to oxidation (I_{DS0}) was recorded and TEM cross sections on similar unprocessed layers were used for calibration of the oxide thickness (see Fig. 24). The drop in I_{DS} is relatively slow up to 4 min. of oxidation (with an oxide thickness reaching 1.5 nm) and accelerates up to 8 min. of oxidation (with oxide thickness of 3 nm) where the heterostructure starts to suffer a structural degradation as seen in the TEM cross sections. The initial oxidation rate is about 0.4 nm/min.

Since the access regions are protected during oxidation we can assume a direct proportionality between I_{DS} and N_s for oxidation times up to 8 minutes before the heterostructure

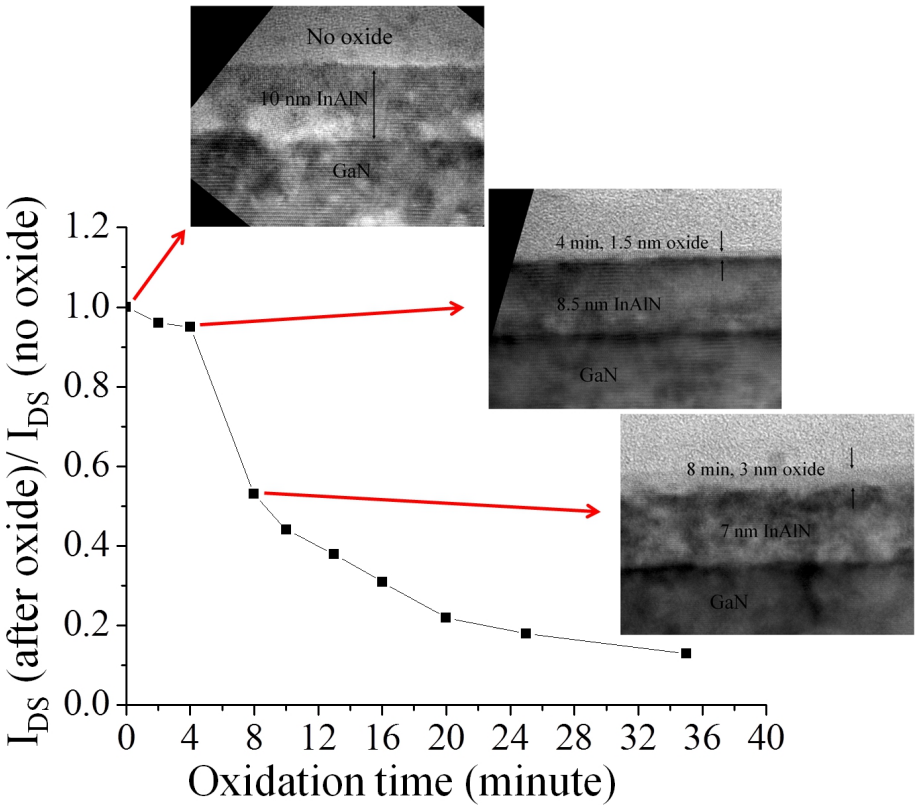


Figure 24: Relative change in I_{DS} with oxidation time. The insets show TEM cross sections (performed by MFA) of the layer before oxidation and after 4 and 8 minutes of oxidation.

starts to degrade (before oxidation N_s = 2.6 x 10^{13} cm^{-2} from Hall measurements) . By superimposing these data on the calculated N_s dependency on ϕ_s and barrier thickness presented earlier in Fig. 8, and taking into account the actual InAlN barrier thickness seen from the TEM cross sections, a quantitative description of the oxidation effect can be made. As shown in Fig. 25 for oxidation times up to 4 minutes, N_s drops with thickness but following a constant surface potential contour. At higher oxidation times the drop in $N_s$can not be explained by only a reduction in the barrier thickness, and to fit the tendency an increase in the surface potential is required. The TEM analysis showed that at 8 minutes of oxidation the concentration of Indium is higher near the InAlN/GaN interface, which could cause a polarization change and a surface potential shift. A verification of this process needs more detailed elemental analysis at smaller oxidation time steps. However, the above analysis shows that 4 minutes of oxidation is the optimum time since it is the limit at which the thickest possible oxide can be generated before degrading the heterostructure.

3.6 HEMT passivation and output power performance

To use the thermal oxidation process in subsequent NCD-coated power HEMT, the oxide should not introduce additional surface or bulk traps that causes current collapse and

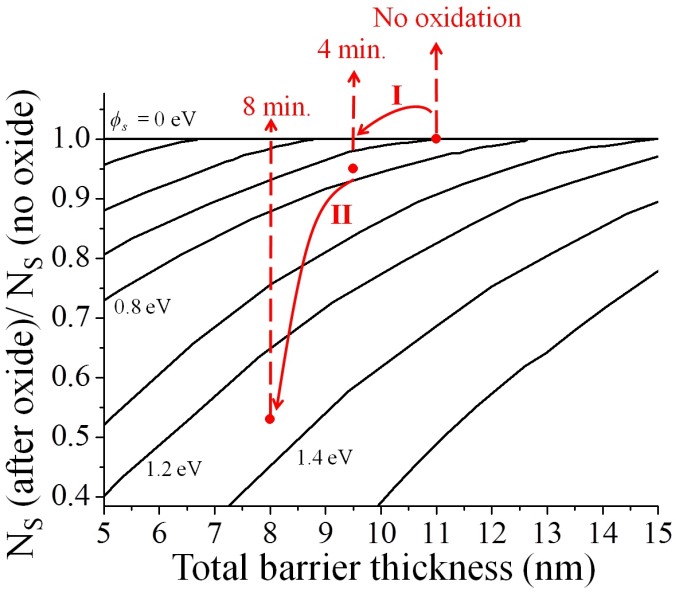


Figure 25: The effect of oxidation on carrier density using the data obtained from Fig.24 and 8 can be explained by (I) a constant surface potential for reduced barrier thicknesses at short oxidation times and (II) an increase with the surface potential and barrier thickness. After 8 min. of oxidation, ϕ_s increases to approximately 1.1 eV.

should be an efficient diffusion barrier to ensure gate stability in case of the high NCD deposition temperature, or if used in high temperature operation. This section and the next will provide evidence for the suitability of the thermal oxide for very efficient surface passivation and will also provide preliminary evidence for the high temperature stability. The final verification of the thermal stability will be shown under actual NCD growth conditions in the next chapter.

As discussed earlier in sections 2.5.1, the surface traps causing the current collapse should not only be minimized but also localized as far as possible from the surface and moved into the passivation. Thus the thermal oxidation alone is not expected to reduce the current collapse effects except when it is combined with a thicker passivation. The nature of the thermal oxide makes it an ideal platform for subsequent Al_2O_3 growth, which can serve as both passivation and gate dielectric but this material was not available to this work.

Typically, a traditionally used PCVD Si_3N_4 film was employed in this work, deposited using ammonia and Silane precursors, on the globally oxidized MOSHEMTs of Fig. 21, with a thickness of 200 nm. Fig. 26 shows the DC characteristics after passivation. Compared to the unpassivated devices, an unpinning of the surface due to the Si_3N_4 overlayer is visible through an increase of the maximum current density of about 25%, thus reducing (or eliminating) the already small surface potential of the unpassivated surface further. The passivation however caused a degradation of the gate diode characteristics compared to the unpassivated devices (see Fig. 27a) due to surface current leakage in the Si_3N_4 layer or at its interface, which is reflected on the 3-Terminal breakdown of the device (see

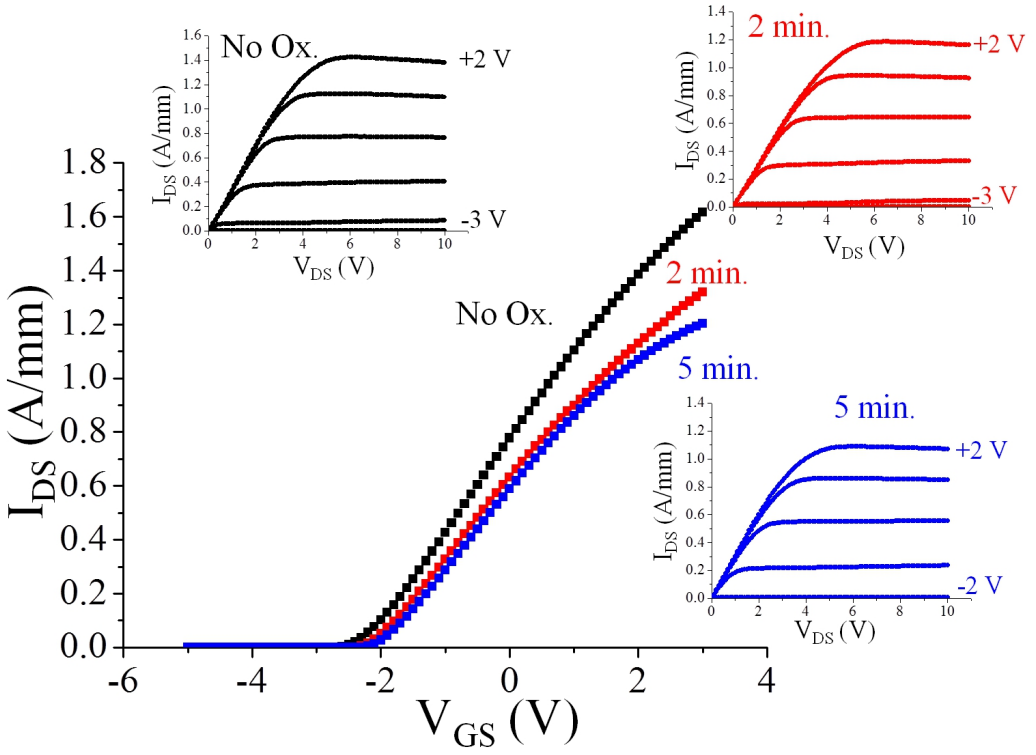


Figure 26: Transfer characteristics of 0.25 µm x 50 µm MOSHEMTs shown in Fig. 21 after passivation with 200 nm PCVD Si_3N_4. The insets show the output characteristics (V_g in 1 V steps) of the devices.

Fig. 27b) limiting it to 35 volts of source-drain bias (in the best cases). This effect may not be considered for the moment, but have to be dealt with in the case of NCD overgrowth as will be seen later.

Pulse and power measurements, performed by IEMN, were conducted on the MOSHEMTs with 2 min. oxidation. Fig. 28a shows the pulsed I-V measurements of the passivated devices with 500 ns pulse duration and 10 µs intervals. The thermal oxidation proved efficient in suppressing the gate lag (see Fig. 28a), which indicates a clean and widely trap free interface (confirming that the drain current increases due to a widely unpinned interface). Moreover, As compared to identical devices fabricated without thermal oxidation, the oxidation process did not have any apparent effect on the drain lag, indicating that the oxidation process did not introduce additional bulk trapping effects in the oxide layer. This is discussed in details in [209]. The load-pull power measurements, performed by IEMN, showed encouraging results in terms of the maximum output power achieved at 10 GHz and up to 30 V drain bias (see Fig. 28b). With 2 minutes oxidation, a maximum output power of 5.06 W/mm with a power added efficiency of 42% was obtained despite the added parasitics due to the oxidation of the ohmic contact metal. The s-parameter measurements yielded an f_t of 42 GHz and f_{max} of 61 GHz (compared to f_t of 37 GHz and

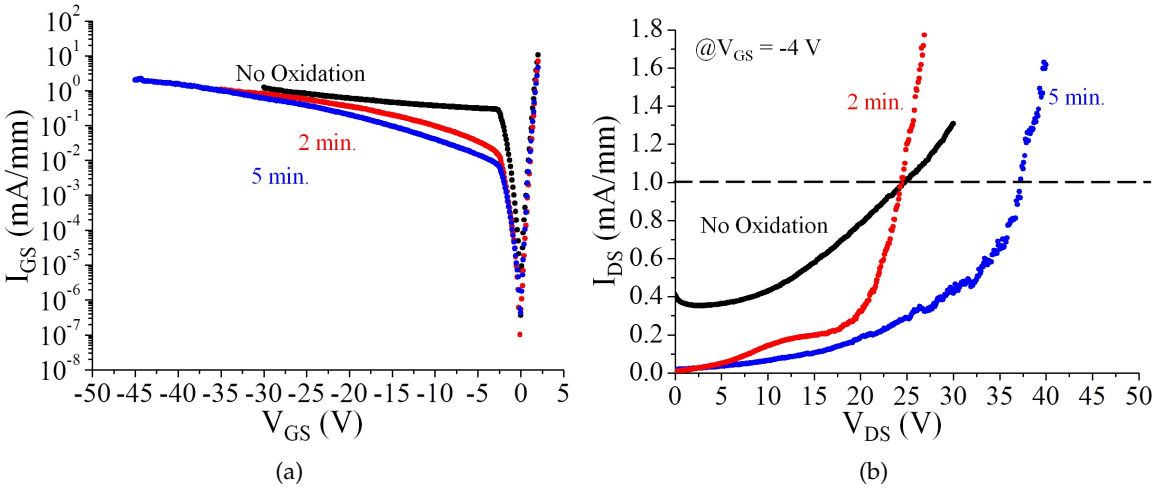


Figure 27: (a) Gate diode characteristics and (b) 3-terminal breakdown defined at 1 mA/mm of the devices shown in Fig. 22 after passivation with 200 nm PCVD Si_3N_4. The passivation caused a degradation of the gate diode characteristics compared to the unpassivated devices (see Fig. 27a) due to surface current leakage in the Si_3N_4 layer or at its interface, which reflected on the 3-Terminal breakdown of the device (see Fig. 27b) limiting it to 35 volts of source-drain bias in the best cases.

f_{max} of 60 GHz for HEMT device of the same gate length of 0.25 µm without oxidation), indicating no degradation of the small signal channel transport properties.

These results confirm the high efficiency of the thermal oxide + PCVD Si_3N_4passivation scheme. The thermal stability of the oxide was confirmed by TEM cross sections of the same HEMTs annealed at 800 °C for 30 minutes in vacuum. Despite the segregation and flow of Au in both the ohmic and gate contact no inter-diffusion into the oxide was seen, and the interface remained sharp and well defined (see Fig. 29).

3.6.1 *MOSHEMT with local oxide recess*

The realization of a MOSHEMT with the local oxidation scheme as in Fig. 19c, confined under the gate to the gate area only, avoids the oxidation of the entire surface and prevents the increase in the access resistances, employing the native oxide as an oxide recess. As discussed earlier, the high field region near the gate is the main area which should be controlled in power operation. Thus in this case the oxide recess was not confined only to the region under the gate, but also extended 50 nm on each side of the gate. MOSHEMTs (0.25 µm and 0.1 µm x 50 µm) were prepared by this method by oxidizing a 10 nm barrier layer for 4 minutes. The as-grown wafer had a mobility of 1290 $cm^2V^{-1}s^{-1}$ and an N_s of 1.9 x $10^{13}cm^{-2}$. Despite the higher number of fabrication steps required in this scheme compared to the global oxidation, its benefit can be seen by comparing the MOSHEMT current with the current of the passivated gateless HEMT before recessing and oxidizing, which represents the maximum current that could be driven in the HEMT. As can be

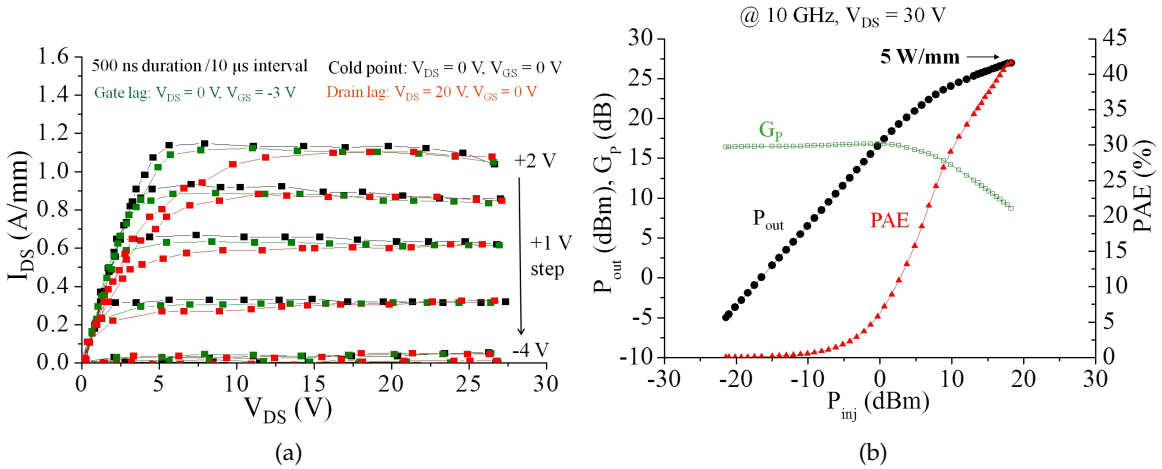


Figure 28: (a) Pulsed I_{DS}-V_{DS} characteristics (V_{GS} swept from -3 to 2 V by step of 2 V) at the quiescent bias points (V_{DS0} = 0 V, V_{GS0} = 0), (V_{DS0} = 0 V, V_{GS0} = -3) and (V_{DS0} = 20 V and 25 V, V_{GS0} = -3) of MOSHEMT with 2 min. oxidation and (b) the load-pull measurements of the MOSHEMT at V_{DS} = 30 V. The measurements were performed by IEMN.

seen in Fig. 30a, the full current density could be recovered with no change in the access resistance.

Pulse measurements with a 500 ns pulse duration (see Fig.30b) did not show any apparent gate or drain lag effects, thus the full channel density was accessible during power operation. Load-pull measurements conducted at 4 GHz (see Fig. 31a) yielded a saturated output power density of 11.6 W/mm at a drain bias of 20 V, the highest reported for LM-InAlN/GaN up to the time of this work.

This output power density is higher (almost 2 fold) than what can be expected theoretically from the approximation of equation 2.20, but follows the equation 2.21, with a 1/4 factor instead that of a 1/8, which is the case, if the microwave current waveform is half wave rectifier [66, 67]. This can be achieved by hard gate overdrive conditions, well into saturation and well into pinch-off as shown in the dynamic load lines (the output load line for various input power levels up to saturation as recorded as a function of time) superimposed on the DC cold-point pulse data in Fig. 31b. No current compression is observed in the output ellipse, and the full current density of 2.4 A/mm could be accessed. The ability to operate the device in such conditions indicates a high breakdown strength of the gate dielectric and hence, in essence, of the thin native oxide layer. Thus the thermally generated oxide is electrically stable. This is in addition to the high thermal stability shown earlier. The s-parameter measurements yielded an f_t of 44 GHz and f_{max} of 105 GHz for L_G = 0.25 µm. For L_G = 0.1 µm (Fig. 32) an f_t of 61 GHz and f_{max} of 112 GHz were achieved.

Due to the high electronic stability and most importantly the high thermal stability the thermal oxidation passivation scheme was adopted as a standard fabrication process. This was also applied to the HEMTs overgrown with NCD layers as will be discussed next.

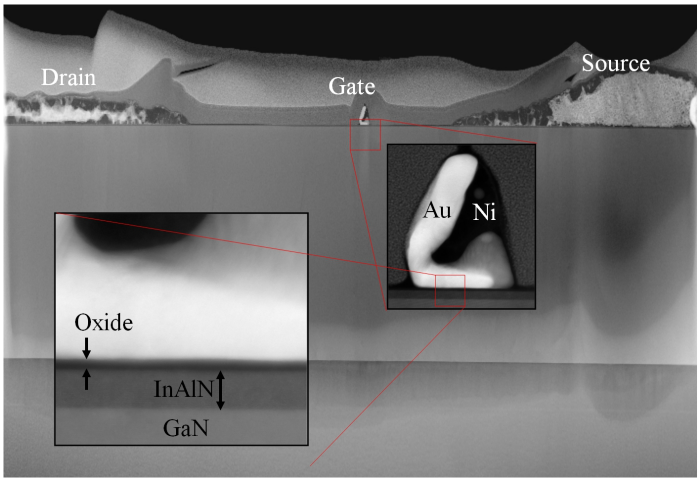


Figure 29: TEM cross section (performed by E. Elektronenmikroskopie, Ulm) of the MOSHEMT with 2 min. oxidation after thermal stress at 800 °C for 30 min. Despite the segregation and flow of Au in both the ohmic and gate contact no inter-diffusion into the oxide was seen, and the interface remained sharp and well defined.

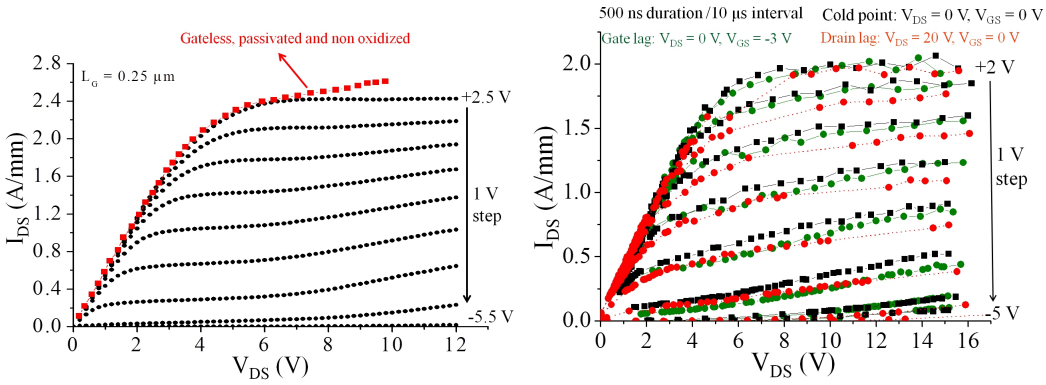


Figure 30: (a) DC output characteristics of 0.25 µm x 50 µm MOSHEMT with thermally generated oxide recess. The maximum current density of 2.4 A/mm in the layer could be accessed after oxidation. (b) Pulsed I_{DS}-V_{DS} characteristics (performed by IEMN) of the device indicated a largely lag free device.

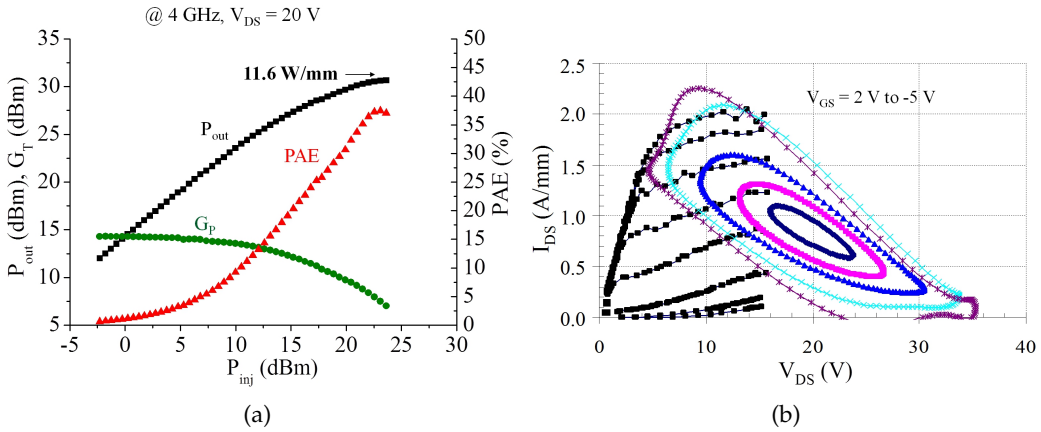


Figure 31: (a) Load-pull measurements of the oxide recessed MOSHEMT at V_{DS} = 20 V and (b) Measured RF load lines for a class-A bias point superimposed on pulsed DC characteristics (cold point) of the device. No current compression is observed in the output ellipse, and the full current density of 2.4 A/mm could be accessed. The measurements were performed by IEMN.

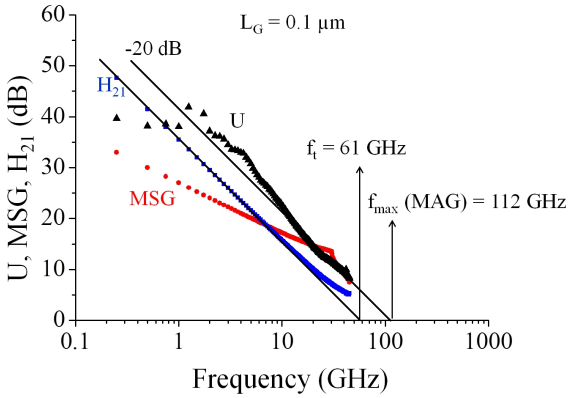


Figure 32: s-parameter measurements of 0.1 µm x 50 µm MOSHEMT with oxide recess.

However, the PCVD Si_3N_4 layer needed a modification in the deposition precursors to cope with the thermally demanding process of NCD deposition.

4

COMBINING DIAMOND AND GaN: ADVANTAGES AND CHALLENGES

This chapter will discuss the technological steps needed to combine GaN HEMT devices with Diamond overlayer, largely directed toward heat spreading. Thermal aspects are not discussed, since the heat sink technology had not been part of this study. However, the efficiency of the methods applied here can be evaluated initially by thermal simulations and an investigation into the thermal properties of the used Diamond films.

At high output power densities, like the ones demonstrated in the previous section, device self heating is the main limiting factor for stable operation of the device, as discussed in section 2.5.2. Heat extraction is mainly through the substrate, and is therefore dependent on the substrate type. But heat can be also extracted from the top. Thus their are three possible combinations for heat management. The first approach would be using either a SiC, Sapphire, Si, single crystalline Diamond or polycrystalline Diamond (in the form of Nanocrystalline Diamond or NCD) as substrates, with an attached heat sink for bottom heat extraction. The second approach would be combining the same set of substrates with nanocrystalline Diamond (NCD) on top but the heat sink still on bottom (thus it is still a bottom heat dissipation approach). The third approach would be the same as the second approach but with attaching the heat sink to the NCD top layer, instead of attaching it to the substrate, thus extracting the heat from the top of the device. The later approach puts the heat sink in close proximity to the channel, providing a shorter thermal path for the heat to dissipate and avoiding thermal barriers like the GaN buffer layer, the thermal conductivity of which is affected by its quality [234, 235]. A first insight on the efficiency of top heat heat extraction using Diamond was given by P. Schmidt and M. Neuburger et. al. in [236]using thermal simulations. However, due to its relevance to this work 2D thermal simulations are also performed to evaluate the efficiency of both approaches (bottom and top heat spreading), and to estimate the maximum HEMT temperature as a function of the power loss in the device, in view of the data obtained and results achieved in the course of this work.

The thermal simulations were performed using Finite Element Method (FEM) software (COMSOL) with a 2D model. The simulated structure is based on the building blocks of a HEMT as shown in Fig. 33, with GaN buffer thickness of 2 µm, 10 nm thick InAlN barrier, Cu as metallization for ohmics and gate, and 50 nm Si_3N_4 as passivation. The source-gate distance is 0.75 µm and the gate-drain distance is 2 µm. The simulator assumes a 1 µm width of the device for purposes of unit normalization.

Different substrates were used for bottom heat spreading, namely, Sapphire, SiC, Si, nanocrystalline and single-crystalline Diamond. The thermal properties of the used materials used in this simulation are listed in table 4. The 10 nm InAlN barrier is ignored since it does not significantly influence the heat spreading compared to the buffer or the passivation. The device self heating is simulated by introducing a 1-dimensional heating

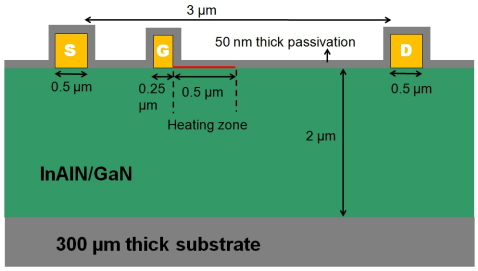


Figure 33: GaN HEMT device geometry used in the 2D FEM simulation.

zone, representing the hot spot region in the channel between gate and drain (0.5 µm long) adjacent to the gate metal contact stripe, as was demonstrated also for AlGaN/GaN HEMTs [189, 237]. This is done by introducing an inward heat flux (in units of W/m^2) across the heating zone area shown in Fig. 33. The heat flux is calculated by dividing an assumed RF power loss, ranging between 1 and 20 W/mm, by the heat zone area. Thus, the simulations do not calculate the device self heating as a function of the output power but rather introduces a pre-calculated amount of power loss, which is expected to be generated during device operation. Heat dissipation is then simulated using the aforementioned configurations of a heat spreader on bottom or on top, taking into account the thermal boundary resistances (TBR) at the interfaces. Adiabatic boundary conditions were used at all interfaces and surfaces except for the heat sink. At the bottom (when the simulated heat sink is placed at the substrate side), or at the top (when the simulated heat sink is placed above the top heat spreading layer) an isothermal boundary condition is assumed with T=25 °C (i.e. the heat sink is considered an ideal heat sink at a constant temperature of 25 °C obtained by forced cooling). To simulate the thermal resistances at the interfaces at the bottom and top (between substrate and the GaN buffer and between device passivation and the NCD top layer respectively) a thermal resistive layer (thickness 100 nm, k_{TBR}=1 W/mK) is included in the model. Solving the heat diffusion equation, the simulator will calculate the peak channel temperature in the HEMT as a function of the power loss (dissipated heat flux) for each different configuration.

Firstly, the heat dissipation effect of the substrate with an attached heat sink on the bottom is simulated. Here the device is passivated with 50 nm Si_3N_4 and is without an NCD top layer. Fig. 34 shows the maximum HEMT temperature as a function of the device power loss. As can be seen in Fig. 34, the device maximum temperature is greatly influenced by the type of substrate. A higher thermal conductivity of the substrate yields in a higher thermal dissipation efficiency.

Of course, the most efficient configuration would be, using a single crystalline Diamond substrate. But despite its very high thermal conductivity (2000 W/mK at R.T.) the device temperature can still reach high values. For example the device temperature will reach 100 °C at a power loss of approximately 5 W/mm using single crystalline Diamond and will reach 100 °C at 3 W/mm when using SiC (the most commonly used substrate in this work). The bottle neck for heat extraction from the bottom is the GaN buffer (ranging from 1 µm to 3 µm in thickness) and its thermal interface resistance with the substrate. A slight

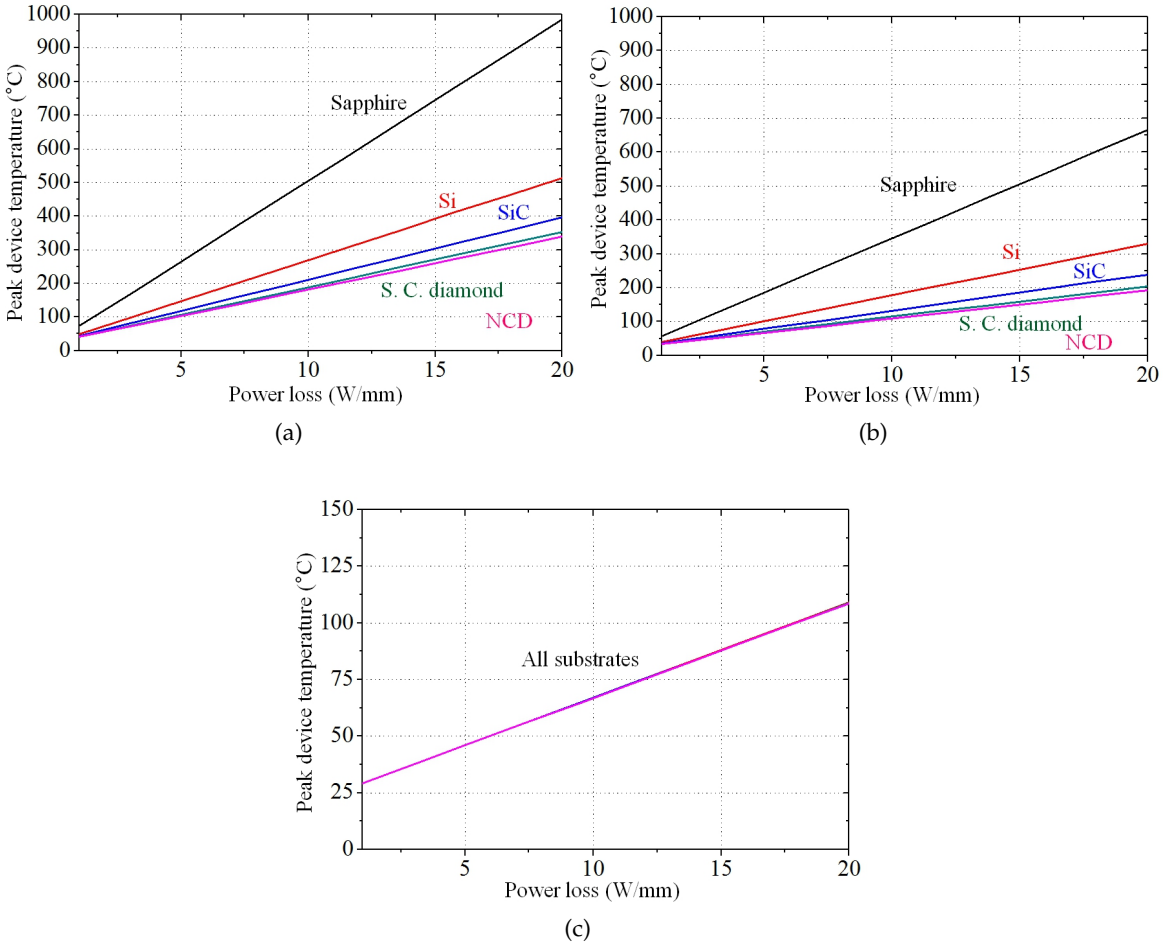


Figure 34: HEMT maximum channel temperature as a function of power loss for different heat dissipation configurations. (a) For bottom heat spreader and heat sink, the device temperature depends on the substrate type. (b) For bottom heat spreader and heat sink but with a 2 µm NCD layer on top, a slight reduction in the maximum temperature of the device can be achieved. (c) Using a 2 µm NCD heat spreading layer with an attached heat sink on top, the device temperature is significantly reduced and is independent of the substrate type.

Material	Thickness (µm)	κ(W/mK)
GaN	2	130
Cu metallization	0.2	340
Si_3N_4 passivation	0.05	15
Sapphire	3000	40
Si	3000	150
SiC	3000	340
Nanocrystalline Diamond	3000	500
Single crystalline Diamond	3000	2000

Table 4: Material parameters used in the thermal simulations.

reduction in the maximum temperature of the device can be achieved by adding a top NCD heat spreader (without heat sink). Fig. 34b shows the effect of adding a 2 µm thick NCD layer on top of the device with a thermal conductivity of 500 W/mK (only 1/4 of the ideal Diamond thermal conductivity) but without a heat sink. The heat sink is still attached to the bottom of the substrate only and the heat dissipation is again still strongly dependent on the type of substrate. The NCD layer on top of the device distributes the heat across the surface of the device, which is then however hardly removed (see Fig. 35). When using a SiC substrate a maximum device temperature of 100 °C is reached at a power loss of approximately 7 W/mm. The alternative is to deposit an NCD heat spreader and ideal heat sink on the top of the device structure. Fig. 34c shows such a case with a 2 µm thick NCD top layer and attached heat sink. Similar to a flip-chip configuration, no heat sink at the bottom was used. In this configuration the device temperature is only marginally influenced by the GaN buffer and is essentially independent of the substrate type used. To appreciate the difference between the three heat dissipation methods the temperature distribution in the HEMT for the different configurations is shown in Fig. 35.

The key factor for efficient heat extraction in the last configuration is the close proximity of the heat source to the ideal heat sink. Despite using a heat spreader containing only 1/4 of the ideal Diamond thermal conductivity, the maximum channel temperature will reach the 100 °C temperature now at a power loss of 18 W/mm. Thus, using NCD on top of the HEMT structure with an attached ideal heat sink presents the most efficient method of heat dissipation but the Diamond films have to be grown on top of the GaN HEMT without inducing damage.

Epitaxial combination of Diamond and GaN, whether on top or on bottom, is however not straight forward, and each approach has its own limitations as will be discussed next. Both of these approaches (Diamond on bottom and Diamond on top) were demonstrated successfully in this work. The very high thermal stability of the LM-InAlN is highly valued for reliable device operation but also provides an opportunity to coat the HEMT NCD films for heat extraction from top. This requires first a verification of the heterostructure stability under actual NCD growth conditions (section 4.1.2) and certain modifications

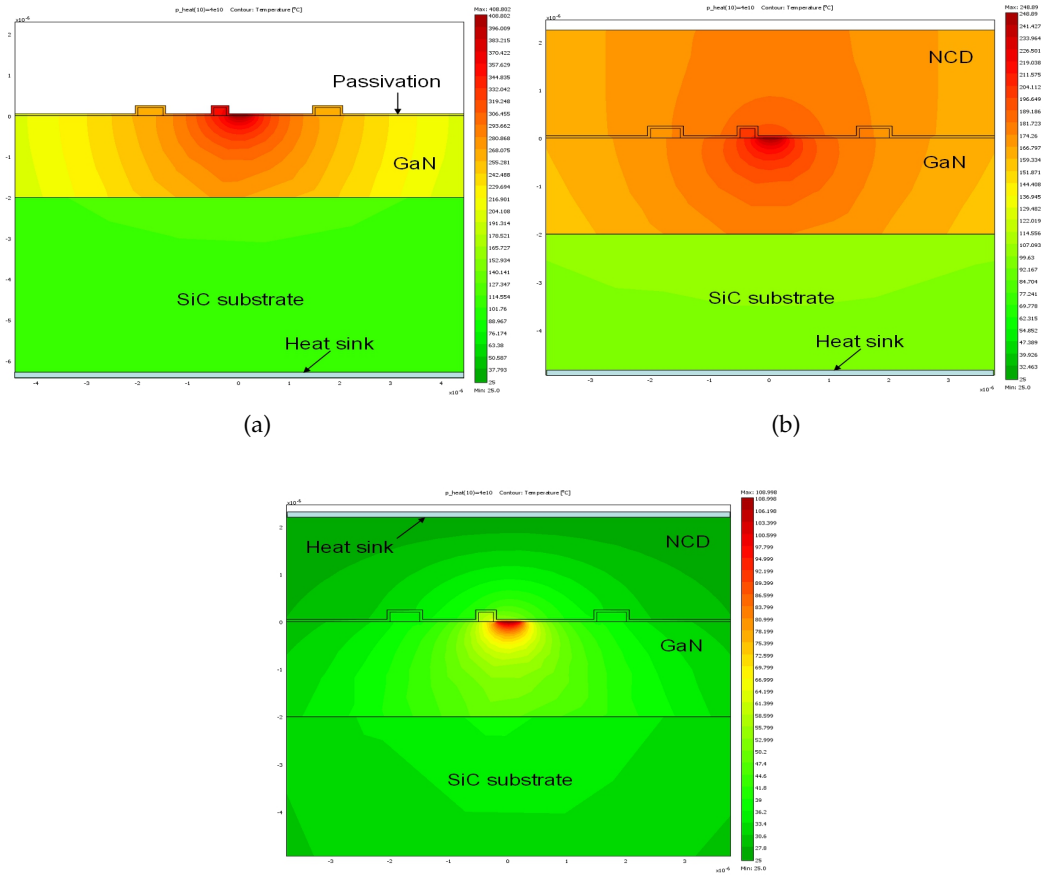


Figure 35: Temperature distribution in the simulated HEMT structure on SiC substrate using different heat spreading configurations at a power loss of 20 W/mm (a) with heat spreader and heat sink on bottom (b) with heat spreader and heat sink on bottom but with top NCD layer (c) with top NCD heat spreader with an attached heat sink.

on the HEMT processing routine as will be discussed in section 4.1.3. The results of this technology are presented in sections 4.2.1 and 4.2.2 but can be used in applications other than heat dissipation, like, for example, electrochemical applications combining the inertness of Diamond and the high transconductance of the InAlN/GaN in a monolithically integrated ISFET. The application of Diamond for chemical sensing and the InAlN/GaN - Diamond ISFET will not be discussed here but can be found in [40, 41, 42]. This approach could be combined in the future with GaN HEMT grown on single crystalline Diamond substrates, which through a joint effort with the GaN material growers, was demonstrated for the first time in this work (see section 4.3).

4.1 Nanocrystalline Diamond on GaN

This section will briefly present the main challenge of growing NCD films on GaN and the basic properties of the grown films. This required a common optimization of the NCD films (carried on by the Diamond growth group M. Dipalo and S. Rossi), and the GaN technology. Discussed here are the NCD optimization results relevant to HEMT overgrowth. Details about the growth mechanism and conditions of the NCD films used in this work are presented in the work of M. Dipalo [238].

In general, Diamond will only nucleate on carbide forming materials like many refractory metals or Si and will not outgrow in the single crystal phase even on cubic substrates (except for growth on Iridium [239]). The attempt to grow oriented polycrystalline Diamond on GaN resulted in a non closed film with islands few micrometers wide [240], which is not suitable for heat extraction. An alternative is to grow randomly oriented polycrystalline Diamond, nucleated or seeded on InAlN or GaN.

The most common polycrystalline Diamond growth processes are based on methane providing the carbon atoms for incorporation into the Diamond lattice and H-radicals as catalytic element in the reaction cycle. The gases are dissociated and radicals are formed by the energy provided either by a Microwave Plasma (Microwave-Plasma CVD Diamond growth) or thermally by a hot source like a heated wire (Hot-Filament Diamond growth or HF-CVD). Since carbon may be incorporated as SP^3 continuing the Diamond phase or as SP^2, forming graphitic inclusions a high content of H-radicals is needed to etch the graphitic phase continuously.

An HF-CVD growth chamber was used to grow the NCD films in this work. In a HF-CVD reaction chamber the substrate holder is facing a set of filaments (wires), which are needed to split the precursor molecules into radicals. This is mainly the splitting of H^2 into $2H^*$ above 1600 °C. As mentioned before, to achieve hetero epitaxial Diamond growth on foreign substrates nuclei are needed. These nuclei can be created in-situ or deposited by seeding. In the case of seeding they are deposited as nanoparticles from a slurry. Care has to be taken to obtain a widely monolayer thin coverage avoiding agglomerates. Furthermore, for good adhesion and good thermal contact covalent bonds need to be formed with the substrate, in general requiring alloying. The other option is the formation of Diamond nuclei within carbide clusters and their outgrowth. To create cubic carbon clusters within a carbide matrix, C-atoms need to be implanted. Thus, such a process needs ionization and a high electrical field. Such a process is Bias Enhanced Nucleation (BEN) developed for the case of a Si substrate. Again, this is a hydrogen/methane process and carbon ions are implanted into a SiC cluster, which has formed on the Si substrate surface in the H^2/CH^4 gas environment. The implantation of further carbon ions leads to increased stress and pressure within the crystalline SiC cluster forming an encapsulated cubic C-cluster. At high temperature the SiC cluster will be etched in the presence of the high H-radical density. Thus, the cubic C-cluster may penetrate the surface, serving as nucleus for further outgrowth.

Two main criteria should be met for an efficient heat extraction using a top Diamond layer. Firstly, the Diamond layer should have the highest possible thermal conductivity. Since

the grain boundaries are the main limiter, vertically oriented large grains are preferred, resulting from a 2D growth mode, where the thermal conductivity is anisotropic and higher in the vertical direction. A 3D growth mode would yield an isotropic thermal conductivity but generally has lower thermal conductivity [241]. The grain boundaries should also contain a limited content of graphitic phases and α-carbon clusters. In addition, the thermal conductivity of both modes will depend also on the film thickness Fig. 36a. These properties are typically obtained at growth temperatures above 650 °C in CH_4 highly diluted in H_2 with growth rates below 1 µm/hour and thus long growth times.

The second criteria for efficient heat extraction is a low thermal resistive interface between the NCD and the GaN passivation. The BEN method described above meets this criteria due to the covalent bonding of the NCD with the nuclei originating from the substrate (the passivation in this case), and thus provides strong phonon coupling across the interface and mechanical stability. In addition, voids between the NCD film and the interface should be avoided, which requires a high nucleation density in the range of 10^{10} cm^{-2}, which is typically obtained at nucleation temperature above 700 °C.

Although the top heat extraction approach using NCD films was proposed as early as 1992 [242], only few successful attempts have been reported to overgrow GaN HEMT structures with NCD, the main reason being the thermal/chemical stability of the heterostructure in the harsh growth environment, along with the high thermal stress on the HEMT components. Under these conditions GaN may even decompose into metallic Ga and N_2 in the presence of a high H-radical density [146]. The only reported attempt so far has therefore been based on rather low temperature growth below 500 °C, in order not to degrade the GaN and AlGaN materials and damage their surfaces [243]. Additionally, the attempts reported on the thermal management of GaN heterostructures using Diamond films (either from top or bottom) were mostly based on technologies like wafer bonding to the rear of the chip [37, 38, 244, 245], but with no clear thermal advantage of the Diamond layer yet [246]. This is probably due to the added thermal boundary resistance of the bonding material.

4.1.1 *NCD growth conditions and film properties*

The NCD overgrowth on LM-InAlN/GaN HEMTs used in this work was performed using HF-CVD growth with BEN nucleation (nanoparticles seeding was also tested in a specific case, as will be seen later). The nucleation and growth conditions were optimized considering the aspects for efficient heat dissipation as summarized below, but with the lowest nucleation temperatures possible:

- The NCD films to be grown should have the highest possible thermal conductivity:

This was achieved by tuning the growth parameters for vertical 2D growth mode, mainly by growing the NCD films at a minimum temperature of 700 °C with a growth rate of approximately 0.1 µm/hour with an average grain size of 100 nm (for films thicker than 650 nm). The content of the films grown under these conditions was investigated by Raman spectroscopy (using UV light) as shown in Fig. 36b. The spectrum confirms that the peak

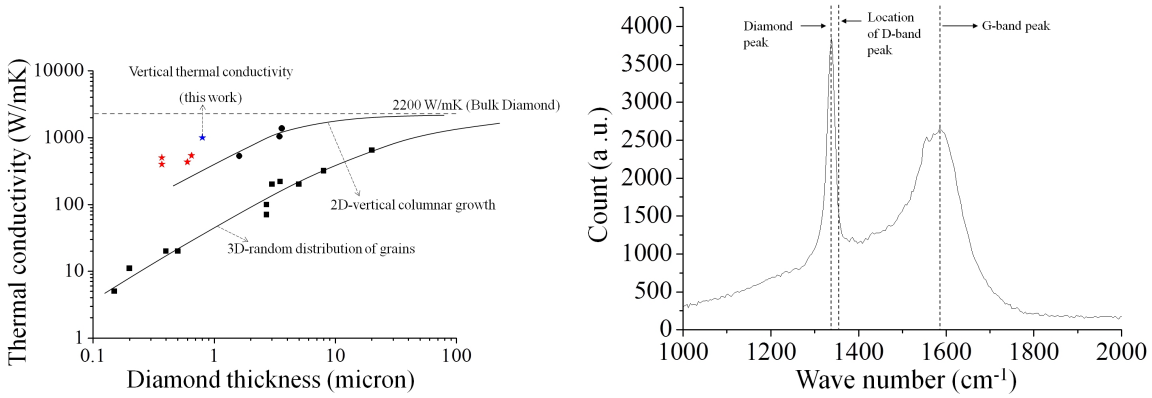
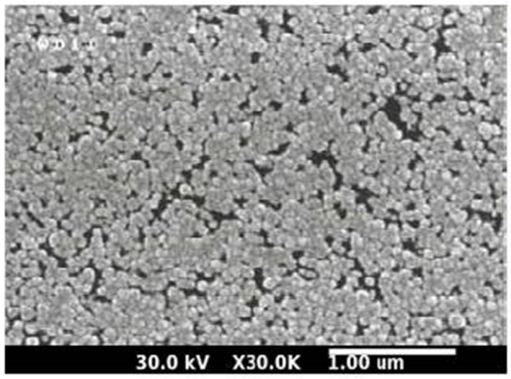


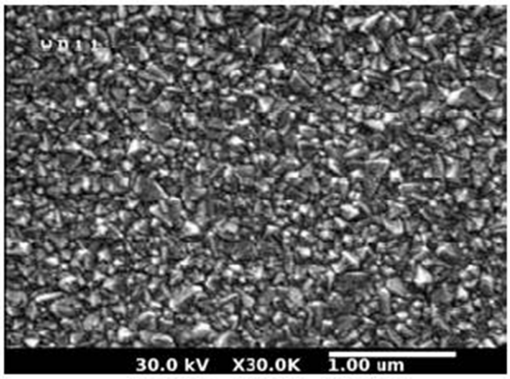
Figure 36: (a) Collected thermal conductivity data of NCD films as function of the film thickness and structure([3, 4, 5, 6, 7, 8]). Also shown in the figure the thermal conductivities (measured by GLG) of the films grown in this work (denoted by stars) optimized for vertical thermal conductivity. (b) Raman spectroscopy of the grown films, showing the dominant Diamond content in the film.

at 1332 cm^{-1}, characteristic of Diamond sp^3 bond, is predominant. The G-band peak at 1580 cm^{-1}, characteristic of graphite phases in the grain boundaries, is much lower in intensity. Moreover, no D-band peak at 1355 cm^{-1} is seen. The D-band is in fact shown to be related to small size graphite clusters [247] which in turn are found to be present in NCD with small grain size [248], the higher intensity of the D-band peak is therefore an indication of higher content of graphitic phases in the grain boundaries of the NCD layer. The absence of the D-band peak and the dominant Diamond peak are therefore a clear indication that Diamond is the main configuration of carbon in the layer. The vertical growth mode and the minimum graphitic content in the films is reflected on its thermal conductivity. Fig. 36a shows the thermal conductivity of the obtained films as compared to reported values. As can be seen in the figure, the grown films follow the 2D-growth mode with thermal conductivities approaching the best reported values. These data were obtained using a combination of SThM measurements and thermal simulations not taking into account the anisotropy in the thermal conductivity and thus limited by the lower lateral component of the thermal conductivity. Measurements on dedicated structures indicated a vertical thermal conductivity of 1000 W/mK (for films 800 nm thick) which is sufficient for efficient heat extraction according to the thermal simulations presented earlier. It should be mentioned that the optimization of both the thermal conductivity and the measurement method is still a work under progress.

- The interlayer and nucleation or seed layers used in the NCD overgrowth process should create the lowest thermal interface resistance possible with a high nucleation density to reach a grain configuration of high vertical and lateral thermal conductivity within a minimum of thickness.



(a)



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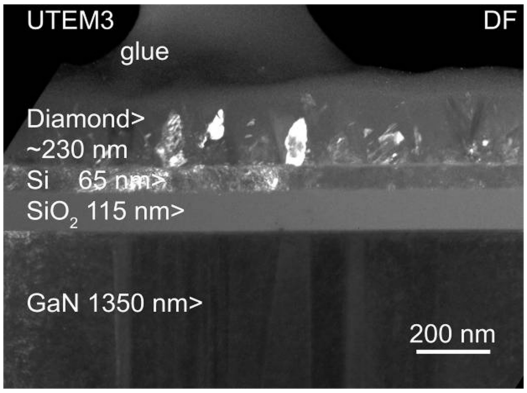

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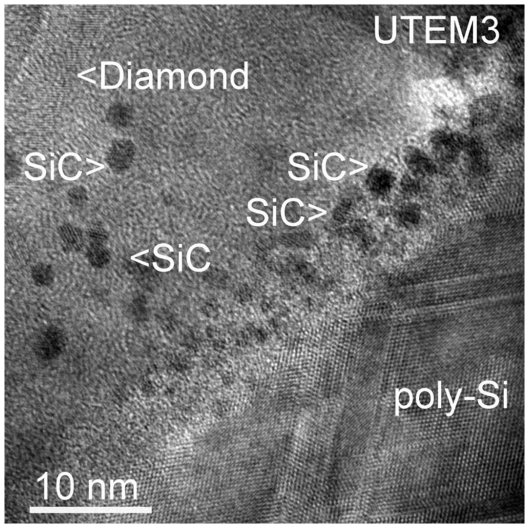


(d)

Figure 37: SEM images of (a) BEN nucleation and (b) NCD overgrowth on LM-InAlN/GaN. (c) TEM cross sections (performed by MFA) showed a continuous void free NCD layer nucleated from SiC clusters (d) propagating from the nucleation layer.

This is achieved by BEN, performed at a minimum temperatures of 700 °C (maximum nucleation temperature used in this work was 800 °C), using an insulating Si interlayer deposited by PCVD on top of the device passivation. The minimum thickness of this layer was 50 nm to allow a nucleation density larger than $10^{10}cm^{-2}$ [249]. Initial experiments used SiO_2 as device passivation, and the Si interlayer thickness varied between 50 nm and 100 nm. The replacement of this passivation by Si_3N_4 will be discussed later. Figures 37a and 37b show an SEM image of a nucleated surface and the subsequent NCD grown film on LM-InAlN/GaN. The high nucleation density allowed the growth of the NCD film with the properties described above. TEM cross sections (see Fig. 37c) showed a closed layer with no voids, and the SiC clusters, which forms during the BEN process, extending up to 10 nm into the Si interlayer (see Fig. 37d). Thus, the interface between NCD and the top of the Si nucleation layer is continuous and covalently bonded.

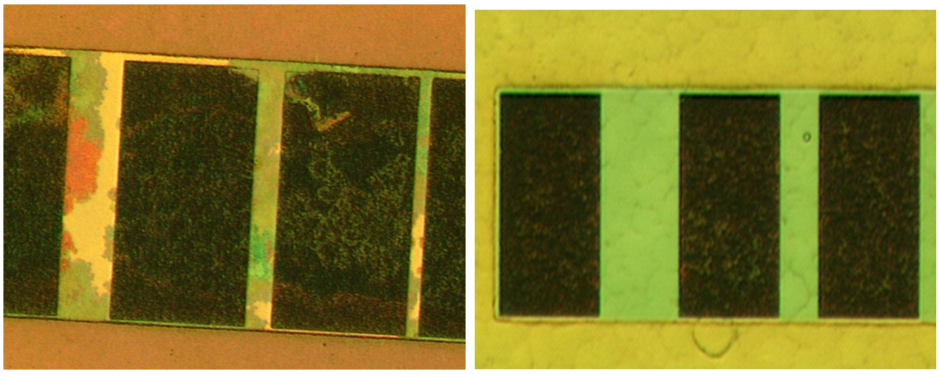
The NCD films grown under these conditions are primed for efficient heat extraction but a final verification would require the addition of a heat sink on top, a feature which is not covered in this work.

4.1.2 *HEMT stability under NCD growth conditions*

The above discussed requirements apply to the NCD side. On the HEMT side, a high thermal budget tolerance is required from the heterostructure and the device metallization and passivation to tolerate the growth. Although the LM-InAlN/GaN showed very high thermal stability as was shown in section 3.4, this does not ensure the stability under actual growth conditions. To verify the stability, a bare heterostructure was coated with a PCVD SiO2/Si interlayer. The nucleation step (1.5 hrs at 750 °C) was followed by outgrowth of a 500 nm thick Diamond for 5 hrs at 740 °C. After growth, the NCD film was removed completely by plasma etching in RIE and HEMT structures were processed using standard fabrication process. The maximum output current density (1.2 A/mm) was identical to that of devices fabricated from the same wafer but without undergoing the Diamond overgrowth step, indicating that the polarization of the heterostructure was entirely preserved, and the heterostructure stable under such overgrowth conditions.

The next step was to grow a gateless HEMT. At this stage the ohmic contact stability has to be considered also. The standard Au-containing ohmic contacts were optimized for low contact resistance, but at high temperature operation or storage showed limited stability due to the ductility of Au as discussed in section 3.4. The NCD overgrowth experiments performed on gateless HEMTs using this type of ohmic contacts (after mesa etch) showed similar behavior of Au instability. Overflow of Au was observed even in the beginning of the growth process, short-circuiting the source and drain contacts (see Fig. 38a). To overcome this problem, the Au layer was completely removed and substituted by a top 25 nm Ta layer to protect the Ni surface from oxidation. The removal of Au from the ohmic contact allowed NCD overgrowth without degradation (see Fig. 38b). Further optimization of the ohmic contact stack was performed later as will be discussed in section 4.1.3.

So far these experiments used SiO_2 passivation, since it was routinely used as part of the NCD interlayer and known for its stability. However, this passivation is not the common

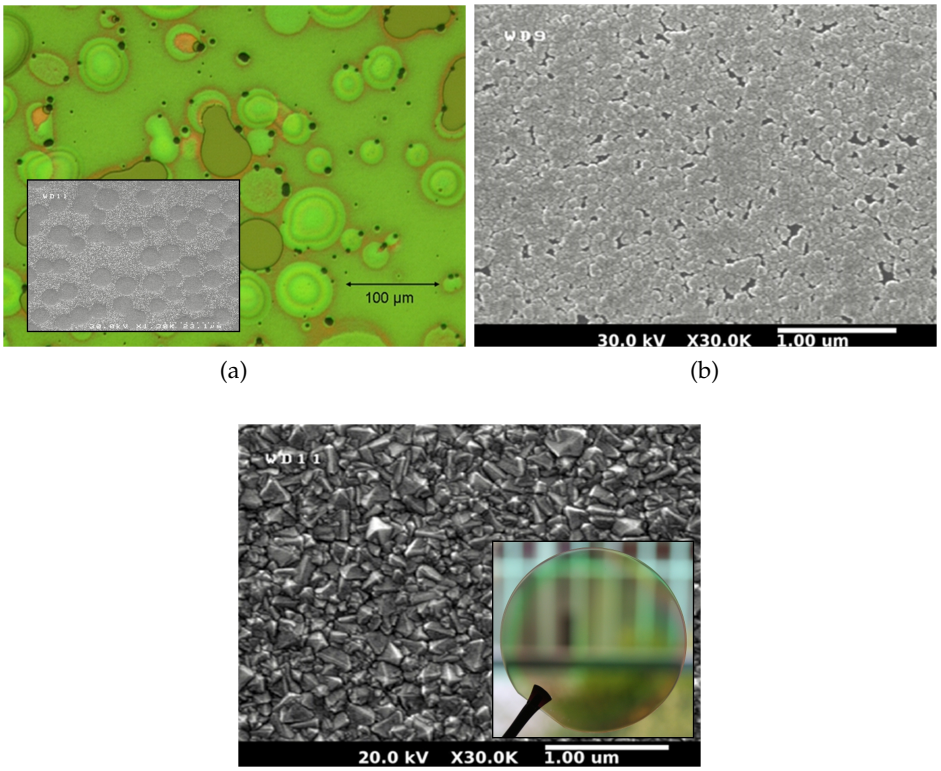


(a) (b)

Figure 38: (a) Standard Au-containing contacts did not survive the NCD growth process. (b) Au was removed from the stack and the gateless HEMTs could be overgrown.

passivation material in GaN based HEMT structures. Here it is disadvantageous, because of its extremely low thermal conductivity (the thermal conductivity of SiO_2 (quartz) is 0.064 W/Kcm), which might represent a bottle neck for the heat transfer. Si_3N_4 passivation on the other hand is widely used in GaN based HEMTs and most importantly proved very efficient, when combined with the thermal oxidation of LM-InAlN, as discussed in chapter 3. and has a thermal conductivity of around 1.05 W/Kcm, which is approx. 20 times that of SiO_2.

However, first experiments of NCD overgrowth on top of a nucleation layer / passivation layer stack of 100 nm Si_3N_4/100 nm Si, both deposited by PCVD, using NH_3 as nitrogen precursor, were not successful and resulted in the formation of bubbles (see Fig. 39a) after the nucleation step, which indicated outgasing from one of the materials of the stack. Since the interlayer stack was compromised in the areas where outgasing took place, NCD could not be outgrown to a coalescent layer. Since the pattern of bubble generation was homogeneous and not confined to the mesa pattern nor to the buffer layer outside the mesa, the problem seemed indeed confined to the Si_3N_4/Si stack. Both materials are known to contain hydrogen (depending on the deposition conditions), which tends to escape at high temperature, but the Si layer did not cause this problem, when deposited on top of the SiO_2 under the same deposition conditions. Thus the Si_3N_4 is the likely source of outgasing. In the beginning, it has not been clear, whether both films were the source of outgasing. Si could also act as non-transparent cap to the outgasing flux originating from hydrogen in the Si_3N_4 film, when the sample is exposed to a nucleation temperature above 700 °C as well as to a high H radical density. Thus, a PCVD deposition routine, using N_2 as nitrogen precursor was developed in first overgrowth experiments, and tested onto bare InAlN/GaN heterostructures. Fig. 39b shows an SEM image of Si/Si_3N_4 (50 nm Si nucleation layer on top of 60 nm Si_3N_4) after the nucleation step of 2 hrs at 750 °C and after subsequent 300 nm NCD outgrowth (3 hrs at 750 °C) in Fig.39c. Clearly, there was no uncontrolled hydrogen out-diffusion during NCD overgrowth. In addition, a high nucleation density of 1 x 10^{11} cm-2 could be achieved, and a uniform NCD growth on 2″



(a) (b)

(c)

Figure 39: (a) Optical image and SEM image of BEN on Si_3N_4 passivation deposited with ammonia precursor. Outgasing in the film prevented the growth of a closed layer. (b) BEN on Si_3N_4 passivation deposited with N_2 precursor. No outgasing was observed and high nucleation density is achieved allowing (c) closed films to be grown uniformly up to 2" wafers.

wafers could be obtained. The overgrowth on fully fabricated HEMTs discussed later used this Si_3N_4passivation deposited as described above.

4.1.3 *Development of high thermally stable metallization scheme*

A low contact resistance, highly thermally stable metallization scheme was developed to enable both the NCD growth and high temperature operation. The previous experiments showed that Au is the main contributor to contact degradation due to an excess, non-alloyed Au ratio. Since Al could also play the same role, specially since it has the lowest melting temperature among the used metals, the first modification on the standard ohmic stack was to reduce the Al thickness from 200 nm to 100 nm, and increase the Ti thickness slightly to 15 nm (from 10 nm). The second modification was to replace Au with an equally conductive metal but with less ductility. Cu was used for this purpose, with a thickness of 100 nm. Fig. 40 shows the complete contact stack used for HEMT overgrowth experiments. The Ta cap layer is used to protect the Cu surface from oxidation, but is etched away after

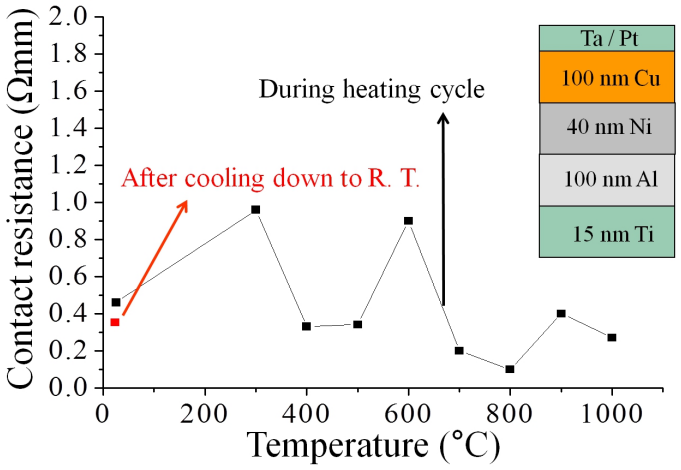
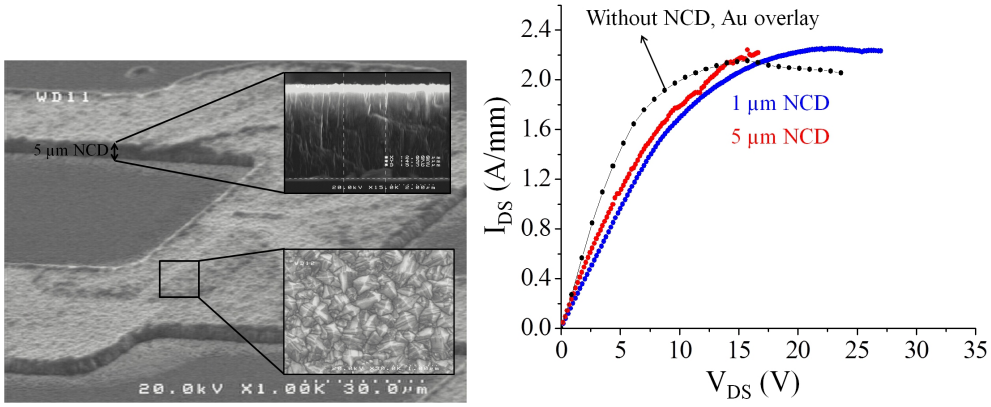


Figure 40: TLM measurement of the Au-free ohmic contact stack (shown in inset) at temperature up to 1000 °C. This stack is compatible with NCD overgrowth.

the complete fabrication and overgrowth step, when performing the pad opening step. The stack is annealed at 900 °C. TLM structures fabricated on LM-InAlN/GaN heterostructure, with 10 nm InAlN barrier, were prepared by optical lithography using this stack. After device passivation with 200 nm Si_3N_4, pads for ohmic contacts were opened through the passivation layer and the top Ta layer, which was replaced by Pt. This was accomplished by dry-etching followed by deposition of a 20 nm thick Pt layer deposited in-situ in the same etching/deposition reactor. Variation in the ohmic contact stack configuration was investigated by varying the Ta interlayer thickness between 0 nm, 12 nm and 25 nm, and varying the Cu layer thickness between 50 nm and 100 nm. Shown here is the results for the stack used in the NCD overgrowth later on and the detailed results of this experiment are reported in [250]. To evaluate the contact stability, R_c was extracted from TLM structures measured at room temperature, at 300 °C and then up to 1000 °C in steps of 100 °C, and after cooling down to room temperature (see Fig.40). The contact stack was structurally stable during the measurements cycle. The fluctuation of the extracted R_c values during the heating cycle is due to the difficulty in applying the same pressure for contacting the Tungsten probes each time the measurement was conducted with the difference in temperatures and the mechanical vibration of the vacuum chamber pump. Nevertheless, the contact maintained a relatively low value below 1.0 Ωmm up to temperatures of 1000 °C. Most importantly, after the whole heating cycle and cooling down to room temperature, R_c did not increase (it was even lower than before the measurement cycle due to enhanced alloying) which indicates the suitability of this metallization scheme for NCD overgrowth experiments. This metallization scheme also serves as the base for the contacts used in the HEMT high temperature operation reported in [194, 195, 228, 231].



(a) (b)

Figure 41: (a) SEM images of 5 µm NCD layers grown on gateless LM-InAlN/GaN HEMT. (b) The DC characteristics are comparable to HEMTs with 1 µm NCD and without NCD.

4.2 NCD coated HEMTs

This metallization scheme allowed direct verification of the HEMT stability under overgrowth conditions including the modified PCVD Si_3N_4, during different steps of growth. A set of experiments were conducted, where Diamond was grown on a 10 nm LM-InAlN/GaN gateless HEMT structure on SiC substrate. The growth was periodically interrupted and the HEMT current density was monitored. The NCD growth was conformal across the sample and no rupture occurred at the mesa edge and ohmic contact steps, which demonstrates homogeneous Diamond overgrowth with no cracks. Moreover, the ohmic contacts showed no structural degradation despite the long growth time at high temperature and frequent thermal cycling.

The thickest layer grown in gateless HEMT structures had 5 µm thickness (see Fig. 41a) deposited at 750 °C for 50 hours. As can be seen in Fig. 41b, the full current density of around 2 A/mm could be maintained after growth of 1 µm and also after growth had continued to 5 µm. This confirms indeed the exceptionally high thermal/electrical stability of the heterostructure and the ability to grow thick NCD layers, if required. The increase in the access resistance of the overgrown HEMTs compared to the ungrown HEMT seen in the graph is due to the Ta ohmic contact cap layer (which was not removed in this experiment), which has a higher resistivity than the Au top layer (in the control sample).

A similar approach was used to modify the gate contact. The Ni/Au stack was replaced with Cu, and capped by Ta. Ta is very difficult to evaporate in the E-beam chamber. So a sputtering source was used. To avoid oxidation of the Cu gate, the Cu metallization was also sputtered in the same chamber. Growth on fully fabricated HEMT including the gate, using the modified metallization (both ohmic and gate) and the modified Si_3N_4 in combination with the thermal oxide with 1 µm NCD layers is presented next.

4.2.1 *Fully overgrown HEMTs using BEN*

Initial experiments of overgrowth on fully fabricated HEMTs used the modified metallization scheme but with SiO_2 passivation. These results are reported in [200]. Here are the main conclusions of this experiment. A 0.5 µm thick NCD layer was nucleated and grown on the HEMTs of a 7 nm barrier LM-InAlN/GaN heterostructure. The devices were fully functional and the device did not show degradation as compared to the DC output characteristics before NCD growth. The characteristics of the devices before and after NCD growth were largely identical and neither the maximum channel current nor the pinch-off voltage has changed essentially. Thus, at the substrate side, the channel isolation and the GaN buffer layer properties have not been degraded. S-parameter measurements (performed by IEMN) yielded cut-off frequencies of f_t = 4.2 GHz and f_{max} = 5 GHz. These values, although the first one for such an NCD overgrown device structure, are still essentially lower than what can be expected. However, the RF-tested device showed high gate leakage. Therefore it had not been possible to identify the influence of any additional residual leakage caused by the NCD nucleation layer or the buffer layer. Moreover, the unchanged on-resistances illustrated also that the source and drain contact resistances and the electrical potential of the free surface between the contacts have not noticeably changed. The unchanged pinch-off voltage shows that neither the differential interfacial polarization nor the barrier layer separation between channel and gate metal have changed. Thus no gate sinking is observed.

Next was the growth of thicker NCD layers on HEMTs passivated with the thermal oxidation passivation scheme developed in chapter 3, but using the modified contact metallization and the modified Si_3N_4deposition recipe discussed before.

In this case a heterostructure with 10 nm barrier on SiC substrate has been used. The channel charge density N_s and the sheet resistance R_{sheet} of the fabricated devices were 2.7 x 10^{13} cm^{-2} and 199 Ω/□ respectively. In these devices a stack of Ti/Al/Ni/Pt (15 nm /100 nm /40 nm /60 nm) annealed at 900 °C was used for the ohmic contacts. The gate contact was Cu. The devices were passivated with 50 nm thick Si_3N_4 and a 50 nm thick Si layer was used as a nucleation layer. It should be mentioned that the fabricated devices were subjected to uncontrolled oxidation in one of the fabrication steps, thus lowering the maximum drain current and yielding a contact resistance of 2 Ω-mm and a sheet resistance of 400 Ω/□. Also, due to the unavailability of the Ta sputter source at the time the Cu gate metallization was not capped. Thus, due to Cu oxidation, gate line and gate feed resistances are high. The devices however were fully functional after overgrowth with 1 µm of NCD (10 hours at 730 °C after nucleation at 780 °C for $1\frac{1}{2}$ hrs).

Fig. 42a shows SEM images of the overgrown HEMT and a cross section of the 1 µm NCD overlayer, where no visible damage was observed even after such long process at 730 °C. The DC characteristics of the device before and after Diamond overgrowth (see Fig. 42b) are again largely identical with no change in the maximum drain current density or the pinch-off voltage. S-parameter measurements (see Fig. 42c) yielded cut-off frequencies of f_t = 16.8 GHz and f_{max} = 6.4 GHz. Here the low f_{max} is due to the high resistive gate line and the high on-resistances. The f_t x L_g product of 4.2 GHz.µm is however larger

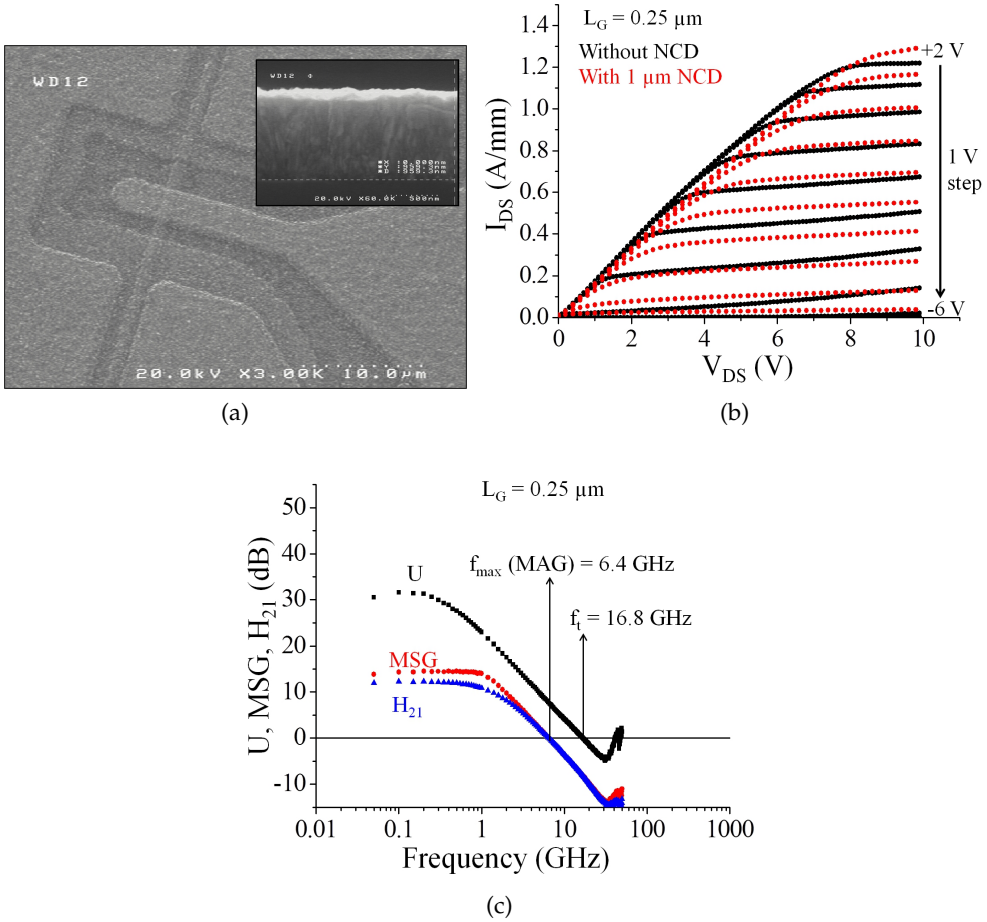


Figure 42: (a) SEM image of 10 nm barrier LM-InAlN/GaN nucleated by BEN and grown with 1 µm NCD layer. (b) The DC characteristics of the device are largely identical to the characteristics before growth and (c) the cut-off frequencies are in the GHz regime but still limited by parasitics (measurements performed in EBS, Ulm University).

than the one obtained from the previous device with SiO_2 passivation (1.05 GHz.µm). A conclusion on the role of the Si interlayer (especially concerning gate/drain feedback characteristics) could not be drawn, despite an attempt to identify this feature by equivalent circuit modeling. Nevertheless the cutoff frequencies would already allow operation in L-band (around 2 GHz). There is the possibility, that the BEN process results in lossy dielectric surface conditions. Although detrimental at microwave frequencies, these would indeed be very desirable in low frequency power devices. An alternative to the nucleation using BEN would be nanoparticles seeding, which is discussed next.

Growing thicker NCD films on full HEMTs was not successful in first attempts. No gate modulation was possible , and in best cases significant gate leakage currents were observed. This could be due to degradation of the gate diode, caused by stress generated by the thicker NCD films, or by a degradation of the passivation layer due to long growth

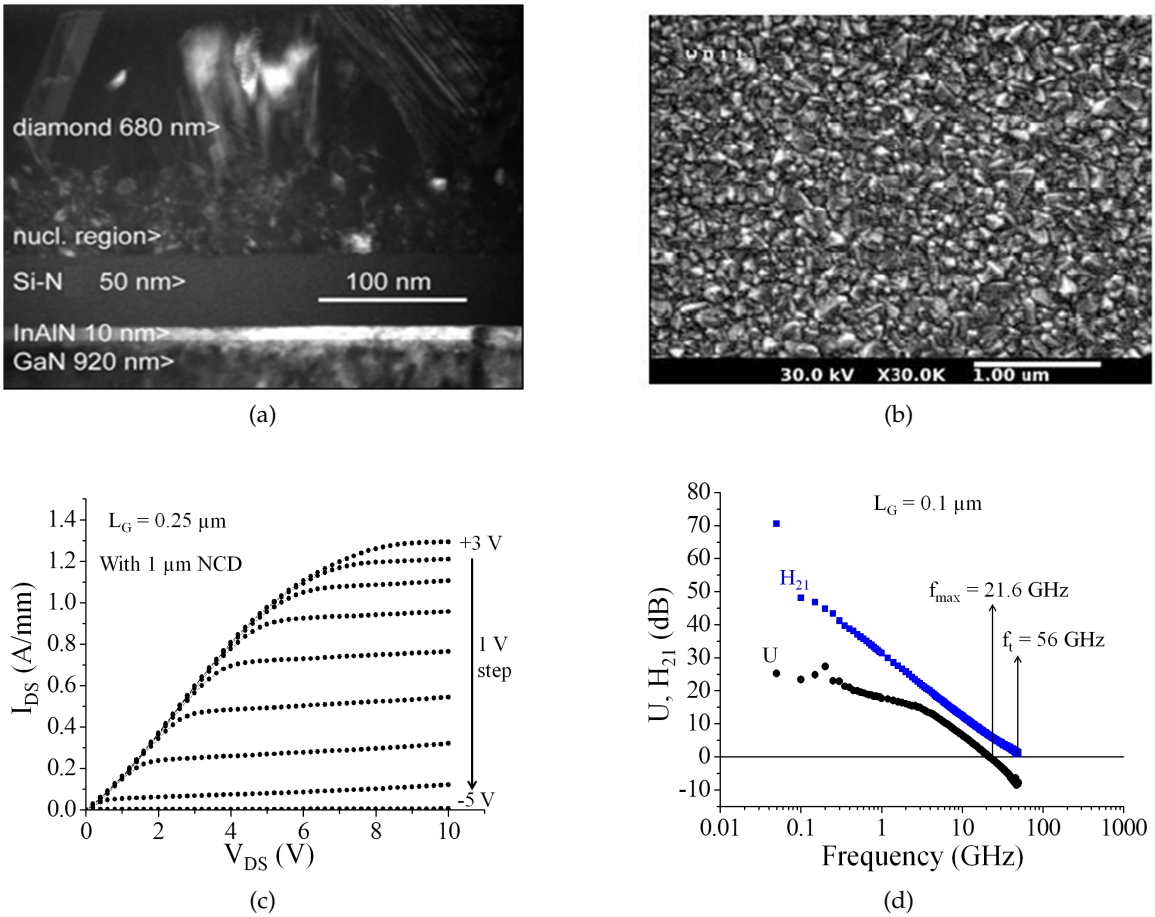


Figure 43: (a) TEM cross section (performed by MFA) of NCD layer nucleated by nanoparticles seeding and grown by MP-CVD followed by HF-CVD growth on InAlN/GaN HEMT (b) SEM image of the 1 µm NCD overgrown HEMT (c) DC characteristics of the 0.25 µm x 50 µm HEMT and (d) the cut-off frequencies of the HEMTs with 0.1 µm long gates (measurements performed in EBS, Ulm University).

times at high temperature. Suggestions on improving the gate and passivation technology for thick NCD growth will be presented in chapter 5.

4.2.2 *Fully overgrown HEMTs using nanoparticles seeding*

The alternative to initiate Diamond growth by nanoparticles seeding was investigated in collaboration with the National Cheng Kung University (NCKU) in Tainan, Taiwan, where the nanoparticles seeding was applied on the fabricated devices. With the seeding the carbide forming Si interlayer is not needed. Instead, a layer of Diamond nanoparticles is deposited on the surface of the passivation layer using an ultrasonic stimulation (in a liquid bath).

The same metallization and passivation schemes of the previously discussed device were applied on a heterostructure with a 10 nm barrier on SiC. The channel charge density N_s and the sheet resistance R_{sheet} of the as-grown wafer were 2.1 x 10^{13} cm^{-2} and 2.1 $\Omega/\square$ respectively. The nanoparticles nucleation was conducted in NCKU (with an average particle size of 30 nm) and followed by short growth at low temperature (around 80 nm at 550 °C) in a H_2/HC_4 plasma process (MP-CVD) to obtain a closed layer film. Due to the high seed density, the films are indeed continuous and without voids. The growth was then continued at Ulm in the HF-CVD equipment with growth parameters discussed earlier. Fig. 43a shows TEM cross section of the overgrown stack. It can be seen that the average grain size of the initial MP-CVD film grown directly after seeding at low temperature (550 °C), with the thickness of approximately 80 nm, is smaller than that of the HF-CVD layer grown at 750 °C. Thus, the first 80 nm thick MP-CVD layer may effectively result in an increased thermal transfer resistance as discussed earlier. However, this increase could be counter balanced by the absence of the additional Si nucleation interlayer needed for BEN.

Fig. 43b shows SEM images of the grown device. The outgrown Diamond film showed the same texture as the ones obtained by BEN, and thus no effect of the nucleation method on outgrowth was observed. The DC characteristics and the cut-off frequencies of the overgrown device are shown in Figures 43c and 43d respectively. The maximum drain current density of about 1.3 A/mm and the pinch-off voltage are identical to the one of devices fabricated on the identical wafer (but on a different piece) without the NCD overgrowth. The cut-off frequencies of the devices are the highest ever achieved for NCD overgrown HEMTs with an f_t of 35.4 GHz for a 0.25 µm long gate and 56 GHz for the 0.1 µm long gates (shown in the figure). The f_t x L_g values obtained for these overgrown devices are largely identical to what is usually obtained from HEMTs without NCD growth using SiC substrates. It can be assumed that the passivated surface does not possess the properties of a lossy dielectric in this case. It was however not possible to identify this feature as the main source for the different microwave performance of the device structure with seeded NCD overgrowth as compared to the structure with BEN initiated overgrowth. Certainly, seeding will be the preferred step for overgrowth, if thin NCD layers are desired, where the thermal conductivity is not of prime concern, like the case of the electrochemical sensor reported in [40], but the mechanical stability and adhesion of the seeded layers on large area has to be confirmed first for thick NCD growth used for thermal management applications.

4.3 GaN on single crystalline Diamond

The second heat dissipation approach would be using Diamond on bottom. The main challenges to this approach are the large lattice mismatch (26%), the large thermal mismatch (300%) (see table 3) and the non polarity of Diamond. As discussed in section 3.2 this may result in cracks or high dislocation density, rotated or inverted domains, thus a mixed polarity preventing the realization of a HEMT structure as was shown in [251]. The problem is complicated further by Diamond surface reconstruction at high temperatures [252] usually used in GaN epitaxy. To reduce these effects the low temperature MBE growth

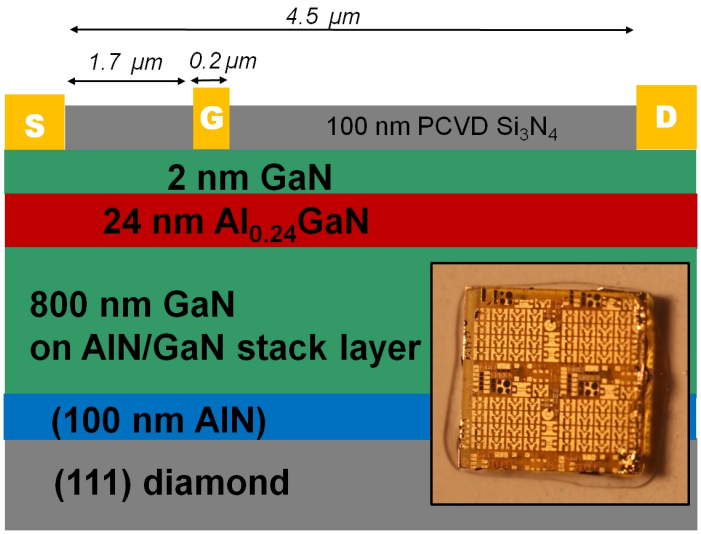


Figure 44: Cross section of AlGaN/GaN on (001) Diamond grown by MBE in EPFL. The inset is a photo of the fabricated devices on the 3 mm x 3 mm Diamond substrate.

approach was used by several labs. In 2003 Miskys et al. [253] demonstrated a p-n junction of Si doped (0001) AlN grown on (100) Diamond. However, no GaN heterostructure (using AlGaN as a barrier material) was demonstrated since then due to the still high dislocation density in the AlN. The first successful attempt to grow a GaN heterostructure was demonstrated in 2009 by A. Dussaign [254] and the first demonstration of GaN HEMT on single crystalline Diamond was presented in 2010, as part of the work presented here.

Here GaN is grown on (111) single crystal Diamond substrate by ammonia source MBE by EPFL. The growth was carried out on a 3×3 mm^2 (111) s. c. Diamond substrates supplied by Element Six Ltd.. An AlN buffer layer was first grown at low temperature. Details of the nucleation phase are reported in [254]. After the growth of the AlN layer, strain engineered interlayers, composed of 200 nm thick AlN and GaN multi-layers, were introduced to place the subsequent GaN layer under compressive strain before the epitaxy of a 800 nm thick GaN layer. The growth temperature and growth rate of GaN (AlN) were 800°C (900°C) and 1ML/s (0.1ML/s), respectively. Finally, a HEMT structure, composed of an AlGaN layer of 24 nm with an Al content of 28% and followed by 2 nm GaN cap-layer. A schematic cross section is shown in Fig. 44. Hall effect measurements show an electron mobility of 731 cm^2/Vs (1740 cm^2/Vs) and a sheet carrier density of 1.3 x 10^{13} cm^{-2} (1.4 x 10^{13} cm^{-2}) at room temperature (77 K), respectively, approaching those grown on Si. More details on the electronic properties of this heterostructure are reported in [255].

Since the single Diamond substrate available could not be diced, a conservative processing routine was carried on and the the HEMTs were fabricated as described in section 3.3, without recessing the GaN cap layer which yielded an R_c of 4.6 Ωmm as measured by TLM. The sheet resistance was 364 Ω/□ after passivation with 100 nm PCVD Si_3N_4. Fig. 45a shows the DC output characteristics 0.2 µm x 50 µm devices. The maximum I_{DS} is 0.73 A/mm but the characteristics are still limited by parasitics caused by a relatively large

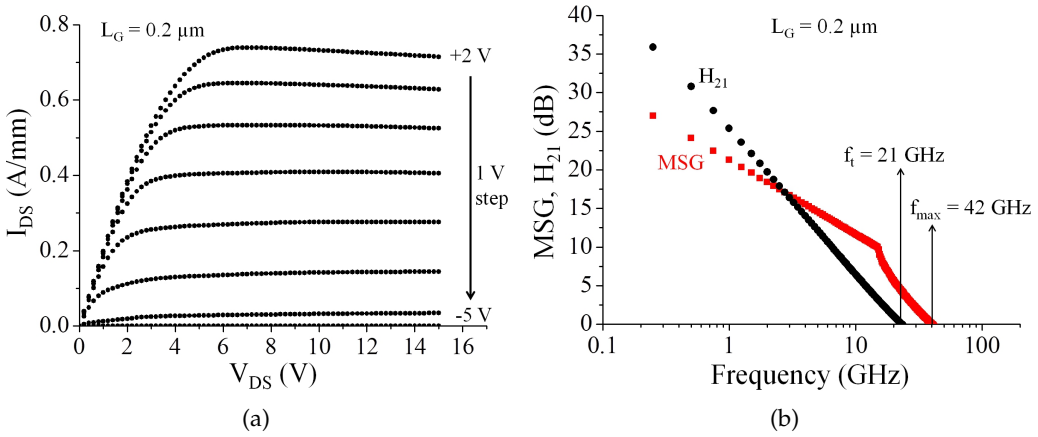


Figure 45: (a) DC output characteristics of 0.2 mm x 50 µm AlGaN/GaN HEMT on (001) Diamond. Complete pinch-off of the device at V_p = -5 V was seen throughout the devices with no significant buffer leakage. (b) The HEMT cut-off frequencies (measurement performed by IEMN)..

source drain distance of 4.5 µm and the high contact resistances. Complete pinch-off of the device at V_p = -5 V was seen throughout the devices with no significant buffer leakage. Devices with 0.2 µm gate length showed an f_t = 21 GHz and an f_{max} = 42 GHz respectively (measured by IEMN), as shown in Fig. 45b.

These results demonstrate the ability to grow high quality GaN heterostructures directly onto single crystal Diamond substrates, resulting in a GaN based HEMT structure with monolithically integrated Diamond heat spreader. The thermal aspects were not the subject of this work, but thermal analysis on similar structure reported in [256] revealed a thermal resistance reduced by almost 50% compared to SiC substrates. Although the (111) Diamond substrate provides a 3-fold symmetry preferred as a template for the growth of hexagonal GaN it is more expensive and more difficult to obtain and process than the widely available (001) substrates. Thus research has lately focused on the growth of GaN on (001) Diamond and was demonstrated in 2011 using MOCVD [257] and MOVPE [258].

5

CONCLUSIONS AND OUTLOOK

A conclusion of the work presented here is made as the following:

Technological steps were developed to fabricate an NCD-coated LM-InAlN/GaN HEMT, as a solution for the device self heating problem. However, for the device to suffer from this effect, it has first to be capable of delivering high output powers, thus the developed overgrowth technology should be compatible with the power device fabrication routine, and should not degrade the heterostructure. This is a main concern when using NCD films for heat spreading purposes, since growing highly thermally conductive films requires long growth times at temperatures above 700 °C in H-radical rich atmosphere. These growth imposes restrictions on the the heterostructure and the device components. The heterostructure itself should be initially highly thermally stable, and the device fabrication technology should also withstand the growth conditions and allow the fabrication of a power HEMT device. For example, despite the expected high performance of AlN, the limitations of mechanical stability due to the high lattice mismatch would not make it suitable for NCD overgrowth using simple planar technology. InAlN on the other hand can be grown lattice matched to the GaN buffer with an Al-content of 83%, thus gaining the advantage of a high Al-content and avoiding the mechanical stability problems, while maintaining a very high sheet charge density due to the larger polarization discontinuity with the GaN buffer.

Although this heterostructure was known for optical applications, little was known about its performance as a HEMT structure, so the first part of this work was focused on defining the capabilities and limitations of the LM-InAlN/GaN in a HEMT configuration. Experiments and simulations indicated a relatively low surface potential, allowing a high aspect ratio, and also indicated very high thermal stability of the heterostructure. The very high thermal stability of the heterostructure allowed unconventional processing to address intrinsic HEMT limitations like current collapse, and technological limitations like gate leakage, using thermal oxidation of the LM-InAlN, which proved efficient in reducing the gate leakage but most importantly was very efficient as a surface passivation component. Lag-free devices (at 4 GHz and up to V_{DS} of 20 V) could be demonstrated thus allowing high output power density of 11.6 W/mm, using simple planar technology.

Initial high temperature storage and operations tests up to 800 °C indicated that the NCD growth conditions were within the heterostructure capability. However, degradation in the other HEMT components, like metallization and passivation, was observed. An investigation of these components through spectroscopic means, SEM, TEM and electrical measurements helped in optimizing a highly thermally stable scheme capable of withstanding the Diamond growth process. The thermal stability of the optimized full HEMT was verified in high temperature tests and also under actual growth conditions, and lead to the first demonstration of a Diamond coated HEMT operating at frequencies in the GHz

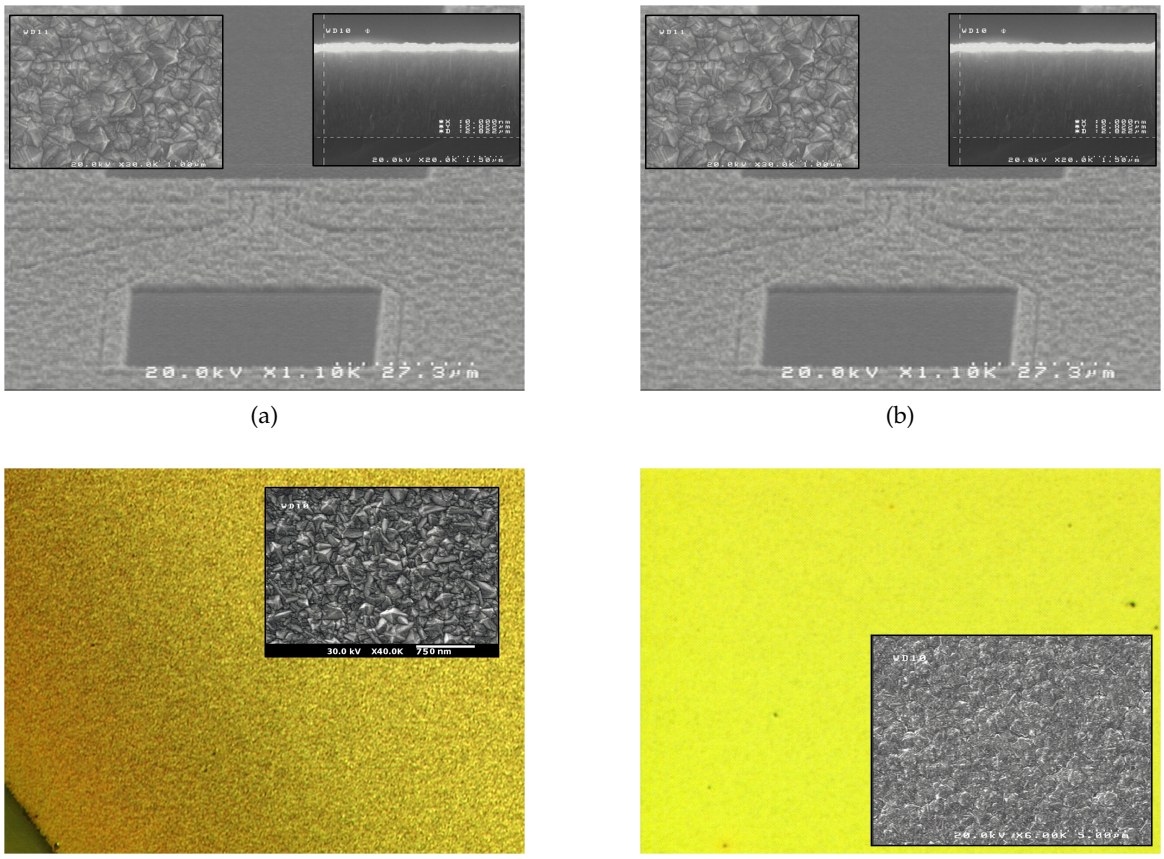
regime and up to f_t of 56 GHz. The fabrication routine developed for high temperature stability also helped in the demonstration of continuous operation of a HEMT at 1000 °C, and in a monolithically integrated Diamond-GaN ISFET for harsh electrochemical applications.

It was clear after the conclusion of this work that the heterostructure did not reach its limit yet, and further optimization of the HEMT structure can lead to even higher temperature applications. The degradation observed was due to the other HEMT elements like the metallization and passivation. Thus essentially further optimization of the HEMT elements can lead to very high temperature applications to be accessed without reaching the physical limits imposed by the semiconductor stability. A case in question is the growth of even thicker NCD films, more than 1 µm, on the full HEMTs. The first experiments used a direct approach of overgrowing fully processed HEMTs with more than 1µm NCD films without any change on the fabrication routine used to obtain HEMTs with 1 µm NCD films described earlier, except that the ohmic contacts did not contain Cu, but was used only as gate metal. No current modulation by the gate was possible on these devices and no current saturation was observed (overgrown with 3 µm NCD in this case takes 30 hours at 750 °C). In addition, gateless devices fabricated on the same sample also showed the same behavior. However, devices without BEN interlayer (thus without the Si interlayer) stressed with high temperature storage up to 1000 °C in vacuum did not show such degradation. These efforts to identify the source of the problem, lead to the following conclusion: local Cu diffusion into the Si_3N_4 passivation layer had caused local conduction paths on the surface between the contacts, effectively causing a short circuit. Finally, this could be traced to the CVD deposited Si_3N_4 passivation layer, being rich in Si, and alloying the mixing of excess Si with the Cu gate metallization during the long growth process at 750 °C. To rule out any possible interaction of Cu with a Si rich Si_3N_4 passivation layer, experiments were performed with a set of samples, where Cu had been replaced by Mo or Pt respectively and where the PCVD Si_3N4 deposition conditions have been modified. This experiment was actually an outcome of the technological optimization for ultra high temperature stable devices operation reported in [195]. The process modifications performed during this last set of experiments were in essence focused on the improvement of the passivation layer system and included a further adjustment of the deposition precursors. This modified gate and passivation scheme was used to fabricate a full HEMT from a 10 nm barrier layer. After that the BEN interlayer system was deposited and the structures nucleated and outgrown by approximately 3 µm NCD layer (28 hours at 750 °C) shown in Fig. 46b. Despite a still persistent leakage, current saturation was observed and the devices showed the expected open channel current density as compared to uncoated devices. Most importantly, current modulation by the gate could be verified (see Fig. 46b). The leakage of the devices still needs further investigation, because it may also be stress related (which may be related to the high brittleness of the Mo film). Nevertheless the experiments may still be viewed as an important achievement, indicating that successful overgrowth of fully processed HEMT device structures with thick NCD layers should be possible with further passivation layer optimization.

A possible alternative to the PCVD Si_3N_4 is the use of in-situ Si_3N_4, but stoicheometry is not easy to establish at the GaN growth temperatures. However, reports have shown the suitability of this passivation for high power GaN HEMTs. In addition, the passivation is deposited at high temperatures, around 800 °C, and thus is expected to be more stable than the PCVD Si_3N_4 deposited at 300 °C. For overgrowth purposes the passivation is also required to withstand the growth conditions, which is harsher than operation temperatures equal to the NCD growth temperatures, due to the presence of Hydrogen radicals. Initial experiments conducted on such passivation grown on LM-InAlN/GaN show encouraging results. No visible degradation was seen on the films and the usual NCD growth pattern could be achieved (see Fig. 46c).

Another alternative would be using ALD-deposited Al_2O_3, which also passed initial NCD growth tests as shown in Fig. 46d, indicating a high thermal stability. Combined with the thermal oxidation of the InAlN, this passivation can be used in a MOSHEMT configuration thus increasing the gate diode stability under high temperature operation by reducing the gate leakage significantly. In addition, when grown on the thermal oxide, which is largely crystalline Al_2O_3, it is highly likely that the interface between the heterostructure and passivation is smooth and continuous thus reducing the thermal resistance at this interface.

Since the growth of GaN on single crystal Diamond could also be demonstrated, a future goal would be to combine such substrates with the top NCD layers coating, thus creating an all-Diamond-encapsulated HEMT, with a maximum heat extraction configuration and a robust and inert surface, making it suitable not only for very high power applications, but also for operation in harsh environment.



(a) (b)

(c) (d)

Figure 46: (a) SEM image of 10 nm barrier LM-InAlN/GaN HEMT nucleated by BEN and overgrown with 3 µm NCD film (b) Despite the harsh and long growth conditions the HEMT could be modulated but suffered from a parasitic leakage due to a degradation of the PCVD Si_3N. An alternative to this passivation would be using (c) in-situ deposited Si_3N_4 passivation or (d) a ALD-deposited Al_2O_3. Both passivation passed initial NCD growth tests.

A

APPENDICES

Here the routinely used lithographic steps are described and an example of a Silvaco simulation input file is shown.

A.1 HEMT FABRICATION LITHOGRAPHIC STEPS

The lithography process details used for HEMT fabrication was as follows:

- Cleaning the wafer with acetone and 2-propanol
- Mesa isolation:
  - AZ 5214 photo resist coating at 6000 rpm
  - Hot plate Baking at 100 °C for 90 seconds.
  - Exposure at a constant intensity of 276W for 6.5 seconds.
  - Development using MIF-AZ 726 developer for 30 seconds.
  - Ar-plasma dry etch in RF-sputtering chamber with a power of 150 W, Ar flow of 17.6 sccm and a pressure of 50mT.
  - Resist removal in 1M-2p at 150 °C.
- Ohmic contact lithography:
  - LOR 7B photo resist coating at 6000 rpm, hot plate baking at 190 °C for 5 minutes.
  - Ti 09 photo resist coating at 8000 rpm, hot plate baking at 100 °C for 60 seconds.
  - Exposure at a constant intensity of 276W for 3.7 seconds.
  - Development using MIF-AZ 726 developer for 25 seconds.
  - Metal deposition in E-beam or sputtering in Ion-beam.
  - Lift off in 1M-2p at 150 °C.
  - Ohmic contact annealing in RTA at 800 °C for 30-45 seconds.
- Gate E-beam lithography:
  - PMMA/MA 33% resist coating at 3000 rpm, hot plate baking at 180 °C for 5 minutes.
  - PMMA-950K resist coating at 6000 rpm, hot plate baking at 180 °C for 5 minutes.
  - E-beam exposure with 50 KV.

  - deposition and lift off as in the ohmic contacts.

- Device passivation was done in a PCVD chamber.

A.2 HEMT STATIC SILVACO SIMULATION FILE

go atlas
SECTION 1: Mesh input 8nm AlInN
mesh nx=140 ny=140
x.m n=1.0 l=0.0 r=1.0
x.m n=140.0 l=0.1 r=1.0
y.m n=1.0 l=0.0 r=1.0
y.m n=10.0 l=0.008 r=1.0
y.m n=70.0 l=0.03 r=1.0
y.m n=140.0 l=0.15 r=1.0
SECTION 2: Structure Specification, The polar.scale is used to adjust the default values of the simulator. The simulator does not recognize InAlN so InN is used as name and the material parameters are redefined later
region num=2 material=InN x.min=0.0 x.max=0.1 y.min=0.014967 y.max=0.023033 polarization polar.scale=-1.9
region num=1 material=Air y.min=0.0 y.max=0.014967
region num=3 material=GaN x.min=0.0 x.max=0.1 y.min=0.023033 y.max=0.15 polarization polar.scale=-0.9
#electrodes which should be defined in the simulator
electrode name=source number=1 x.min=0.0 x.max=0.0 y.min=0.15 y.max=0.15
#contacts, the above electrode is set to neutral
contact num=1 name=source
#background doping
doping region=2 uniform n.type conc=1e15
doping region=3 uniform n.type conc=1e15
#The interface counter charge is inserted as a line charge
interface charge=-2.6E13 region=2 S.I
#surface donor traps can not be inserted as a line charge but inserted in a 0.3 nm wide line
trap e.level=3.85 donor density=7e20 degen=1 x.min=0 x.max=0.1 y.min=0.014967 y.max=0.015333
SECTION 3: Material parameters. The band offsets are adjusted in this simulator by adjusting the affinities
material material=InN eg300=4.65 permittivity=11.6 affinity=3.8 alattice=3.189
# material
material=GaN eg300=3.42 permittivity=10.28 affinity=4.6 3 alattice=3.189
# material
material=Air
#model

```
model srh fldmob fermidirac print mobility material=GaN fmct.n fldmob.n
# SECTION 4: method and solution
method gumits=300 newton trap itlim=35 maxtrap=10 vsatmod.inc=0.1 carriers=1 elec
output con.band val.band j.total polar.charge charge
solve initial
save outf=8nmInAlN.str
quit
```

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Other contributions

Co-author of more than 20 international conference presentations and 5 poster presentations.