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Nanocrystalline Diamond Growth for Top Heat-Spreading Applications on GaN-based Devices

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ABSTRACT

Diamond is undeniably an exceptional material. With hardness, elastic module and thermal conductivity among the highest of all known materials, a wide bandgap, transparency from UV to IR, chemical inertness, high corrosion and radiation resistance – to name only a few of its properties – a broad spectrum of electronic devices would profit from the integration of diamond components. Due to the lack of large-area single-crystalline diamond substrates however, most applications have to rely on CVD poly-/nano-crystalline diamond films, which can be deposited on a wide range of substrates and surfaces as thin films, but whose properties may differ significantly from the ideal ones, due to the mixture of different carbon phases present in such films and due to their internal anisotropic microstructure. Besides, the harsh requirements of the CVD growth in terms of thermal budget may represent a serious obstacle towards the monolithic integration of diamond with other electronic materials.

In this work, several issues related to the direct growth of nanocrystalline diamond (*NCD*) films onto III-Nitrides for the thermal management of GaN-based high electron mobility transistors (*HEMT*s) are addressed and handled.

The first and most fundamental issue consists in fabricating GaN HEMTs able to withstand a diamond deposition process, which exposes for several hours the device to a plasma of H-radicals and to high temperatures above 700 °C. By using NCD overgrowth experiments performed on InAlN/GaN HEMTs as test-base, high temperature stable metallization systems (in which Au is replaced with Cu or with refractory metals such as Ta or Mo) and passivation dielectrics (with low as-deposited hydrogen content) were developed in this work, which led to fully-fabricated InAlN/GaN HEMTs successfully coated with 0.5, 1.0 and 2.8 μm NCD films, deposited at a temperature of 750 °C. Not only such devices largely preserved their DC and RF electrical characteristics after the diamond deposition process, but the maximum drain current density of about 1.3 A/mm and cut-off frequency f_t of 16.8 GHz obtained on the devices with 0.5 μm gate length and 1 μm NCD cap are the highest ever achieved for diamond-coated HEMTs.

This work investigates also the correlation between growth parameters and structural and thermal properties for submicron-thick columnar-*NCD* films to find out whether such films may reach high thermal conductivity figures, and how is the thermal conductivity influenced by their anisotropic microstructure. The results of the structural analysis by means of SEM, AFM and *HR-TEM* and of the thermal characterization by scanning thermal microscopy (*SThM*) and μ-Raman thermography show that such NCD films may indeed reach high k values, but are very heterogeneous, with a clear dependence of the thermal conductivity k on the film's in-plane grain size and thickness. They also indicate the heat is spread more efficiently by vertical conduction along the columns, with a vertical conductivity 2–3 times higher than the lateral in the first micron (1000 vs 300 $Wm^{-1}K^{-1}$ for the peak values), but due to the influence of the highly-resistive nucleation region at the bottom of the film, their average thermal conductivity may be even three times lower. However, they also show

that low thermal boundary resistance (R_{th}) (*TBR*) values at the nucleation interface (~5 m^2K/W) and nearly 50% higher k figures could be reached with optimized process parameters for the BEN and outgrowth stage of diamond deposition, the latter of which makes use of $\alpha-/\gamma-$parameter engineering to finely tune the geometry of the grains.

In its essence, this thesis develops all the fundamental technological blocks necessary for the fabrication of diamond-coated GaN-based HEMTs, besides laying the basis for future optimization work which could allow to improve such a promising concept, and thus eventually solve the self-heating issue in high power GaN-based devices.

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α	ratio of the growth rates on {100} and {111} faces
γ	grain growth gradient
k	thermal conductivity
k_B	Boltzmann's constant
τ_q	phonon scattering relaxation time
τ_U^{-1}	phonon scattering rate for Umklapp processes
v	average phonon velocity
v_g	phonon group velocity
ω	phonon frequency
ω_D	Debye frequency
θ_D	Debye temperature
α-Si	amorphous Si (a-Si)
2DEG	two-dimensional electron gas
AFM	atomic force microscope
ALD	atomic layer deposition
AlGaN	Aluminium Gallium Nitride
Al2O3	aluminum oxide
BEN	bias enhanced nucleation
CVD	chemical vapor deposition
CTE	coefficient of thermal expansion
FEA	finite element analysis
FEM	finite element method
FC	flip-chip bonding
FET	field effect transistor
HFET	heterostructure field effect transistor
HEMT	high electron mobility transistor

HFCVD	hot-filament CVD
HOD	highly-oriented diamond
HPHT	high-pressure high-temperature
InAlN	Indium Aluminium Nitride
lm-InAlN	lattice-matched Indium Aluminium Nitride
MCD	microcrystalline diamond
MMIC	monolithic microwave integrated circuit
MODFET	modulation-doped field effect transistor
MESFET	metal-semiconductor field effect transistor
MTTF	mean time to failure
MWPCVD	microwave plasma CVD
LP-MOCVD	low pressure metal organic CVD
MOCVD	metal organic CVD
MBE	molecular beam epitaxy
NCD	nanocrystalline diamond
PECVD	plasma enhanced CVD
PCD	polycrystalline diamond
PAE	power added efficiency
RIE	reactive ion etching
RT	room temperature
RTA	rapid thermal annealing
SiO2	silicon oxide
SiN	silicon nitride (Si_xN_y, Si_3N_4)
SiON	silicon oxy-nitride (SiO_xN_y)
SEM	scanning electron microscope
SThM	scanning thermal microscopy
TDTR	time domain thermo reflectance
TEM	transmission electron microscope
HR-TEM	high resolution transmission electron microscope
TBR	thermal boundary resistance (R_{th})
UNCD	ultra nanocrystalline diamond

1 INTRODUCTION

Since the birth of solid state electronics in the 1950's, silicon has been the material of choice for the realization of a wide range of electronic devices. The availability of high purity, monocrystalline silicon coupled with the ease of doping and a native oxide of high quality paved the way for such a wide adoption. Even in power electronics applications, where high breakdown voltage and high switching speeds are desirable, silicon dominated the scene, despite energy losses due to its narrow bandgap and a low carrier mobility.

The increasing demand for devices with a higher efficiency in power conversion, able to operate at higher power, higher frequency, higher temperature than the Si-based ones spurred intense research on compound semiconductors with a wider bandgap, SiC and GaN being the most promising alternatives to Si.

GaN and the III-Nitrides material system (GaN, AlN, InN and their ternary/quaternary compounds) benefit from an extensive experience base in material growth and processing gained through 40 years of development in the field of optoelectronics, which enables today the fabrication of several key devices for power electronics, e.g. heterostructure FETs and Schottky diodes [1, 2, 3, 4]. In particular, GaN-based heterostructure field effect transistors (*HFETs*) are suitable candidates to replace Si power transistors, in respect to which they offer nearly ten times the power density, enabling at the same time dramatic reduction of both the power loss and the chip area due to low on-resistance and high current switching [5].

However, the raise of the power levels in these devices (up to 40 W/mm [6]) poses serious challenges for their thermal management and, as a consequence, for their long-term reliability. In fact, a higher device density and higher RF power both lead to increasing thermal loads on the packaging, whose thermal pathways may quickly saturate causing self-heating, if inadequate in removing the excess heat. Self-heating in turn leads to reduced electron mobility [7, 8], thus degrading device performance. Severe heating may even damage the device itself by degrading source, drain and gate electrodes due to accelerated electromigration, thus causing device failures and reliability problems. Furthermore the heat generation in these devices is not uniform across the active area, rather it is localized in specific spots, which are significantly hotter than the surrounding areas. At power densities above 10 W/mm the hot-spot localized near the gate contact [9] may reach temperatures above 200 °C, which is considered a safe upper threshold for long-term operation [10].

It is clear on one hand that a thermal design aiming at reducing the working temperature of GaN HFETs is critical for high power applications and on the other hand that a classical approach to the problem is largely inadequate for GaN. In a conventional packaging design, soft or hard solders are used to mount the power transistor into a package, which is subsequently attached to a heat sink by means of a thermal paste as an interface material. The resulting thermal path includes the full thickness of the device as well as the package and the interface materials, each of which contributes with its thermal resistance to the total thermal impedance. With

such a high thermal impedance this configuration is unable to handle the power dissipated by a GaN transistor if driven to its limits. Several thermal designs have therefore been proposed during the years for self-heating mitigation, each with its set of trade-offs.

For instance, a way to reduce the peak temperature in GaN *HFET*s consists in attaching a heat spreader, whose function is to distribute the heat across a larger area before sinking it, directly to the substrate side of the device. The effectiveness of this solution depends primarily on the thermal conductivity of the GaN epi layer and the substrate on which GaN is grown, apart from the interface resistance of the bonding material, since the heat has still to cross these layers before reaching the ultimate heat-sink. Commercial substrates for GaN epi layers include sapphire, Si and silicon carbide (SiC), which are single-crystalline and have thermal conductivities of 40, 150 and 340 $Wm^{-1}K^{-1}$ respectively. Even if SiC is the best choice thermally, its high cost per wafer make it less attractive compared to a cheaper sapphire or silicon substrate, which can be either thinned down [11], drilled with via-holes [12, 13, 14, 15, 16], or completely removed after the HFET fabrication [17] to compensate for its poor thermal conductivity.

A substrate that has far superior thermal properties to that of SiC is diamond. With thermal conductivity up to 2200 $Wm^{-1}K^{-1}$, both single-crystalline and thick, *CVD*-deposited poly-crystalline diamond would offer optimum heat spreading for GaN devices. Indeed recently GaN-on-Diamond devices have been demonstrated [18, 19, 20, 21, 22, 23], which exploit the exceptional thermal conductivity of diamond to achieve by far the best results in terms of heat dissipation. GaN epi layers can be attached to a diamond carrier after removing the initial substrate or diamond can be used as a substrate for GaN epitaxy. Although the former method is simpler under the device processing point of view, since the HFET can be fully fabricated prior to the bonding process, it has to cope with several technical challenges concerning the bonding areas. Obtaining a uniform and flat GaN epi layer after the substrate removal (Si, sapphire or SiC), achieving a mechanically strong and uniform diamond bond with very low GaN/diamond thermal interface resistance and minimizing wafer bow issues due to GaN/diamond CTE mismatch are indeed crucial factors for a successful integration. The second method instead, i. e. growing GaN epi-layers on diamond, is troublesome under the material growth point of view; in fact the heteroepitaxial growth of hexagonal GaN-based heterostructures on diamond (either 111-oriented single crystals or polycrystalline diamond plates) has to cope with the large lattice mismatch (26% on a 111-oriented substrate) and the difference in thermal expansion coefficients (~300%) of both materials systems.

A way to reduce the impact of the thermal bottlenecks at the interface between GaN epi-layer/substrate consists in establishing a top-side heat extraction pathway. This is commonly achieved by flip-chip bonding the GaN HFET to a carrier material with high thermal conductivity like single-crystalline AlN (which has a k of 270 $Wm^{-1}K^{-1}$ [24]). In this case the heat-spreading in the carrier reduces both the local as well as the overall chip temperature, even when GaN is grown on a poor thermally conductive substrate. Indeed GaN HFETs grown on sapphire and FC-bonded to AlN by Au bumps reached similar power dissipation efficiencies to the ones of GaN on SiC [25, 26]. Factors such as the number and location of the bonding bumps [27] as

well as the material chosen for the filling [28] have to be taken into account to allow efficient heat extraction from the device in a wide range of power densities.

A step forward in GaN thermal management by such a top-side heat extraction approach would be the direct integration of a diamond heat spreader on top of the HEMT. In this case the improvement would be double-fold, combining higher thermal conductivity in the spreading layer with a close proximity to the hot-spot. Furthermore, a low thermal interface resistance may be achieved due to the absence of any intermediate bonding layer. Nanocrystalline diamond (NCD) is the most attractive candidate for this purpose; besides benefiting from the possibility of large area deposition, the ability to fine control its material properties through the deposition parameters [29] allows to grow thin layers, which may reach high thermal conductivity figures in just a few microns [30].

Although promising, the direct overgrowth of GaN-based HEMT devices with NCD presents a number of technical challenges, which have prevented to pursue this approach to its full extent. The first and most important challenge consists in fabricating a *HEMT*, which could withstand the harsh conditions and high thermal budget of diamond deposition. This means that each component of the device – GaN buffer layer, heterostructure, ohmic and gate contacts metallization, device passivation – must be able to survive several hours at temperatures above 650 °C in a hydrogen-rich plasma. Moreover, the NCD deposition process should not degrade the DC/RF performances of the HEMT. This is the technical challenge, Seelman-Eggebert *et al.*, who first attempted to coat AlGaN/GaN HEMTs with NCD in 2001 [31], were only in part able to meet. Indeed to prevent any damage to the GaN device they had to adopt a low diamond deposition temperature of 500 °C, even if that meant to grow a nanodiamond film of low crystalline quality, and hence with poor thermal conductivity. More recently, Tadjer *et al.* [32] proposed a diamond-before-gate fabrication scheme for AlGaN/GaN HEMTs, in which a thin, 0.5 µm thick NCD cap layer is deposited at 700 °C on the gate-less device and the gate contact is subsequently evaporated in a recess etched into the diamond film. This fabrication scheme is safer for the gate contact, which is easily prone to damage due to the high thermal stress induced by the diamond deposition process. However, short gate lengths require deep and narrow recesses in the diamond overcoat, which are difficult to achieve.

Besides the device-related issues, an additional challenge is represented by the method chosen to enhance diamond nucleation on top of the device passivation. It must enable high nucleation densities, at the same time assuring strong mechanical adhesion and good thermal contact with the lowest possible thermal interface resistance. Even NCD deposition itself may represent a challenge, since NCD is an anisotropic material whose thermal properties depend strongly on its growth mode and will change with outgrown thickness [33]. In addition, horizontal and vertical thermal conductivities may not be identical, especially at small distances from the nucleation layer [34]. Moreover, since most characterization methods provide only spatially-averaged values of the heat conductivity k, the thermal properties of such thin nanodiamond films and thus their heat extraction and spreading effects are still under debate.

The work of this thesis stems from the need to address the above mentioned technical challenges and enable the integration of nanocrystalline diamond thin films onto GaN-based *HEMT*s for top heat-spreading purposes. The heterostructure

adopted here is InAlN/GaN, chosen for its ceramic-like chemical and thermal stability, with reported FET operation up to 1000 °C in vacuum [35]. The processing routine developed in this work allowed fully processed InAlN/GaN HEMT devices to be coated with micrometer-thick NCD films, deposited at a temperature of 750 °C, while preserving their electrical characteristics [36, 37]. Significant effort has been invested in optimizing the diamond deposition parameters to grow thin, high thermally conductive NCD films. Their anisotropic thermal conductivity was characterized in this work for the first time (to the author's best knowledge) by means of scanning thermal microscopy (*SThM*) and μ-Raman thermography techniques and correlated with the film microstructure [38].

OUTLINE OF THE THESIS

After stating the motivation behind this work in the introduction, Chapter 2 presents an overview of the key features of wide bandgap semiconductors, focusing on GaN and the III-Nitride material system. The advantages of the InAlN/GaN heterostructure compared to the conventional AlGaN/GaN for electronics in extreme conditions are also discussed. Chapter 3 describes the self-heating issue affecting GaN-based power transistors and reviews the solutions currently adopted to mitigate it. The last section of the chapter is dedicated to a thermal simulation comparing the effect of these different thermal designs on the channel temperature of a GaN-based HEMT. The results of the simulation indicate the top-side heat-spreading approach by means of nanocrystalline diamond as the most effective in reducing the hot-spot temperature. In Chapter 4 the growth of diamond films by chemical vapour deposition is described in details, with particular attention to the hot-filament technique and the BEN-on-interlayer technology developed in this work for the growth of thin nanodiamond films on GaN devices. Chapter 5 reviews the main experimental results of thermal conductivity measurements conducted on poly-crystalline diamond, which highlight the correlation between thermal properties and film microstructure. The influence of nanodiamond deposition parameters on the film microstructure will be discussed in Chapter 6, where the rationale behind the choice of the adopted set of parameters will also be explained. Chapter 7 describes the diamond overgrowth experiments which led to identify and to improve the HEMT components detrimental for the device stability at high temperature. The work on a new metal stack for the contacts and on a suitable device passivation will be illustrated. Moreover, the electrical characterization of InAlN/GaN HEMTs successfully coated with μm-thick NCD overlay will be discussed. In Chapter 8 the thermal characterization of the nanocrystalline diamond overlay by *SThM* and μ-Raman is described. The results of the analysis are discussed and the extracted values for the anisotropic thermal conductivity are correlated with the film microstructure. Finally, the conclusions and a perspective on future developments and applications enabled by the diamond coating approach to the self-heating issue are summarized in Chapter 9.

2 GAN-BASED HEMTS

2.1 WIDE BANDGAP ELECTRONICS

The ideal semiconductor for power applications should possess a high breakdown voltage, excellent transport properties, high thermal conductivity, chemical inertness and mechanical stability, besides allowing to fabricate both unipolar and bipolar devices with low parasitics. Although most of the power devices today in the market are made from silicon or GaAs, as these materials reach their performance limits, in the future they are set to be partially replaced by wider bandgap semiconductors such as SiC and GaN. The reasons behind this shift can be understood by referring to Table 2.1, where the material properties associated with high temperature, high power, high frequency application of SiC and GaN are compared to the aforementioned Si and GaAs.

The wide bandgap of GaN and SiC, about three times larger than the one of Si, makes them more suitable for high temperature/high power electronics. In fact, SiC and GaN may reach much higher temperatures than conventional Si, Ge, GaAs, without incurring in uncontrolled conduction caused by thermally-generated carriers. Hence power devices can better tolerate harsh, hot environments with less cooling issues. Furthermore, with a wide bandgap comes a high breakdown field, which scales roughly with the square of the energy gap. Therefore those power devices, which have a vertical device structure, can be made thinner than their Si-based counterparts and have a smaller resistance of the drift region when based on wide bandgap semiconductors.

GaN features excellent electron transport properties, including good mobility and a high saturated drift velocity, hence making this material very promising for microwave devices. Since the high-frequency switching capability of a semiconductor material depends on its drift velocity, with drift velocities more than twice the one of Si at low field, power devices based on GaN could be switched at higher frequencies than their Si counterparts. Moreover, a higher drift velocity allows faster charge removal and shorter recovery times for power diodes.

SiC has a thermal conductivity, which is three times the one of Si and nearly one order of magnitude higher than GaAs. A high thermal conductivity is crucial for the thermal management of high power devices, whose power losses are in the order of several Watts/mm. Altough bulk GaN crystals may reach thermal conductivities similar to the one of SiC [39, 40] the hetero-epitaxial layers used in the actual devices include defects, doping and oxygen impurities, which reduce the heat transport capabilities and make them comparable to Si, yet about three times better than GaAs. Furthermore, the power-frequency limit of SiC and GaN is two orders of magnitude higher than Si and GaAs, as indicated by the Johnson's figure of merit (JFM) [41].

Although SiC and GaN have similar capabilities, GaN supports a heterostructure technology within the III-Nitrides material system, which has no SiC equivalent. Quantum wells, modulation-doped heterointerfaces, and heterojunction structures

Table 2.1: Semiconductor properties from [42, 41, 43].

property	Si	GaAs	GaN	4H-SiC
$E_g\,(eV)$	1.12	1.4	3.4	3.3
ϵ_r	11.8	12.8	9.5	10.0
$\mu\,(cm^2/V\,s)$	1400	8500	1200	900
$E_{Br}\,(MV/cm)$	0.3	0.4	5.0	3.0
$v_{sat}\,(\times 10^7\,cm/s)$	1.0	2.0	2.5* (1.3)	2.0
$k\,(Wm^{-1}K^{-1})$	150	50	130	340
JFM[1]	1.0	7.1	2029	712
KFM[2]	1.0	0.45	1.6	5.2

* peak value at low field, within brackets the value at high electric field.
[1] Johnson's figure of merit, normalized to Si.
[2] Keyes' figure of merit, normalized to Si.

can all be made with III-Nitrides, thus leading to new device concepts for electronic devices (and also to new spectral regions for optical devices).

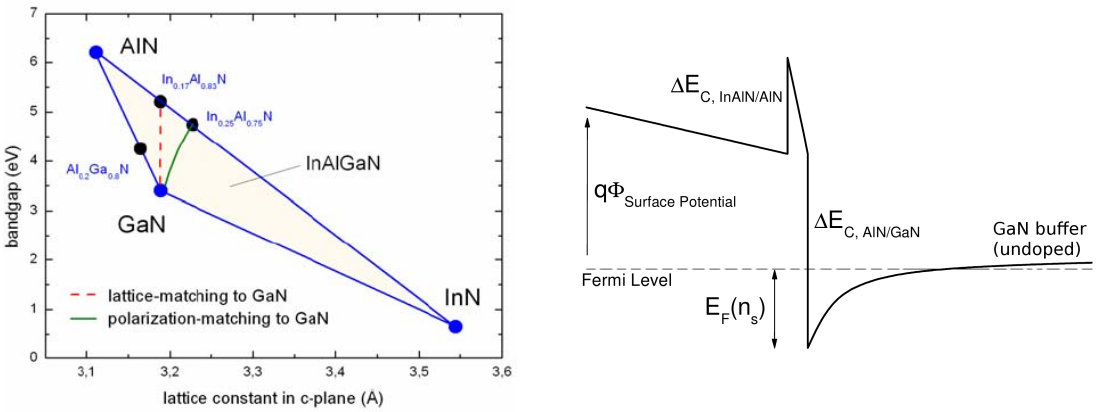
2.2 III-NITRIDES HETEROSTRUCTURES

The group III-Nitrides comprises AlN, GaN, InN and their ternary and quaternary alloys, which are all wide bandgap materials and can crystallize in both wurtzite and zinc-blende polytypes. In the wurtzite (hexagonal) lattice configuration GaN, AlN and InN have direct room temperature bandgaps of 3.4, 6.2 and 0.7 eV, respectively. They are polar materials, with both spontaneous polarization and piezoelectric polarization originating from the high electronegativity of the nitrogen atoms inside the crystal. The direction of the polarization depends on the crystal orientation, which distinguishes between N-face or Ga(Al, In)-face surfaces. In zinc-blende (cubic) form instead, GaN and InN have slighly smaller direct bandgaps, while AlN is indirect. In addition, the cubic structure is symmetric, hence leading to a non-polar lattice, which is of particular interest for optical applications. However, since the zinc-blende structure is more troublesome under the material growth point of view, all electronic applications today rely on the hexagonal configuration.

Figure 2.1 shows the diagram of bandgap versus lattice constant for the III-Nitride system with wurzite lattice. The typical heterostructure in this system consists of a ternary alloy – the barrier layer – grown on top of a relaxed GaN buffer layer, the interface between the two being the channel. At the boundary between the two crystals the superposition of two distinct polarization effects, namely the difference in spontaneous polarization between GaN/barrier plus the piezo-polarization induced by the strain of the lattice mismatch, gives rise to an electrically charged region. Due to the conduction band discontinuity between the two semiconductors, the electrons (holes) diffusing from the ternary alloy into the GaN buffer layer are confined in the quantum well at the interface, where they form a two-dimensional electron (hole) gas

(2DEG/2DHG), whose high mobility can be exploited to fabricate lateral-conduction devices. The barrier layer in the heterostructure is commonly a nm-thick ternary alloy of III-Nitrides with bandgap larger than GaN, i.e. $Al_xGa_{1-x}N$ or $In_xAl_{1-x}N$. In Figure 2.1b a schematic representation of a GaN/AlGaN heterostructure is presented.

AlGaN layers grown on GaN typically have a thickness in the range of 10–30 nm with an aluminum content, which is commonly kept between 20 and 40% to limit the tensile stress induced by the lattice mismatch with GaN. An InAlN barrier instead can be grown lattice-matched to GaN [44], and hence stress and piezo-polarization free, when an Al ratio of 83% is used. The advantages of such a high Al-content in the InAlN barrier are twofold. In fact, on the one hand the spontaneous polarization in the InAlN/GaN heterostructure induces a larger carrier density in the 2DEG-channel compared to typical AlGaN/GaN, hence allowing higher output current densities to be reached. Moreover, the InAlN alloy exhibit high thermal/chemical stability and exceptional robustness against harsh environments, with InAlN/GaN HEMTs reported to operate at 1000 °C [35].



(a) (b)

Figure 2.1: (a) Bandgap versus lattice constant of III-N semiconductors. (b) Band structure of the InAlN/GaN heterostructure.

The electrical transport properties of the 2DEG in these materials are remarkable. For instance, an AlGaN/GaN heterostructure with an aluminum concentration of 26% and a lattice-matched InAlN/GaN heterostructure exhibit sheet carrier concentrations n_s of 8.54 $\times 10^{12}\,cm^{-2}$ and 2.07 $\times 10^{13}\,cm^{-2}$, respectively. These values are about 8–10 times higher than sheet carrier densities obtained in intentionally doped AlGaAs/GaAs heterostructures. Heterostructures with peak electron velocity and electron mobility of $3 \times 10^7\,cm/s$ and $\sim 2000\,cm^2/Vs$ respectively have been achieved [45], which are close to the values predicted by means of theoretical simulations [46, 47].

The possibility of forming thin native-oxide layers of Ga_2O_3 or Al_2O_3 to be used as surface passivation completes the list of III-Nitrides properties, highlighting the tremendous potential of these materials for power electronics applications. The progress in this direction has been accelerated by the extensive experience base of materials growth and processing developed in the past decades for optoelectronic devices.

2.3 III-NITRIDES GROWTH: SUBSTRATES AND METHODS

The deposition of III-Nitride materials is commonly carried out by MOCVD or by MBE [48]. The MOCVD technique makes use of metal organic compounds as metal sources and hydrides for the nitride source. Trimethyl-gallium/-aluminum/-indium (TMGa/Al/In) are normally used as gas precursors respectively for Ga, Al and In, while ammonia (NH_3) is the typical nitrogen source. The precursors are first mixed, and subsequently introduced into the reactor chamber by means of a suitable injector arrangement, which directs them towards a hot substrate. MBE, instead, is based on the evaporation under ultra high vacuum (UHV) conditions of Ga, Al, In, whose vapour beams are regulated by shutters and impinge on a heated substrate. Nitrogen is supplied either by ammonia or by N_2 passing through a RF plasma. Since there is no interaction between the beams, a precise control of the species reaching the substrate can be achieved, which results in layer-by-layer deposition with atomically sharp interfaces. MOCVD growth is performed at higher pressure and higher temperatures than MBE (~1000 vs ~700 °C), in respect to which it offers higher versatility and higher output capacity.

For both MOCVD and MBE the growth of high quality GaN critically depends on the substrate used for growth. In fact, due to the lack of bulk GaN substrates of reasonable cost and size, GaN epitaxial structures need to be grown by heteroepitaxy on foreign substrates. Table 2.2 lists some important parameters of the substrate materials adopted for GaN epitaxy, including lattice mismatch to GaN, coefficient of thermal expansion (CTE) and available size. The list includes sapphire, silicon, silicon carbide and diamond.

Lattice mismatch and difference in CTE affect both material growth and device reliability, mostly because of the strain induced in the material. Substrate isolation, instead, is crucial in lateral devices in order to avoid parallel conduction phenomena in the final device.

Historically, the III-Nitrides have been primarily grown on sapphire due to its wide availability and its hexagonal symmetry. In addition, sapphire is thermally stable at temperatures above 1000 °C and chemically inert in the gas environment required for GaN growth. However, sapphire has a poor thermal conductivity and, most importantly, large lattice and thermal mismatches with GaN. Growing relaxed GaN layers with low defect density can be achieved only by depositing a thin AlN or GaN buffer layer grown at low temperature (600 °C) prior to the high-temperature growth. The function of the buffer layer is to ease the transition between substrate and device-quality GaN layers. Silicon is the cheapest substrate, but has the highest lattice mismatch with GaN of ~17%. SiC is becoming the preferred substrate for GaN growth. It features the lowest lattice mismatch to GaN, provides good device isolation and its high thermal conductivity makes it especially attractive for GaN power devices. However, issues related to the material quality, due to a high density of defects, and the high costs have delayed its adoption in favor of Si.

GaN growth on diamond has been investigated in the last years aiming at exploiting its exceptional thermal conductivity for substrate-side heat spreading purposes in high power devices. Although HEMT devices grown by MBE on small, single-crystalline diamond stones have been already demonstrated [49, 22], the growth on large-area,

Table 2.2: Substrates used for GaN epitaxy (from [53], p. 56).

	Si (111)	Sapphire	6H-SiC	GaN (bulk)	Diamond (S.C.)
size (“)	12	4	4	2	<1
lattice mismatch (%)	17	13	3.4	-	11.8
CTE* ($10^{-6}\,K^{-1}$)	3.59	7.5	4.2	5.59	1.18
isolation ($\Omega\,cm$)	10^4	-	$\geqslant 10^{11}$	$\geqslant 10^9$	$\geqslant 10^9$
k ($Wm^{-1}K^{-1}$)	150	34	490	250	2200

* Coefficient of thermal expansion.

PCD substrates [50, 51, 52, 19] is the most attractive for the commercial applications, owing to the lower cost and wider availability of such substrates.

2.4 GAN-BASED HEMT DEVICE TECHNOLOGY

In the past several years, the electronic device development has emphasized field effect transistor (FET) structures, because this important class of unipolar devices has lower requirements under the growth and fabrication point of view compared to bipolar transistors.

The basic structure of a GaN-based HEMT is depicted in Figure 2.2. It is a unipolar device with three terminals, in which the gate electrode controls the carriers in the 2DEG channel flowing laterally from the source to the drain contact. The most common barrier layer is AlGaN grown on a GaN buffer layer. The gate contact can be realized either by a Schottky contact similar to MESFETs or with an additional oxide layer in between (MOS-HFET).

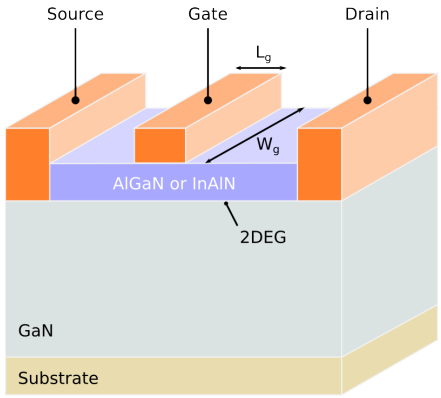


Figure 2.2: Schematic of the epitaxial structure of a typical GaN-based HEMT with an AlGaN barrier including gate, source and drain metal electrodes.

The growth of the heterostructure starts with the deposition of a nucleation layer on the substrate in order to achieve a two-dimensional growth. Nucleation on Si and SiC is typically performed using a resistive AlN nucleation layer grown at ~900 °C. One micron of GaN buffer layer is usually necessary to obtain a high crystalline quality for the channel. Then the barrier is grown. For AlGaN 25 or 30 nm is the

typical thickness, while for InAlN 5 to 15 nm may be deposited. Between the barrier and the GaN channel a thin, 1 nm thick AlN interlayer is grown, which significantly increases the carrier mobility. The HEMT fabrication proceeds with device isolation by mesa-type recessing or by Ar ion implantation of the inter-device area, followed by Ohmic contacts patterning and evaporation. The Ohmics metal stack, which consists of Ti/Al-based alloys (Ti/Al/Ni/Au or Ti/Al/Pt/Au), is then annealed for a short time (e. g. 30 s) at temperatures between 800 and 900 °C in nitrogen atmosphere. Finally the gate contact is formed with a Ni/Au, Pt/Au or Cu/Ta metal stack and the device is passivated.

Surface passivation is very important for GaN-based HEMTs, since it allows to passivate surface defects and to avoid drain current dispersion effects (i.e. the different current levels between DC and pulsed I-V characteristics). Depending on the device design, it can be performed at different stages of device fabrication.

One option is to passivate the surface before ohmics metallization, e. g. by means of in-situ SiN, which is a thin SiN film grown at high temperature (above 700 °C) inside the MOCVD reactor immediately after the growth of the heterostructure [54]. Device passivation can be otherwise performed after the gate has been fabricated, for example by means of ex-situ SiO_2 or SiN dielectric films deposited by PECVD at moderate temperatures of ~300 °C. An alternative passivation scheme consists in passivating the surface before gate formation by means of a thin dielectric film such as SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, MgO [55, 56, 57, 58, 59, 60, 61, 62]. In the case of a InAlN barrier, a thin Al_2O_3 film can be formed by controlled thermal oxidation at 800 °C in O_2 atmosphere [63, 64]. With such a design the gate behaves more like a MOS gate structure rather than a Schottky barrier gate used in regular HEMTs, therefore this kind of device is referred to as MOS-HEMT (see Fig. 2.3). The advantages of MOS-HEMTs compared to regular HEMTs are a significantly lower gate-leakage current and a larger gate voltage swing. The disadvantage is the possible injection and storage of charges in the dielectric [65].

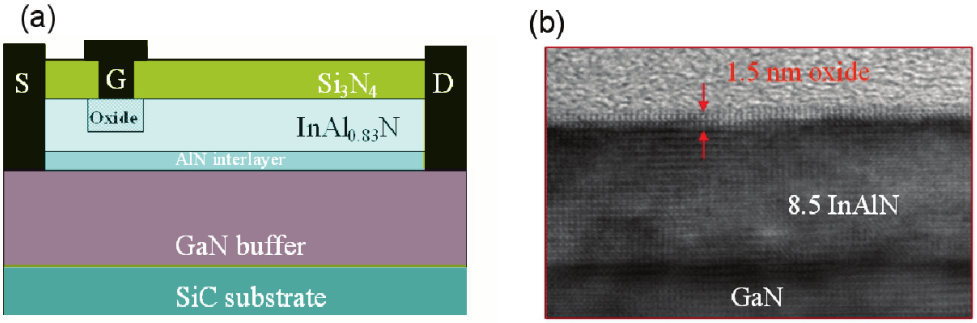
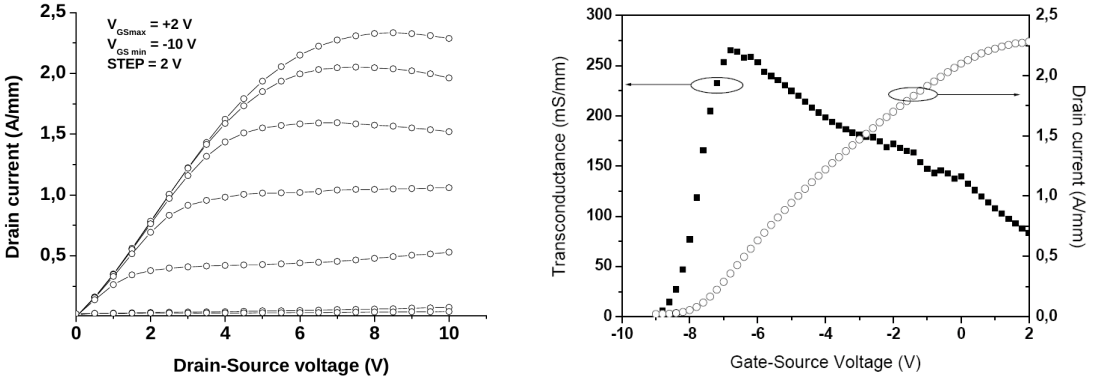


Figure 2.3: (a) Cross section of a InAlN/GaN MOS-HEMT; (b) TEM micrograph of the 1.5 nm native oxide formed onto the InAlN barrier by thermal oxidation at 800 °C.

2.4.1 *DC and RF characteristics*

The measured DC characteristics of a InAlN/GaN HEMT on sapphire with 13 nm barrier and 0.25 µm gate length are shown in Figure 2.4 [66, 67]. The critical parameters related to these characteristics are the maximum drain current (I_{max}), the threshold

voltage (V_T), the peak DC transconductance ($g_m(peak)$), and the breakdown voltage (V_{br}). The maximum DC output current at room temperature in this case was I_{max} = 2.3 A/mm at a gate bias $V_g = +2\,V$ with a peak transconductance $g_m = 265\,mS/mm$ at $V_{gs} = -6.5\,V$. Due to the lower sheet carrier density in the 2DEG, AlGaN/GaN HEMTs output current is typically of 0.7–1.2 A/mm, with transconductances of 200–250 mS/mm [68, 53].



(a) (b)

Figure 2.4: (a) I-V characteristics and (b) DC transfer characteristics of lattice-matched InAlN/GaN HEMT with 13 nm barrier grown on sapphire. Gate length was 0.25 µm and gate width of 25 µm (from [67]).

The RF parameters of interest for power transistors are the unity current gain frequency (f_T), the maximum oscillation frequency (f_{max}), the output power (P_{out}), maximum available gain (MAG) and power added efficiency (*PAE*). f_T and f_{max} can be extracted from the small signal RF behavior of the HEMT, tested by means of S-parameters measurements [69].

Gain and *PAE* are calculated from large signal RF characteristics as follows [70, 71]:

$$Gain = \frac{P_{out}}{P_{in}}, \tag{2.1}$$

$$PAE = \frac{P_{out}(AC) - P_{in}(AC)}{P_{in}(DC)}, \tag{2.2}$$

where $P_{in}(DC)$ is delivered by the DC supply, and is transformed into heat in the device. The variation of the PAE and P_{out} with P_{in} represents the large-signal behavior, of which the saturated P_{out} is an important figure of merit. The power density of a transistor P_{out} under class A operation is estimated to $\frac{1}{8} I_{max} (V_{br} - V_{sat})$. At a typical I_{max} of 1 A/mm and a V_{br} of 100 V, the RF output power is expected to be 12.5 W/mm; a figure of merit, which is 10 times that of Si and GaAs high frequency power devices.

In Figure 2.5a the small signal current gain h_{21} measured on a InAlN/GaN HEMT with gate length L_g of 0.15 µm and gate width w_g of 50 µm between 0.5 and 40 GHz at $V_{gs} = -6.5\,V$ and $V_{ds} = 10\,V$ is shown; cut-off and maximum oscillation frequencies extrapolated from the experimental points were 50 GHz and 60 GHz respectively [35]. These results may still be further improved by using a T-gate structure and by reducing the ohmic contact resistances.

Figure 2.5b shows the microwave power measurements on 4 fingers InAlN/GaN on SiC devices with $L_g = 0.25\ \mu m$ and $w_g = 75\ \mu m$, characterized at 10 GHz under CW conditions. DC bias conditions were $V_{ds} = +30\,V$ and $V_{gs} = -2\,V$. A power density of 10.3 W/mm with 51% power added efficiency and 15.6 dB of associated power gain were measured at room temperature for these devices [72].

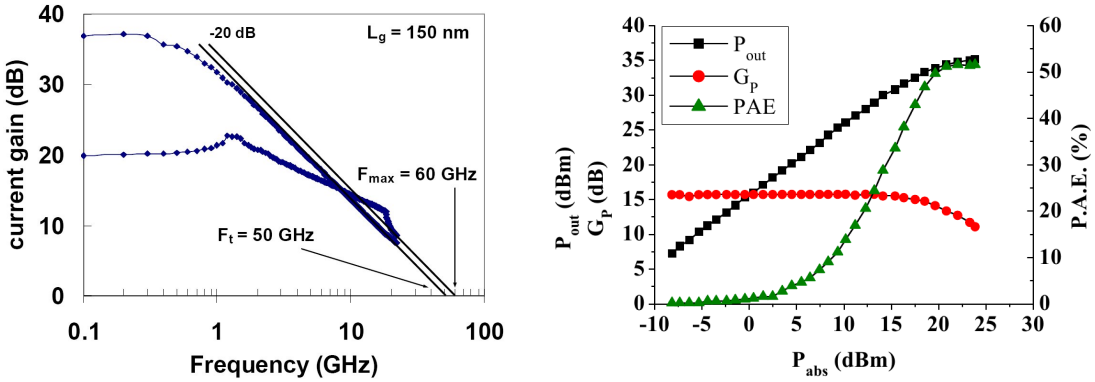


Figure 2.5: (a) Current gain versus frequency for a 0.15 $\mu m \times 50\ \mu m^2$ InAlnN/GaN HEMT biased at $V_{ds} = 10\,V$ (from [35]). (b) Output power, associated power gain and power added efficiency of 4 fingers $\times\ 0.25 \times 75\ \mu m^2$ InAlN/GaN HEMT measured in CW at 10 GHz (from [72]).

2.4.2 *InAlN/GaN HEMTs for high power*

Although most of the GaN-based HEMTs are based on the AlGaN/GaN heterostructure, a InAlN barrier layer enables higher current densities and higher transconductance, and hence is a very attractive alternative for high power, high frequency amplifiers and switches.

The RF power performances of InAlN/GaN HEMTs were reported by Alomari *et al.* on InAlN/GaN MOS-HEMTs realized by thermal oxidation of the InAlN beneath the gate area [63, 64]. They demonstrated that the combination of the MOS-type gate and a PECVD-deposited SiN passivation allows to generate the full RF output power density expected from the DC characteristics.

The processing routine outlined in their work consists in the following steps. First, device isolation is obtained by dry mesa etching in Argon plasma. Subsequently, ohmic contacts are formed by means of a stack of Ti/Al/Ni/Au annealed at 850 °C. Devices are then passivated with 30 nm of SiN deposited by PECVD. This is followed by the definition of the gate area by e-beam lithography and by the opening of the gate foot print by CF_4 plasma in a reactive ion etching (*RIE*) chamber. At this point, a native oxide film of approx. 1.5 nm can be obtained by four minutes of oxidation at 800 °C in O_2 (see Figure 2.3b). Finally the Ni/Au gate metallization is deposited by a separate e-beam lithography step and the ohmic contact pads are opened and re-metallized.

Figure 2.6a shows the DC (a) and RF (b) output characteristics obtained on one of such devices. The epi-layer consisted of 10 nm InAlN/GaN heterostructure grown on a SiC substrate. The 2DEG density and mobility of the as-grown layer at room temperature were $1.9 \times 10^{13}\,cm^{-2}$ and $1290\,cm^2/Vs$ respectively.

As for the DC characteristics, the maximum drain current density is 2.4 A/mm at a gate-source bias of +2.5 V, and the pinch-off voltage is -5.5 V. The three terminal breakdown of the devices (defined at 1 mA/mm) is 30 V.

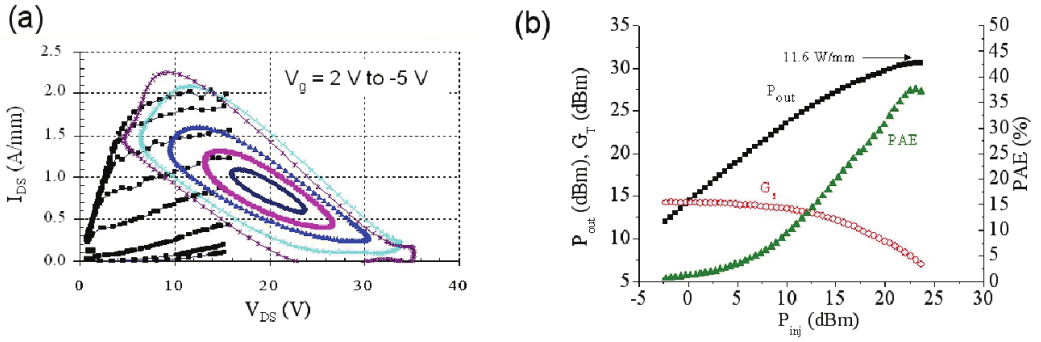


Figure 2.6: (a) RF load lines superimposed on the cold DC-pulsed measurement and (b) large signal RF measurements and output power at 4 GHz for the fabricated InAlN/GaN MOS-HEMT (from [63]).

As for the RF characteristics, for $L_g = 0.25\,\mu m$ the extrapolated cutoff frequencies are $f_T = 44\,GHz$ and $f_{max}(MAG) = 105\,GHz$, $f_{max}(MSG) = 107\,GHz$ ($V_{DS} = 15\,V$ and $V_{GS} = -3.5\,V$). Gate and drain lag characteristics measured with 500 ns pulses showed no major current dispersion. Moreover, from the output load line for various input power levels (superimposed on the DC characteristics in Figure 2.6a) can be observed that no current compression and virtual gate clipping are present. The channel could be fully opened up to 2.4 A/mm in stable overdrive conditions, indicating high breakdown strength of the thin native oxide layer.

From the large signal and output power behavior analyzed at 4 GHz for 2 x 0.25 µm x 50 µm devices (see Fig. 2.6b), a saturated output power density of 11.6 W/mm at a drain voltage of 20 V, and a *PAE* of 37% were obtained (due to a high contact resistance R_c of $0.8\,\Omega \cdot mm$). These figures confirm the exceptional high breakdown strength of the combined oxide/SiN passivation scheme.

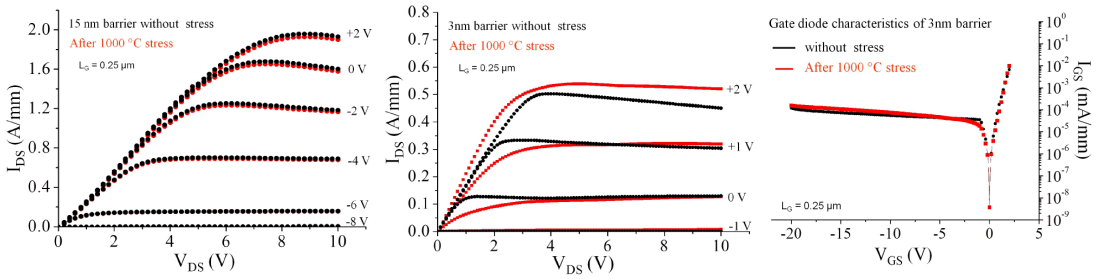
2.4.3 *InAlN/GaN HEMTs for high temperature electronics*

Besides being suitable for the fabrication of HEMT devices targeting high power applications, the lattice-matched InAlN/GaN heterostructure exhibits exceptional thermal and chemical stability, which would allow to realize HEMT devices able to operate at temperature regimes beyond the limits of conventional electronics and robust enough for withstanding a diamond overgrowth process.

Exploiting such a feature, in 2006 Medjdoub *et al.* were the first to demonstrate GaN devices with InAlN barrier feasible to operate for a short time at 1000 °C in vacuum [35]. However, heterostructure stability alone is not sufficient to enable prolonged FET operation at such high temperatures, which indeed impose a high thermal budget on the whole HEMT device, including contacts metallization and device passivation.

The approach adopted by Maier and coworkers in [73] to evaluate and improve the thermal stability of each HEMT component relies heavily on storage and operation tests of HEMTs at high temperature (up to 1000 °C), whereby the possible failure mechanisms occurring in the device in such extreme conditions could be identified.

For instance, Figure 2.7 shows the DC output characteristics of InAlN/GaN HEMTs with barrier of two different thicknesses (3 and 15 nm), passivated by PECVD-SiN, before and after storage for 30 minutes at 1000 °C in vacuum [73]. In the test, the temperature was increased stepwise from 500 to 1000 °C in steps of 100 °C, with each step lasting 30 minutes.



(a) 15 nm (b) 3 nm (c) gate

Figure 2.7: DC output characteristics of PECVD-SiN passivated lm-InAlN/GaN HEMTs before and after 30 min. stress at 1000 °C in vacuum for (a) a 15 nm barrier (b) 3 nm barrier and (c) gate diode characteristics of the 3 nm barrier HEMT before and after the stress test (from [73]).

It can be seen that the device characteristics are largely unchanged for both the devices, with a slight decrease in the access resistance for the HEMT with 3 nm barrier due to changes in the alloy of the ohmic contacts. Also the gate diode characteristics are identical and no shift in the pinch-off voltage could be observed.

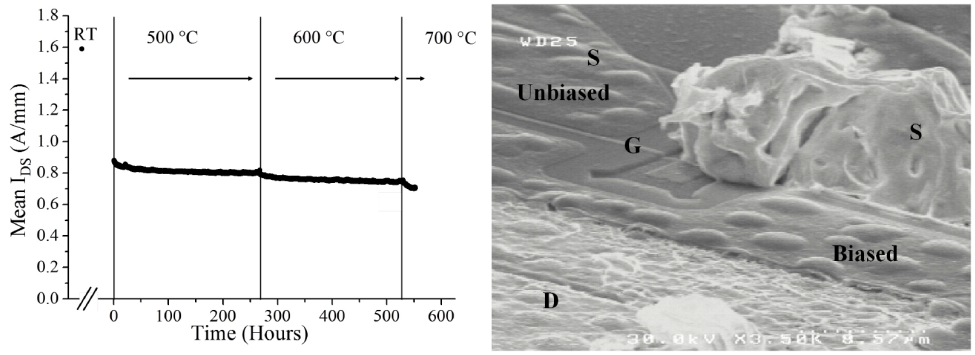
These results indicate that the basic properties of the InAlN/GaN heterostructure, namely the polarization and the barrier thickness, are preserved after the temperature cycles. Therefore, since the heterostructure can withstand temperatures up to 1000 °C for prolonged times under vacuum conditions, any degradation occurring in the HEMT characteristics induced by a high thermal stress is more likely due to either degraded contact metallization or degraded passivation or both.

To verify this assumption, large signal (1 MHz) operation tests at high temperature were conducted. The mean current density measured on a HEMT with 10 nm barrier during such a test [73] is plotted in Figure 2.8a. It shows that the HEMT was able to operate for 250 hours at both 500 and 600 °C without suffering from any degradation in the DC characteristics, but was damaged after 25 hours at 700 °C.

The disruptive breakdown of the metallization (see Figure 2.8b), which caused the sudden failure of the device after several hours at 700 °C was ascribed to an electromigration effect. Those metals, which became soft at high temperature can move on the device surface under the effect of a high electric field, hence short circuiting source, drain and gate contacts. Indeed no degradation occurred to the unbiased finger of the same device (right side in the picture), which could be operated normally after cooling down to RT.

Gold, included in the metal stack for the ohmics and gate contacts, is particularly prone to electromigration effects due to its high ductility. In fact, as HR-TEM analysis[1] of the ohmic contacts after a storage test at 800 °C shows (see Figure 2.9), Au does

1 performed at the department of Electron Microscopy, Ulm.



(a) (b)

Figure 2.8: (a) Long time operation test of 10 nm InAlN/GaN HEMT. The HEMT operated for 250 hours at 500 and 600 °C, and 25 hours at 700 °C before failure. (b) The sudden HEMT failure is due to metallization meltdown, leading to short circuit between source and drain. The unbiased devices were not damaged (from [73]).

not alloy uniformly, but accumulates in clusters, from which it could overflow when heated up at high temperatures.

New metal schemes developed by Maier *et al.* [74, 75] have been designed to address this issue by replacing the Au layer with a less-ductile metal with high melting temperature, like Cu, Pt or Ta. HEMTs using these alternative metal stacks were able to reach 25 hours of continuous operation at 1000 °C in large signal operation tests, thus representing the first InAlN/GaN-based HEMTs able to operate in such extreme environmental conditions.

As described in details in Section 7.1.2, the outcome of this study has been crucial for the development of diamond-capped HEMTs, whose contact metallization must be Au-free in order to be stable during diamond deposition at temperatures above 650 °C.

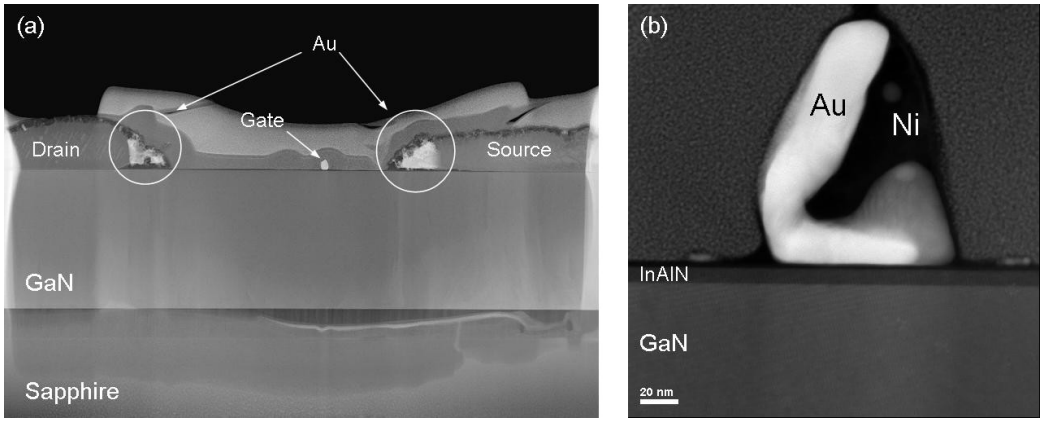
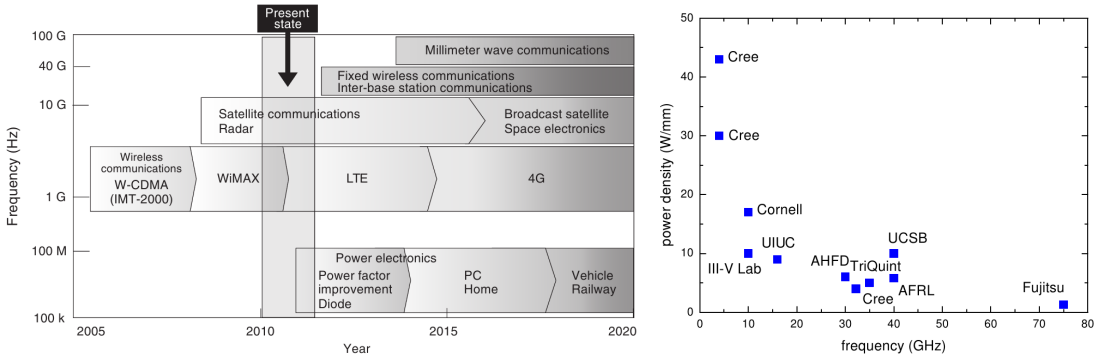


Figure 2.9: TEM cross section of the MOSHEMT after thermal stress at 800 °C for 30 min. The segregation and flow of Au is visible in both the ohmic (a) and gate contacts (b).

2.5 APPLICATIONS AND THERMAL ISSUES

The static and dynamic performances described in the previous sections clearly show the capability of GaN-based HEMT devices to operate at high power regimes in a wide spectrum of frequencies and environmental conditions.



(a) (b)

Figure 2.10: (a) Roadmap of the market for GaN-HEMT-based devices for respective frequencies from [76]. (b) Summary of state-of-the-art RF power performances for GaN-based HEMTs (data from [77, 6, 72, 78]).

According to their design, GaN-based HEMTs may find application in the high-voltage and in the high-frequency branches of power electronics (see Figure 2.10a). High voltage switches for power conversion purposes operate today in the low frequency range (up to 1 MHz), with voltages as high as 10 kV [79, 80]. High frequency power amplifiers instead, cover the microwave frequency spectrum (300 MHz–300 GHz), domain of wireless communications (low range ~ 1 GHz) and radar applications (mid/high range up to 100 GHz). For both these branches the advantages of GaN as wide bandgap semiconductor enable to operate at higher voltages with lower on-resistances compared to equivalent devices based on Si and GaAs technology, thus combining high power and high efficiency.

In Figure 2.10b the RF power performances for state-of-the-art GaN-based devices from [77, 6, 72, 78] are plotted as a function of frequency. It can be seen that extremely high power densities have been achieved, especially in the low frequency range. Densities around 10 W/mm are typical for GaN-based HEMTs without additional measures at the gate, while figures exceeding 40 W/mm have been reported using field plates and multi-fingers configurations [6].

With a multi-finger layout the very large gate peripheries required by high-power applications can be realized in a small chip area, hence reducing the footprint on the die and leading to the high level of integration seen in monolithic microwave integrated circuits (*MMICs*). The core of a *MMIC* amplifier is the so-called powerbar, which is an interdigital device structure consisting of several power devices in parallel, each representing a unit cell. For a given substrate material and thickness, the powerbar has two main design parameters, namely unit gate-width and gate-pitch (i. e. gate-to-gate spacing), which need to be optimized as a function of frequency in respect to power gain and thermal resistance. Shown in Figure 2.11 is a MMIC power

amplifier based on the InAlN/GaN on SiC heterostructure and arranged according to a powerbar layout (5 mm long) with 90 fingers[2].

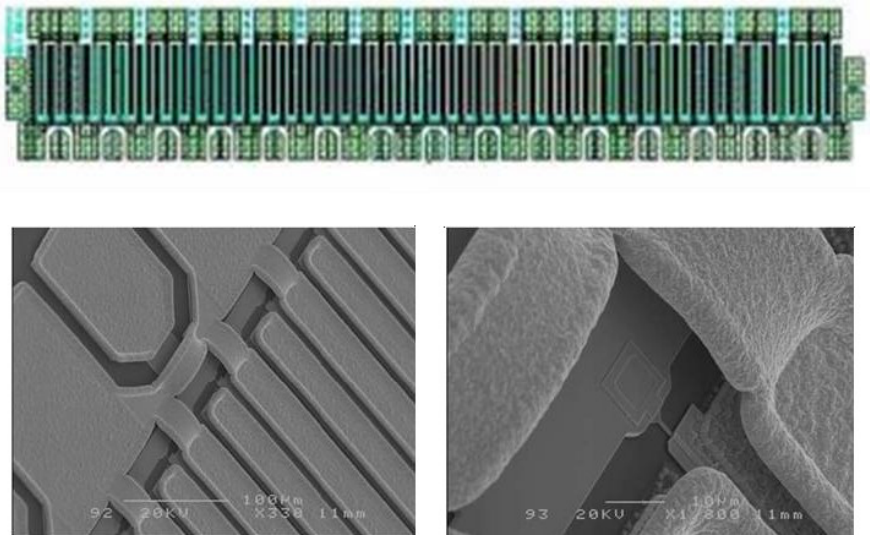


Figure 2.11: (top) Layout of a InAlN/GaN-based MMIC power amplifier with 5 mm wide powerbar consisting of 90 fingers; (bottom) electron micrographs showing the multi-finger structure, with detail of the air bridge (courtesy of S. Delage, Thales III-V Lab).

Although small unit gate-width and short gate-pitch are required for high gain, decreasing the size of the unit cell always comes at the cost of increased power density levels and thermal resistances, which in turn result in significant Joule heat generation in the active area, an effect commonly referred to as *self-heating*. Since self-heating is detrimental for performance stability and device reliability [81, 82, 83], GaN HEMTs employed in realistic (i. e. commercial) power amplifiers are typically limited to power densities below 10 W/mm [84], either by operating them at moderate bias levels or by increasing the gate pitch. For instance, the current line (as of 2014) of Cree's GaN RF amplifiers on SiC features devices which do not exceed 8 W/mm [85]. Such a limitation is largely due to the difficulties of thermally managing the large local heat fluxes that are created in the near junction region of these devices, with fluxes well above $2\,kW/cm^2$ [86].

The development of innovative thermal management solutions able to meet such challenging requirements is therefore crucial to realize the promise of high power, high frequency and high efficiency power devices achievable with GaN-based materials.

2 courtesy of S. Delage, Thales III-V Lab; device realized in the framework of the EU Project MorGaN.

3

DEVICE SELF-HEATING

The term *self-heating* refers to a temperature increase in a transistor device induced by hot carriers (i. e. carriers with high energy) transferring a large amount of their energy to the lattice while traveling in the channel [87].

Although most of the results discussed in this chapter were obtained on AlGaN/-GaN HEMTs, which are more mature and widespread than the InAlN/GaN-based counterparts, the physics behind the self-heating effect, as well as the experimental methods used to characterize it and the solutions currently adopted to mitigate it apply to all GaN-based HEMT devices.

3.1 ORIGIN OF SELF-HEATING IN GAN HEMTS

At the high electric fields present in a GaN channel, the electrons are displaced from equilibrium and become hot, with a peak temperature proportional to the applied power [88, 89, 90]. These electrons tend to lose their excess energy mainly through interaction with longitudinal optical (LO) phonons, because the coupling between electron-LO-phonon is strong in highly ionic materials such as GaN.

However, it is highly likely that the LO-phonons remain then mostly confined in the channel due to their very low group velocity. In fact, the LO-mode vibration cannot be dissipated or removed from the channel unless the non-equilibrium LO phonons are converted to other phonon modes with higher group velocities, e. g. longitudinal acoustic (LA) and transverse optical (TO) modes. In GaN such a conversion takes place through the route $LO \rightarrow LA + TO$ after a characteristic LO-phonon lifetime τ_{LO} has elapsed (see Figure 3.1 and ref. [91]).

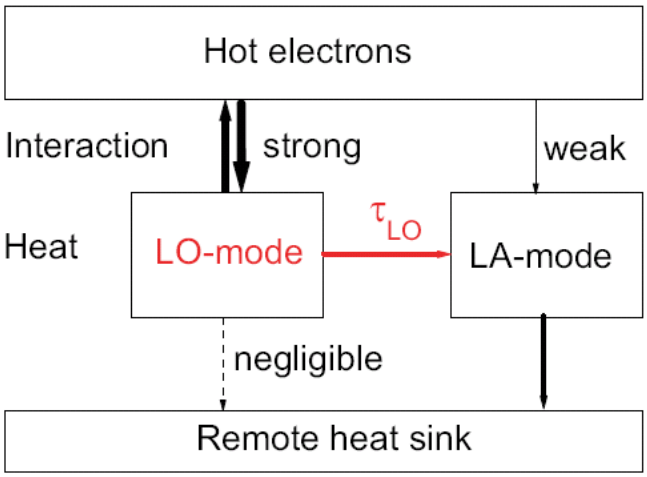


Figure 3.1: Schematic routes for heat dissipation in a GaN channel. Hot electrons primarily lose their energy through interactions with LO phonons. These in turn decay into LA modes before the heat is removed from the channel (from [92]).

Since in the GaN 2DEG channel the hot-phonon lifetime (~ 350 fs) is much longer than the time for spontaneous LO-phonon emission (10 fs) [93], when the hot phonons are unable to escape quickly enough from the active region of the device they accumulate in the channel, thus raising its temperature (*self-heating* effect) and causing additional scattering of electrons.

Self-heating is more important in GaN than GaAs because the 2DEG sheet carrier concentration in GaN ($10^{13}\,cm^{-2}$) is an order of magnitude larger than in GaAs ($2 \cdot 10^{12}\,cm^{-2}$). Additionally, hot electrons are generated 12 times more frequently in GaN than in GaAs [94].

3.2 IMPACT OF SELF-HEATING ON DEVICE PERFORMANCE

In a GaN HEMT, the reduction of carrier mobility (μ) in response to an increasingly higher channel temperature leads to a higher source resistance, which in turn results in lower source-drain current at the identical voltage (for long gates I_{DS} is in fact proportional to the product $\mu \cdot W_g/L_g$, where W_g and L_g are gate width and gate length respectively).

This current droop is clearly visible in the DC characteristics of GaN-based HEMTs when the GaN is grown on a substrate with low thermal conductivity (e. g. sapphire) and the device is biased at high voltages [95]. For instance, Figure 3.2 from [96] shows the I-V characteristics of an 8-finger InAlN/GaN HFET with a total gatewidth of 600 μm and a gate length of 0.25 μm measured under DC and pulsed wave (PW) bias conditions (pulse width of 600 ns, duty cycle of 0.5%). Under DC mode of operation at

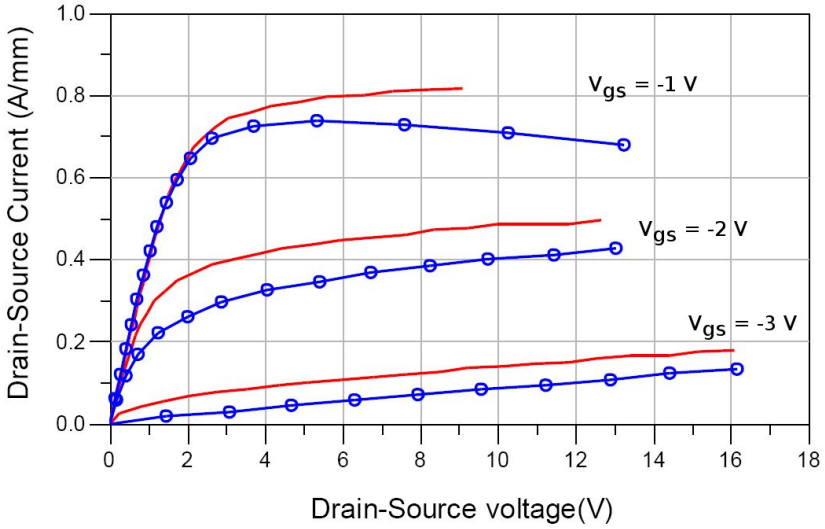


Figure 3.2: Self-heating effect on the DC characteristic of a InAlN/GaN HFET operated under continuous mode (in lines and symbols) and pulsed mode (solid lines), with pulse width of 600 ns and duty cycle of 0.5% (from [96]).

$V_{gs} = -1\,V$, where the dissipated power is the highest, the device exhibits a negative slope in the saturation regime of the $I_{DS}(V_{DS})$ curve, which is absent when the device is operated in pulsed mode and may be ascribed in first approximation (i. e. neglecting any contribution from the trap response time) to a reduction in electrons mobility due to self-heating (as suggested in [82]). A lower mobility reflects in a lower

g_m in continuous wave (CW) operation compared to the pulsed mode, such that the same device achieves lower cutoff frequency and lower gain in CW compared to PW.

This is the reason why GaN-based *MMIC* amplifiers which are able to deliver total output powers of 370 W under CW-operation conditions [97], may reach much higher figures of ~ 1 kW in pulsed-mode with low duty cycles, a condition which mitigates the self-heating effect [98, 6, 99] (see Figure 3.3). To provide a safe margin for reliable

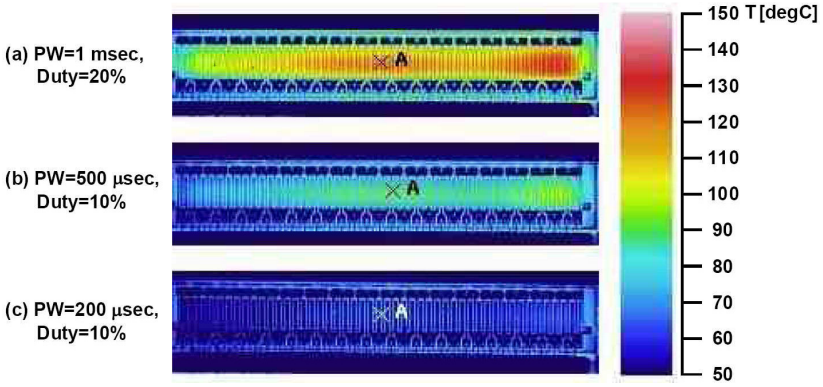
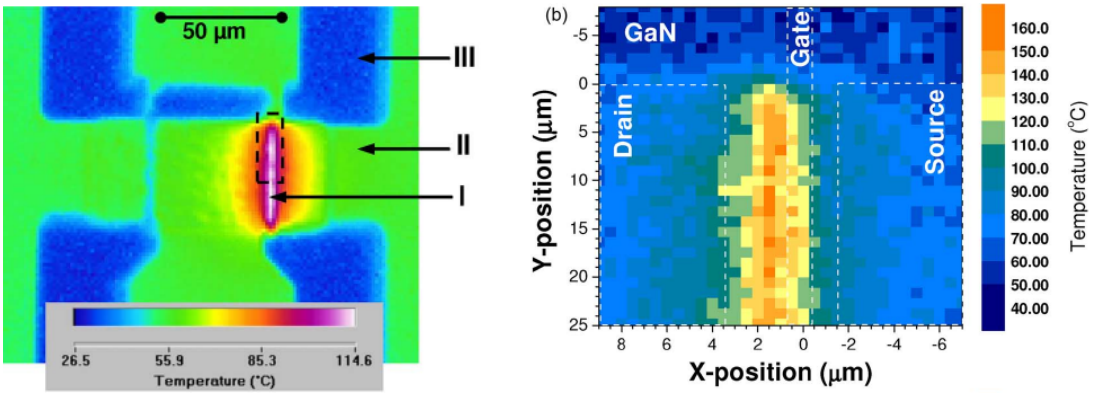


Figure 3.3: IR thermal images of AlGaN/GaN HEMT chip at peak channel temperature with various pulsed operating conditions (f=3.1 GHz, V_{ds}=65 V, P_{out}=58.7 dBm, T_{case}=45 °C (from [99]).

operation, these amplifiers are commonly designed/optimized to operate at relatively low power densities of 3–4 W/mm, rather than at their peak power densities.

In order to measure accurately the temperature in the active area of GaN HEMTs and map the temperature distribution in the channel µ-Raman thermography is widely adopted [9, 100, 101, 102, 103, 104]. Among the techniques available for measuring device temperatures (reviewed by Blackburn in [105]), µ-Raman is the principal optical method, achieving temperature resolution of 5 K and spatial resolution 0.5-0.7 µm, which is suitable to probe the micron-sized source-drain openings typical of most high-power HFETs [100]. In Figure 3.4, Sarua *et al.* [101] used an hybrid IR/Raman



(a) IR (b) Raman

Figure 3.4: (a) IR temperature map of AlGaN/GaN HFET at V_{sd} = 40 V and I = 25 mA. Numbers denote (I) hot spot, (II) area covered by metal contacts, and (III) area free from metal contacts. (b) Raman temperature map of GaN temperature measured over the area depicted by a dashed rectangle in (a) (from [101]).

microprobe system to monitor the temperature reached in an AlGaN/GaN HFET device on SiC substrate with 50 µm gate-length when operated at a source-drain bias of 40 V and current of 25 mA.

As can be seen from the micro-Raman image, the temperature peak clearly occurs at the edge of the gate, on the drain side, with temperatures ranging from 100 °C to 160 °C, while the area underneath the contacts is much cooler, with a temperature of ≈ 90 °C. This temperature peak correlates with the area of maximum field strength and power dissipation [106, 107] and proves that for a GaN-based power transistor, the power is mainly generated in a very small region of the device, typically a 0.5-1 µm area near the gate contact.

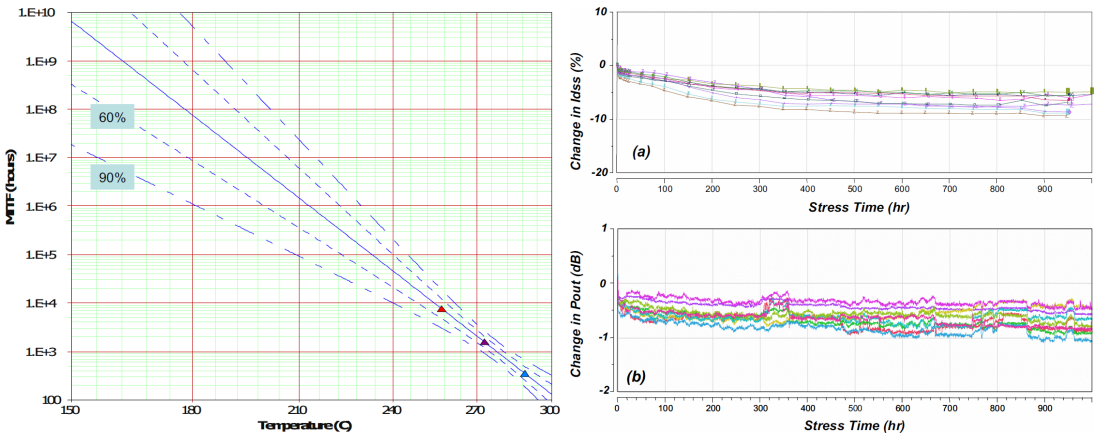
3.3 IMPACT OF SELF-HEATING ON DEVICE RELIABILITY

Besides the detrimental effects on device performances, self-heating may also cause earlier device failures, e. g. by degrading the gate electrode due to accelerated electromigration and thermally-activated chemical reactivity. Furthermore, high operating temperatures due to self-heating are detrimental for the device long-term reliability, as the results of reliability tests conducted by various research groups on GaN HEMTs clearly indicate [10, 108, 109, 110, 83, 111, 112, 78].

DC Arrhenius accelerated-life tests like the one shown in Figure 3.5a, obtained on AlGaN/GaN *MMICs* on SiC [112], are used to predict the mean time to failure (*MTTF*) of FETs. Of critical importance to this type of analysis is the hypothesis that an Arrhenius plot is possible in the first place, and then the confidence interval associated with the estimate. This confidence interval indicates the spread in the *MTTF* over the population of the tested devices. The triangles in the plot show the *MTTF* at junction temperatures of 257, 273 and 289 °C. The dotted lines show the 60% and 90% confidence bounds on the estimate of *MTTF* at any desired channel temperature. For instance, the estimated *MTTF* at 200 °C was between 1.0 $\times 10^6$ and 3.0 $\times 10^7$ hours (considering a 60% confidence interval) and between 2.0 $\times 10^5$ and 1.5$\times 10^8$ hours (for the 90% confidence interval). These results indicate that in order to assure a device lifetime of 10^6 hours, which is considered as the minimum value to enable commercial applications, a channel temperature below 200 °C is strictly necessary.

In Figure 3.5b the impact of DC and RF stress on the device characteristics was evaluated using a 1000 hour stress test conducted at a drain bias of 48V and a power dissipation of 3.36 W/mm, at a base temperature of 170 °C. In such a test the average degradation of the channel current I_{dss} after 1000 hours of DC stress was of 6.8%, while the average decrease in RF power P_{out} after 1000 hours of RF stress was of 0.74 dB, of which 0.32 dB occurred within the first hour. These results demonstrate the excellent reliability and suitability of GaN based HEMT technology for 48V applications, when the operation temperature does not exceed 200 °C.

Thus, although GaN-based HEMT technology has matured to the point where both performance and reliability have been demonstrated at low power densities, its true potential is still hindered by thermal management solutions unable to handle the much higher power these devices are capable of delivering.



(a) (b)

Figure 3.5: MMIC reliability tests: (a) DC Arrhenius accelerated life test (60% and 90% confidence intervals are indicated) and (b) RF operational life test show that GaN MMICs are stable under realistic operating conditions (from [112]).

3.4 THERMAL MANAGEMENT OF GAN HEMTS

The thermal management of GaN-based power HEMTs is a challenging task due to the the extremely high and highly-localized heat fluxes generated in these devices.

Both these factors rule out the possibility of adopting a conventional packaging design, where soft or hard solders are used to mount the power transistor into a package, which is subsequently attached to a heat sink by means of a thermal grease as an interface material. In this case the total thermal resistance of the thermal path between the HEMT channel, where the heat is generated, and the ultimate heat-sink, where the heat is dissipated, would be indeed too high to prevent self-heating.

It is therefore clear that GaN power HEMTs require a shift in the paradigm of thermal management, since the heat has to be managed firstly at the device level, rather than at the packaging level. Furthermore, a thermal path of low thermal resistance has to be provided as close as possible to the channel area, since the thermal properties of the near-junction region have the greatest influence on the channel temperature.

As discussed in the introduction (Chapter 1), both conventional and flip-chip designs have been proposed for self-heating mitigation. The main difference between the two is the location of the heat-sink, which is attached either to the substrate, in a conventional design, or to the top side of the device, in case of a flip-chip design.

In the former case, the heat has to go through the GaN buffer layer and the substrate in order to reach the heat sink, located hundreds of microns apart. Therefore buffer and substrate thermal properties, as well as their thermal interfacial resistance, play a crucial role in the thermal management of the device [113, 114, 115].

For this configuration, growing the GaN heretostructure on a substrate with high thermal conductivity and adopting a thin GaN buffer layer (i. e. < 1 µm) seems the most promising approach to mitigate the self heating effect. For instance Sarua *et al.* [101] reported ~40 °C lower peak channel temperatures – measured on devices with

1.3 µm GaN buffer for the same power density – when the GaN is grown on a SiC substrate instead of sapphire.

To further increase the heat dissipation and power handling capabilities, the SiC substrate can be mechanically thinned down (to ≈50 µm) [116], or the GaN heterostructure can be grown onto single-/poly-crystalline diamond substrates [18, 19, 20, 21, 22, 23], although such a solution requires to overcome challenges related to the deposition of high quality GaN-on-diamond (still in its infancy in respect to GaN-on-SiC). Alternatively, a (poly-crystalline) diamond substrate can be bonded to the GaN buffer layer after removal of the pristine substrate, as proposed by Group4 Labs[1] in [50, 117, 51] and illustrated in Figure 3.6.

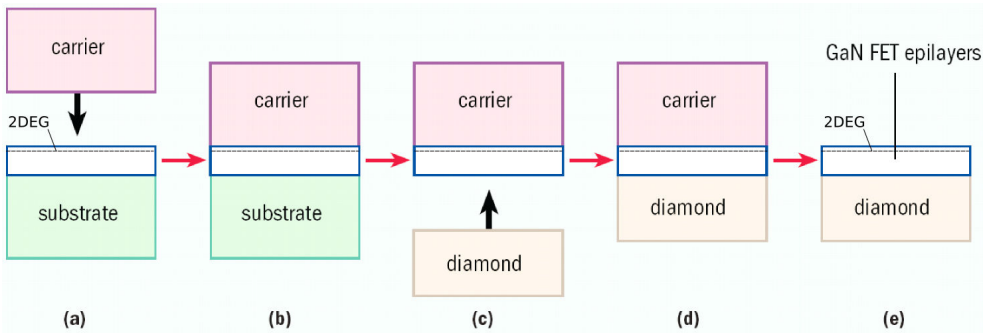


Figure 3.6: Schematic diagram of GaN-on-diamond wafer manufacture (from [50]).

In this case the fabrication starts with the growth of the epilayer on a silicon substrate. After growth, thin dielectric layers are added to protect the GaN surface and enable bonding to a sacrificial substrate, such as silicon (a, b). The original Si substrate is subsequently removed by grinding and a chemical etch that stops on the underlying AlN and GaN layers. The back surface of the GaN epi-wafer is then chemically prepared for CVD diamond attachment (c), which is bonded by means of a proprietary Si-based interlayer. Once the bonding has occurred (d), both the sacrificial carrier and the underlying bonding layer are chemically etched away (e) and the composite wafer is then ready for device processing.

Although AlGaN/GaN HEMTs based on this fabrication scheme have been already demonstrated [51, 118], optimization of the interface material used to bond the GaN epilayer to the diamond substrate is still required [19] in order to improve the thermal efficiency of such an approach over that of conventional GaN-on-SiC devices.

A different thermal configuration is established by a flip-chip design (Figure 3.7). In such a design the HEMT device is flip-chip bonded onto a thermally conductive, electrically insulating carrier, such as aluminum nitride (AlN). AlN is commonly the preferred carrier substrate, because of its high thermal conductivity (270 $Wm^{-1}K^{-1}$) and low substrate loss at RF frequencies. The bonding is done by simultaneously applying heat and pressure to the HEMT and the carrier substrate, on which metal contact pads and Au- or Sn-bumps are previously deposited, followed by a thermal reflow of the solder material. The AlN carrier acts as a heat-spreader, spreading the heat away from the heat source by transferring it to an heat sink.

Such a configuration provides an heat extraction path in close proximity to the heat source, which competes in terms of efficiency with the substrate approach described

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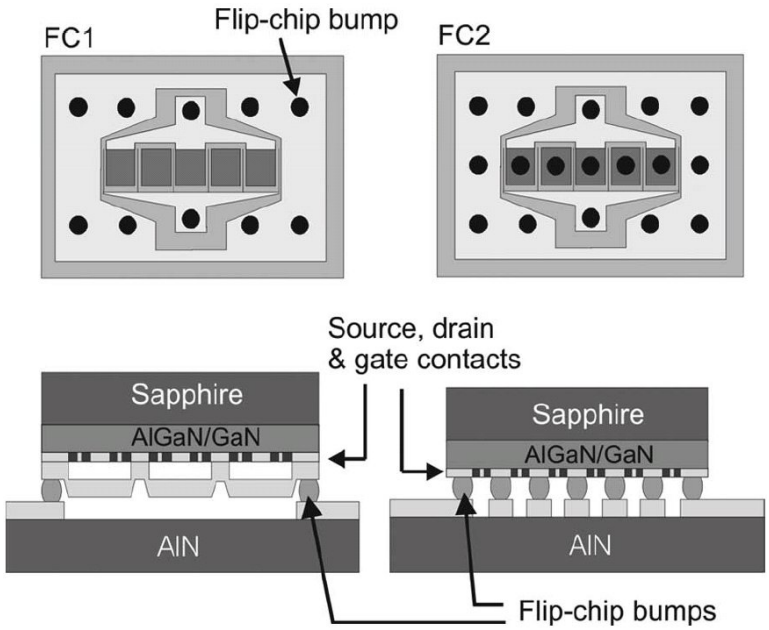


Figure 3.7: Example of two flip-chip designs. In design FC1, bumps are placed on the source, drain, and gate contact pad. In design FC2, additional bumps are placed directly on the source and drain ohmic contacts. In this way, there is direct thermal and electrical contact between the ohmic contacts and the metal pads on the AlN carrier (from [27]).

above. Indeed good results have been achieved even for GaN-on-sapphire, as reported in [26, 28, 119, 68]. However several factors may influence the heat removal efficiency of the carrier. Since the heat has to flow laterally to the metal bumps to be removed, the number and location of the bonding points [27] as well as the material chosen for the filling [28] are both crucial.

A way to improve the flip-chip design by avoiding the need of any bonding process consists in integrating a heat-spreading layer directly onto the HEMT device. This can be achieved either by replacing the SiN device passivation with one which has a higher thermal conductivity (e. g. AlN as in [120]) or by depositing a high thermally conductive, electrically insulating material on top of it.

Nanocrystalline diamond is the ideal candidate for the heat-spreading overlayer, since it combines high thermal conductivity and high electrical resistivity with the possibility of being directly deposited by CVD atop the device passivation, hence lowering the thermal boundary resistance with the HEMT channel in respect to a bonding approach.

In order to evaluate the impact of such a high thermally conductive diamond coating on the working temperature of a GaN HEMT, and to draw a comparison with the conventional (i. e. substrate-side) approach, thermal simulations have been performed, in which the maximum HEMT temperature is calculated as a function of the power loss in the device.

3.5 SIMULATION OF SELF-HEATING EFFECT

Thermal simulations were performed using 2-dimensional finite element analysis (*FEA*). The simulated structure depicted in Figure 3.8 is based on the building blocks of a HEMT, with GaN buffer thickness of 2 µm, 10 nm thick barrier layer, Cu as metallization for ohmics and gate, and 50 nm SiN passivation.

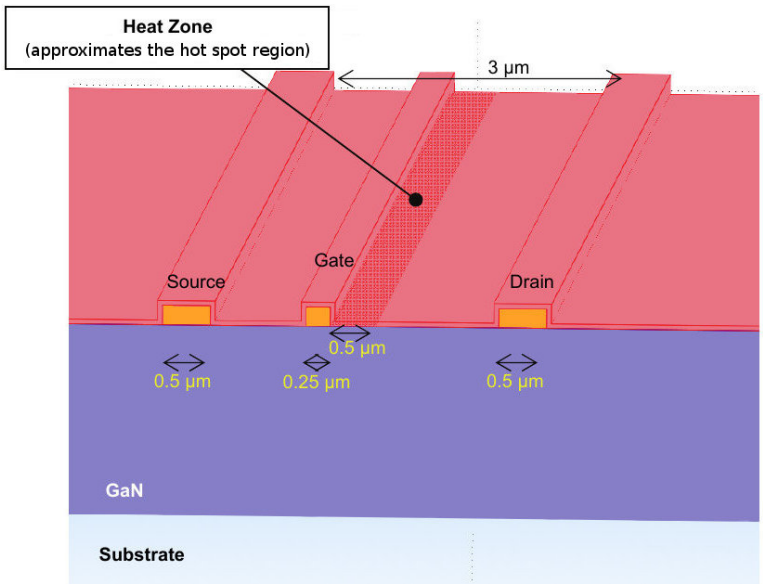


Figure 3.8: GaN HEMT device geometry used in the 2D FEM simulation.

Device self heating is simulated by applying an inward heat flux (in units of W/m^2) across the area highlighted in red in Figure 3.8. This area represents approximately the hot spot region in the channel between gate and drain (0.5 µm long), adjacent to the gate metal contact stripe, where most of the heat is generated, in agreement with the thermal analysis findings (see Fig. 3.4). The heat flux was calculated by dividing an assumed RF power loss, ranging between 1 and 20 W/mm, by the heat zone area. Thus, it is assumed that self-heating accounts for the total power-loss measured during device operation.

Solving the heat diffusion equation, the simulation calculates the peak channel temperature of the HEMT as a function of the power loss for each of the following thermal configurations:

A. bottom heat extraction through a heat-sink attached directly to the HEMT substrate;

B. same as A, but with an additional diamond heat-spreader on top of the device;

C. top heat extraction through a top heat-sink attached to the diamond heat-spreader.

Different substrates were used for bottom heat extraction, namely: sapphire, Si, SiC, polycrystalline and single-crystalline diamond. For case B and C, the diamond is supposed to be nanocrystalline and directly deposited by CVD on top of the device passivation, i. e. with reduced TBR compared to a bonding approach. A thickness of 2

µm was assumed for this *NCD* layer, with a thermal conductivity of 500 $Wm^{-1}K^{-1}$ (1/4 of the ideal diamond thermal conductivity).

Adiabatic boundary conditions were used at all surfaces except at the bottom, when the simulated heat-sink is placed at the substrate side, or at the top, when the simulated heat-sink is placed above the top heat spreading layer. In these two cases the presence of the heat-sink is modeled by applying an isothermal boundary condition, with T = 25 °C. To simulate the thermal resistances at the interfaces at the bottom and top (between the GaN buffer and substrate and between device passivation and the NCD top layer respectively) a thermal resistive layer with thickness 10 nm and $k_{TBR} = 1\ Wm^{-1}K^{-1}$ (and hence TBR of $\simeq 1 \cdot 10^{-8}\ m^2K/W$) was included in the model.

Table 3.1 lists relevant geometrical dimensions and thermal properties of the materials used in the simulation.

Table 3.1: Material properties used in the simulation.

DEVICE MATERIALS	Thickness (µm)	k^* ($Wm^{-1}K^{-1}$)
GaN	2.0	$130 \cdot (300\,K/T)^{1.4}$
Metallization	0.2	340
SiN passivation	0.05	15
SUBSTRATES		
sapphire	300	$40 \cdot (300\,K/T)$
Si	300	$150 \cdot (300\,K/T)^{1.2}$
SiC	300	$340 \cdot (300\,K/T)$
poly-diamond	300	1000
single-crystal diamond	300	2000
TOP HEAT-SPREADER		
nanocrystalline diamond	2.0	500

* temperature dependence according to [121].

CONFIGURATION A. *(bottom heat-sink, no heat-spreader on the top)*

As can be seen in Figure 3.9a, where the peak channel temperature is plotted as a function of the device power loss, for this kind of thermal configuration the substrate on which the heterostructure is grown has a large influence on the maximum temperature reached by the device. In fact, a substrate with high thermal conductivity yields a higher thermal dissipation efficiency, the most efficient configuration being a single crystalline diamond substrate. However, among the high thermally conductive substrates, there is little advantage in growing GaN on diamond instead of GaN-on-SiC. For instance, the device temperature will reach 200 °C at a power loss of approximately 11 W/mm using single crystalline diamond compared to the 9 W/mm when using SiC.

Similar simulation work performed by Nochetto and coworkers in [113, 122] indicates that to fully exploit the heat conduction properties of a diamond substrate thin GaN buffer layers (i. e. < 1 µm) have to be used and low *TBR* between GaN/diamond substrate need to be achieved.

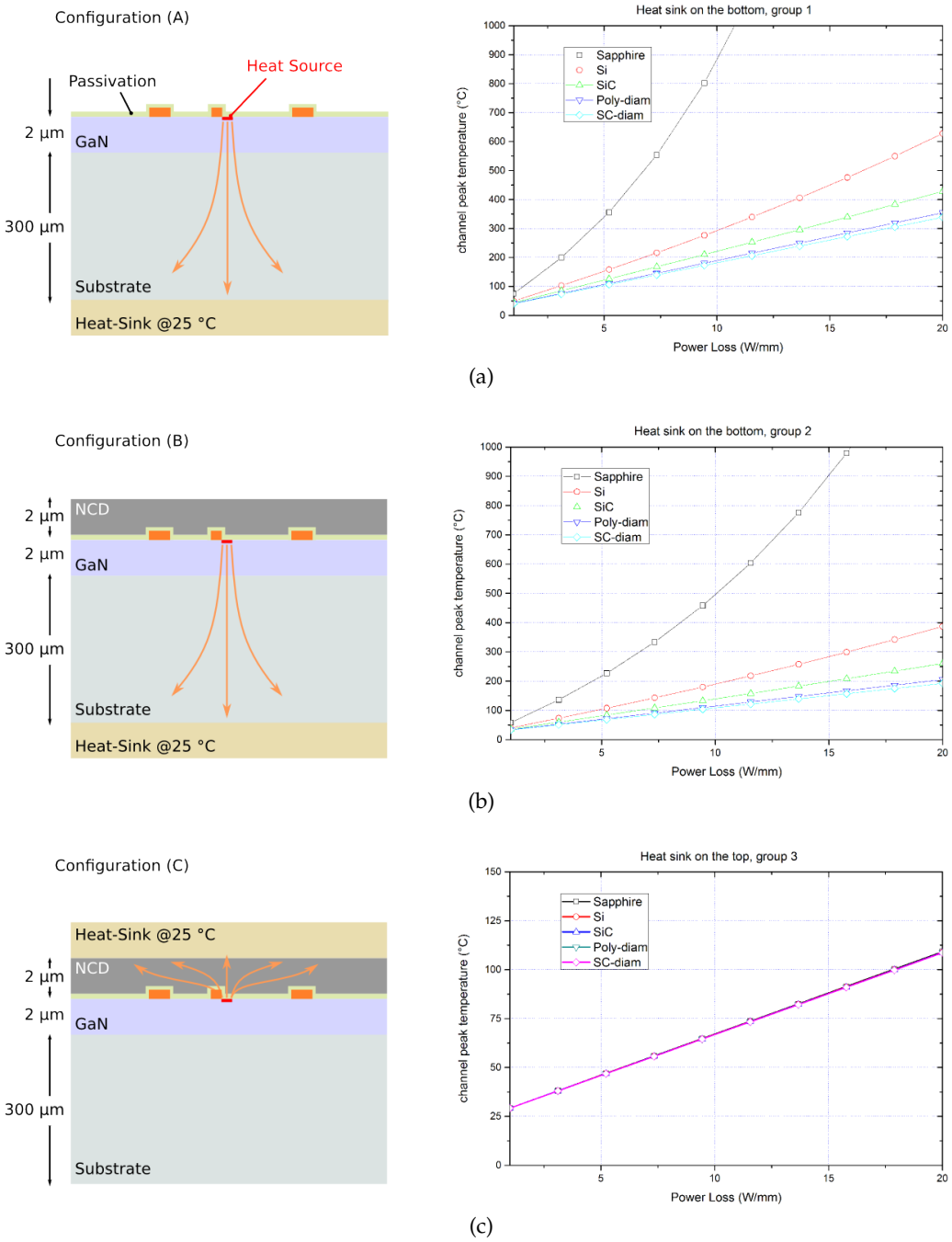


Figure 3.9: (a) HEMT maximum channel temperature as a function of power loss for a bottom heat spreader and heat sink and (b) bottom heat spreader and heat sink but with a 2 µm NCD layer on top. (c) HEMT maximum channel temperature as a function of power loss, using a 2 µm NCD heat spreading layer with an attached heat sink on top. The temperature of the device is independent of the substrate type.

CONFIGURATION B. *(bottom heat-sink, NCD heat-spreader on the top)*

A slight reduction in the maximum temperature of the device can be achieved by adding a top diamond heat-spreader, as shown in Fig. 3.9b. In this configuration, when using a SiC substrate a maximum device temperature of 200 °C is now reached at a power loss of approximately 15 W/mm.

However, the heat dissipation is still a strong function of substrate's thermal properties. In fact, albeit the diamond layer on top of the device removes the heat from the channel by spreading it over a larger area, once it reaches the top surface it can then hardly be removed by the atmosphere (by convection) due to the absence of any heat-sink.

CONFIGURATION C. *(top heat-sink, NCD heat-spreader on the top)*

This configuration is representative of a flip-chip layout, in which a diamond heat spreader deposited on top of device passivation transfers the heat to a heat sink located on the top of the device structure. Fig. 3.9c shows that in this case the device temperature is only marginally influenced by the GaN buffer and is essentially independent of the substrate used.

In this thermal configuration, the key factors for efficient heat extraction are 1. the close proximity of the heat sink to the heat source and 2. the low thermal resistance achievable when the diamond coating acting as heat-spreading layer is deposited by means of a direct-growth method. In fact, despite the assumed thermal conductivity of this thin NCD layer is only 1/4 of the ideal diamond, the device is able to sustain power losses as high as 18 W/mm maintaining the maximum channel temperature below 100 °C. Such a figure represents a significant improvement over a conventional, bottom heat-extraction solution.

In conclusion, the simulation results here presented indicate that a top heat-extraction thermal path established by means of a *NCD* coating with top heat-sink could significantly mitigate self-heating in GaN-based HEMTs, independently of the substrate on which the heterostructure is grown, and at power densities well above 10 W/mm. However, the practical realization of such an approach relies in the integration of two elements, namely 1. a diamond-coated HEMT and 2. a heat-sink attached to the diamond surface and kept at a constant temperature of 25 °C.

While this work focuses on the fabrication of diamond-coated HEMTs, also the realization of a heat-sink, which is integrated with the diamond overlay with minimal thermal interface resistance, and which is able to manage the high heat flux density above $5\,kW/cm^2$ generated in the HEMT requires novel cooling concepts beyond conventional cooling solutions [52].

3.6 TOWARDS DIAMOND-COATED HEMTS

Implementing the promising top heat-extraction approach requires to address several challenges, the most important of which is to realize a fully functional, diamond-coated GaN HEMT. As it will be described in Chapter 4, the conditions in which diamond CVD is performed are very harsh for any kind of electronic device, due to the direct contact with a plasma rich of hydrogen radicals, the high temperatures

above 650 °C and the long deposition time, whose combined effect may severely damage the HEMT.

It is noteworthy that the high deposition temperatures are necessary for the film to be high thermally conductive, even at small thicknesses, despite its nanocrystalline micro-structure. As explained in Chapters 5 and 6, the heat conduction properties of a CVD diamond film are indeed strongly dependent on its micro-structure and phase purity, which are in turn a function of the deposition parameters, such as gas precursors concentration and deposition temperature. In addition, the diamond film has to be directly grown on the device passivation to achieve the lowest possible *TBR* with the heat source in the channel.

As a consequence, the HEMT must be designed from the bottom up to be stable in such extreme environment, if it has to be coated with CVD diamond. In fact, all the HEMT components (i. e. GaN buffer, heterostructure, metallizations and passivation) must withstand the harsh conditions and the high thermal budget imposed by the diamond coating process. For instance, depositing 1 µm of NCD requires to expose the device to a plasma rich of hydrogen radicals at temperatures above 650 °C for at least one hour (which may reach 10 hours, depending on the CVD reactor used and the crystalline quality of the film).

Once these challenges have been addressed and GaN HEMTs are successfully coated with diamond, it is important then to evaluate the thermal benefits of such a coating. To this scope, firstly, the thermal properties of the diamond film have to be accurately measured to ascertain the heat-spreading capabilities of this layer. Second, the coated HEMT must be bonded to a heat sink to be characterized both electrically and thermally. Due to the intrinsic anisotropy of nanocrystalline diamond thin films, the first task requires extremely sensitive characterization techniques and dedicated test structures in order to be accomplished. The second task requires to insert the HEMT into a packaging designed to exploit the improved top heat-spreading properties of the device.

In this work, the design optimization undergone by InAlN/GaN-based HEMTs in order to achieve fully functional, diamond-coated HEMTs will be discussed in details in Chapter 7. The lattice-matched InAlN/GaN heterostructure has been chosen rather than the more common AlGaN/GaN, since the former exhibited exceptional thermal stability, as discussed above, hence representing an ideal test-base for the diamond overgrowth experiments. Nevertheless, this choice does not affect the generality of the experimental strategies developed in this work (in fact a similar approach can be found also in the work of Tadjer and coworkers on coating AlGaN/GaN HEMTs [123, 32]). As already anticipated in Section 2.4.3, it will be shown that besides the heterostructure itself, the metals forming the contact metallization stack as well as the dielectric used as device passivation are crucial to assure the thermal stability of the HEMT during the diamond coating process.

Initial results on the thermal characterization of the NCD coating presented in Chapter 8 will show that high thermal conductivities may be reached already in sub-µm thick films. But they will also point out that the effectiveness of the heat spreading in the top NCD coating strongly depends on the thermal properties of the NCD film region spanning the first hundreds of nanometers from the interface with the HEMT.

4

DIAMOND CVD

4.1 STRUCTURE AND PROPERTIES OF DIAMOND

Diamond is an allotropic form of carbon in which each carbon atom has a tetrahedral configuration consisting of four sp^3 hybrid atomic orbitals. Each carbon atom is bonded to other four by σ bonds set at an angle of 109° to each other. The resulting crystal lattice is face centered cubic (see Figure 4.1), with bond length of 0.154 nm and lattice constant a of 0.356 nm.

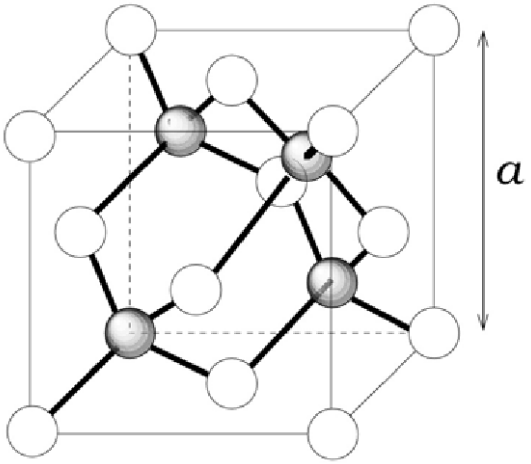


Figure 4.1: Atomic positions in the diamond lattice (zincblende structure), shown in the conventional cubic unit cell of size a.

By virtue of its very strong chemical bonding, the structure of diamond leads to outstanding material properties (see Table 4.1) which promoted its use in a wide range of applications. Interesting for mechanical applications are its hardness and elastic module, whose values are among the highest of all known materials.

Due to its wide, indirect energy bandgap of 5.45 eV, diamond belongs to the class of the wide bandgap semiconductors. The undoped material exhibits resistivity up to $10^{15}\ \Omega \cdot cm$, high breakdown electric field of 10 MV/cm and high carrier mobilities of 4500 (for electrons) and 3800 cm^2/Vs (for holes), all of which are very appealing for electronic applications. The wide bandgap results also in high transparency within a broad range of wavelengths, from UV to IR, hence its high transmittance in the whole visible range.

Moreover, its chemical inertness, combined with the possibility of modifying its surface termination (e. g. fluorine, hydrogen, oxygen and nitrogen) and biocompatibility make it suitable for electrochemical and biological applications.

As discussed in the previous chapters, diamond unmatched thermal conductivity is very attractive for thermal management applications (e. g. for nitride-based HEMTs), hence spurring intense research aiming at finding innovative ways to exploit it.

Table 4.1: Diamond properties compared to Si and GaN (after [42, 124]).

	Si	GaN	diamond
bandgap (eV)	1.12	3.4	5.45
lattice constant (nm)	0.543	0.319	0.36
ϵ_r	11.8	9.5	5.7
thermal conductivity ($Wm^{-1}K^{-1}$)	150	130	2200
μ_e (cm^2/Vs)	1400	1200	4500*
μ_h (cm^2/Vs)	450-600	850	3800*
$v_{sat,e}$ ($\times 10^7$ cm/s)	1.0	2.5	1.6
$v_{sat,h}$ ($\times 10^7$ cm/s)	0.6	2.0	1.1
breakdown strength (MV/cm)	0.3	2.5	~10
Young modulus (GPa)	110	200-400	1140

* from time of flight experiments in ultraclean material.

Apart from the mono-crystalline phase, poly-crystalline forms of diamond can be synthesized by CVD, whose properties may differ significantly from the single crystal material. In polycrystalline diamond (*PCD*) films the diamond crystals are embedded into a grain boundary matrix, which may contain non-diamond carbon phases (i.e. non-sp^3 phases) such as graphite and amorphous carbon. Therefore *PCD* properties are a combination of the diamond grain properties and of the grain boundaries ones, with strong dependence on the size, shape and arrangement of the diamond crystals, besides size and composition of the grain boundaries.

Indeed the class of PCD embraces a wide range of materials, commonly classified according to the size of their grains d into microcrystalline diamond (*MCD*), when $d > 1\mu m$, nanocrystalline diamond (*NCD*), when $0.05 < d < 1\mu m$, and ultra nanocrystalline diamond (*UNCD*), when d is in the nanometers range.

From the electrical point of view, undoped MCD and NCD can show either insulating or conductive behavior according to the size of the grain boundaries. In general, electrical conductivity in both materials is caused by the grain boundary network; depending on the relative size of diamond grains and of grain boundaries, the insulating behavior of diamond may dominate over the conductive one of the grain boundaries, or vice versa. In UNCD, diamond grains of $\approx 3-5\,nm$ are surrounded by a wide network of grain boundaries containing graphitic phases (π-bonds). Therefore, although the small diamond grains are undoped, UNCD can exhibit low resistivity because the wide grain boundaries form a path for metallic (graphitic) conduction through the layer.

The mechanical properties are also influenced by the grain boundaries. For instance, NCD fracture strength is typically half of that of single crystal diamond, namely in the range of 2-5 GPa instead of 10 GPa [125, 126]. On the other hand the Young modulus of NCD may reach values above 1000 GPa, hence approaching the single crystal value of 1143 GPa, as reported in [126, 30].

Concerning diamond thermal properties, as will be discussed in detail in the next chapters, the consequences of the poly-crystalline structure are twofold. On the one

hand, it determines a strong anisotropy in the heat conduction properties, which become dependent on size and shape of the diamond crystals. On the other hand, the grain boundaries are known to have a detrimental effect on the thermal conductivity due to their high content of σ-bonds, defects, impurities and dislocations.

Therefore, although PCD retains only locally the outstanding properties of single crystalline diamond, the flexibility of the former is much higher, allowing thin diamond films to be deposited on a variety of substrate materials and over large areas, thus solving the scarcity and expense limitations of the latter.

4.2 DIAMOND SYNTHESIS

Diamond, together with graphite, is an allotrope of carbon which in nature forms under specific environmental conditions. As shown in the phase diagram of carbon of Figure 4.2, graphite is the thermodynamically stable allotrope of carbon at room temperature and pressure, with diamond becoming the stable configuration only in conditions of sufficiently high pressure and temperature.

Therefore diamond can be synthesized by heating carbon under extreme pressure. In this process, called high-pressure high-temperature (*HPHT*) synthesis, a carbon-rich melt (e. g. C dissolved in a suitable metal catalyst such as Fe, Co or Ni) is compressed in a hydraulic press to tens of thousands of atmospheres, heated to over 2000 K, and left until diamond crystallizes. The diamond crystals produced by this method are single-crystalline and range in size from nanometers to millimeters. Due to their small size, the use of HPHT diamonds is limited to those industrial applications, where hardness and wear resistance properties of diamond are required, e. g. cutting and machining mechanical components, polishing and grinding of optics.

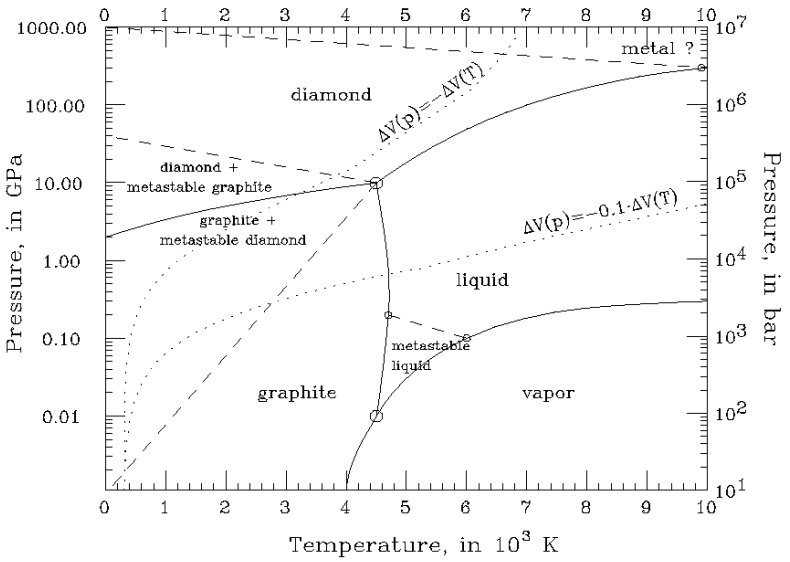


Figure 4.2: Phase diagram of Carbon (as based on [127, 128, 129]).

Rather than duplicating nature's method for creating diamond, the chemical vapor deposition (*CVD*) technique allows to synthesize diamond from carbon-containing gas precursors using H and CH_x (with/out oxygen) as catalysts, at temperatures

between 600 and 1000 °C, but at much lower pressure than in HPHT (see Figure 4.2), with obvious advantages in terms of equipment and energy costs. Discovered in the late 1950's by J. C. Angus [130] and W. Eversole [131] in U.S.A. and by B. Derjaguin [132] in USSR, and later developed in the 1980's in Japan, in the CVD method both diamond and graphite are produced, but graphite is preferentially etched, such that diamond deposition is favored and graphitic clusters not formed and incorporated.

4.3 THE CHEMISTRY OF CVD DIAMOND GROWTH

The CVD method makes use of a carbon containing gas (most commonly methane) and molecular hydrogen, split and ionized by means of an energy source (e. g. hot filament or electric discharge). As illustrated in Figure 4.3, the carbon gas precursor and molecular hydrogen are dissociated passing through the activation region, forming carbon reactive radicals and atomic hydrogen, which drift towards the substrate surface by a gradient in temperature and concentration. The reactive species undergo a complex set of chemical reactions prior to reaching the substrate surface, where they can either adsorb and react with the surface, desorb back into the gas phase, or diffuse until an appropriate reaction site is found. If a surface reaction occurs, carbon is left on the surface, in the form of both diamond and graphite. However, due to the different reaction rate between atomic hydrogen/graphite and atomic hydrogen/diamond, deposition of the diamond phase is favored; in fact, in the right conditions, atomic hydrogen etches graphite at a faster pace than diamond, hence leading to a build-up of diamond. Apart from its role in etching the graphitic sp^2 carbon, atomic hydrogen

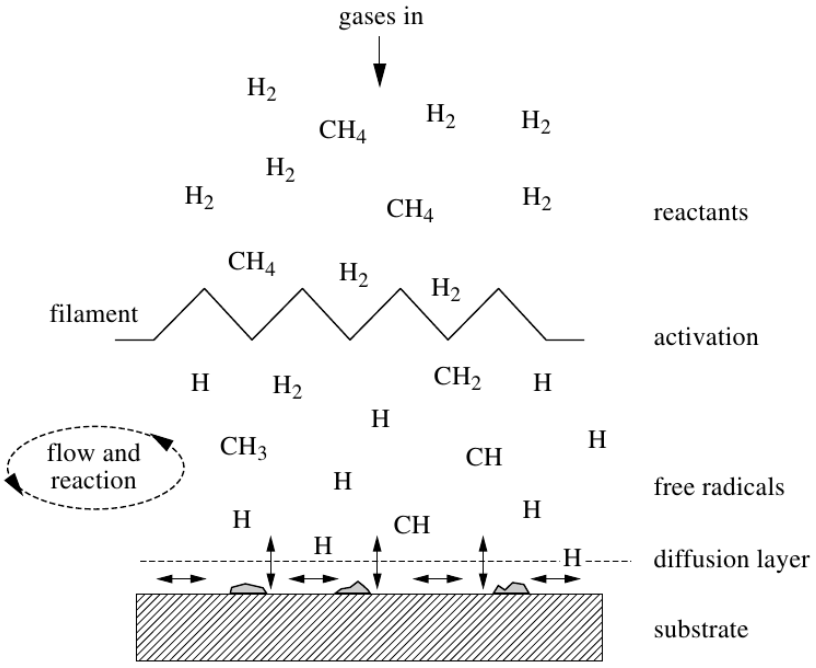


Figure 4.3: Schematic of the physical and chemical processes occurring during diamond CVD (from [133]).

is also responsible for the termination of the surface dangling bonds, thus keeping the sp^3 diamond lattice stable.

Despite the great complexity of the gas phase reactions involved in the CVD process, a first clue on the key principles behind such a process can be gained by means of the C-H-O composition diagram of Figure 4.4, also known as *Bachmann triangle diagram*. Elaborated by Bachmann [134] and based upon over 70 deposition experiments in different reactors and using different process gases, it shows that, independent of deposition system or gas mixture, diamond will grow only when the gas composition is close to the CO line.

Particularly interesting is the small region at the lower left corner of the diagram, along the CH line, representing gas mixtures, where methane is highly diluted in hydrogen and no oxygen is present. This is indeed the most common gas mixture used in CVD diamond growth, comprising solely CH_4 and H_2, with methane/hydrogen ratios usually between 0.1% and 3% according to the activation method adopted and to the kind of *PCD* film one aims to deposit (in respect to crystalline structure and concentration of graphitic phases embedded in the film).

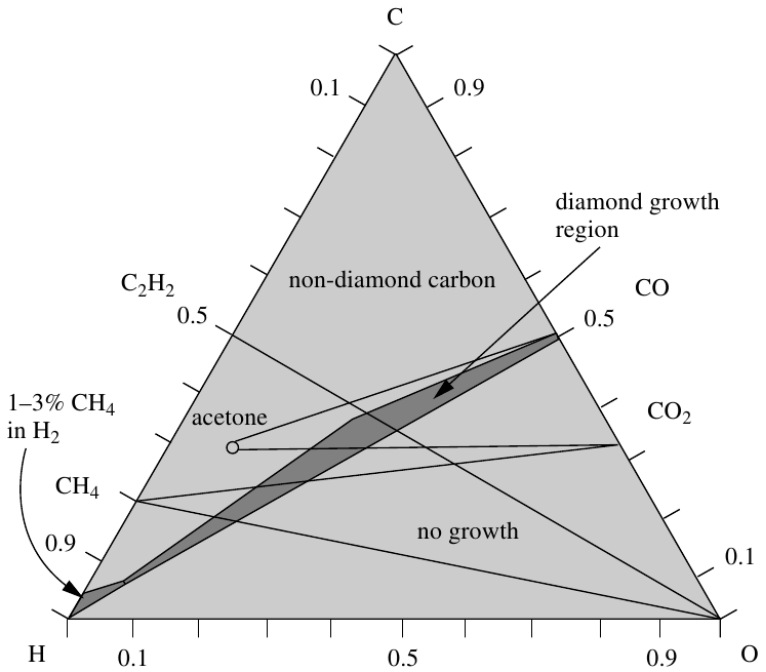


Figure 4.4: Simplified form of the Bachmann triangle C-H-O composition diagram. Most experiments involving a few per cent CH_4 in H_2 are constrained to a small region in the lower left-hand corner (from [133]).

As many studies on the diamond CVD gas chemistry pointed out [135], the fundamental reactions are accredited to involve acetylene C_2H_2 and the methyl radical CH_3 [136], [137], [138] produced in the activation area by the following reactions:

$$CH_4 + H \longleftrightarrow CH_3 + H_2 \tag{4.1}$$

$$2CH_3 \longleftrightarrow C_2H_6 \tag{4.2}$$

$$C_2H_6 + 2H \longleftrightarrow C_2H_4 + 2H_2 \tag{4.3}$$

$$C_2H_4 + 2H \longleftrightarrow C_2H_2 + 2H_2 \tag{4.4}$$

Other methyl groups CH_X and C_XH_Y are also found to have a role in diamond growth [139]. The reactions listed above are promoted from left to right in the

proximity of the activation energy and from right to left on the substrate surface; the left to right reaction is however faster and thus a non-equilibrium is created in the proximity of the substrate surface, where C_2H_2 and CH_3 are not completely converted and tend to precipitate on the substrate.

A simple sketch of the diamond growth process due to CH_3 is shown in Figure 4.5 [133]. Here diamond growth is considered to be a stepwise addition of carbon atoms to the existing diamond lattice by means of CH_3 absorption, catalyzed by the presence of excess atomic H. It is believed that in oxygen-containing systems the OH radical plays a similar role to atomic H.

Diamond deposition is also possible with noble gases in the gas mixture. For instance, the growth of ultra nanocrystalline diamond (*UNCD*) is carried out with a growth chemistry where hydrogen is almost completely replaced by argon [140]. In this case, the film exhibits a fine-grained structure, which is the result of a strong re-nucleation taking place on Ar-generated defects in the film (which act as re-nucleation centers).

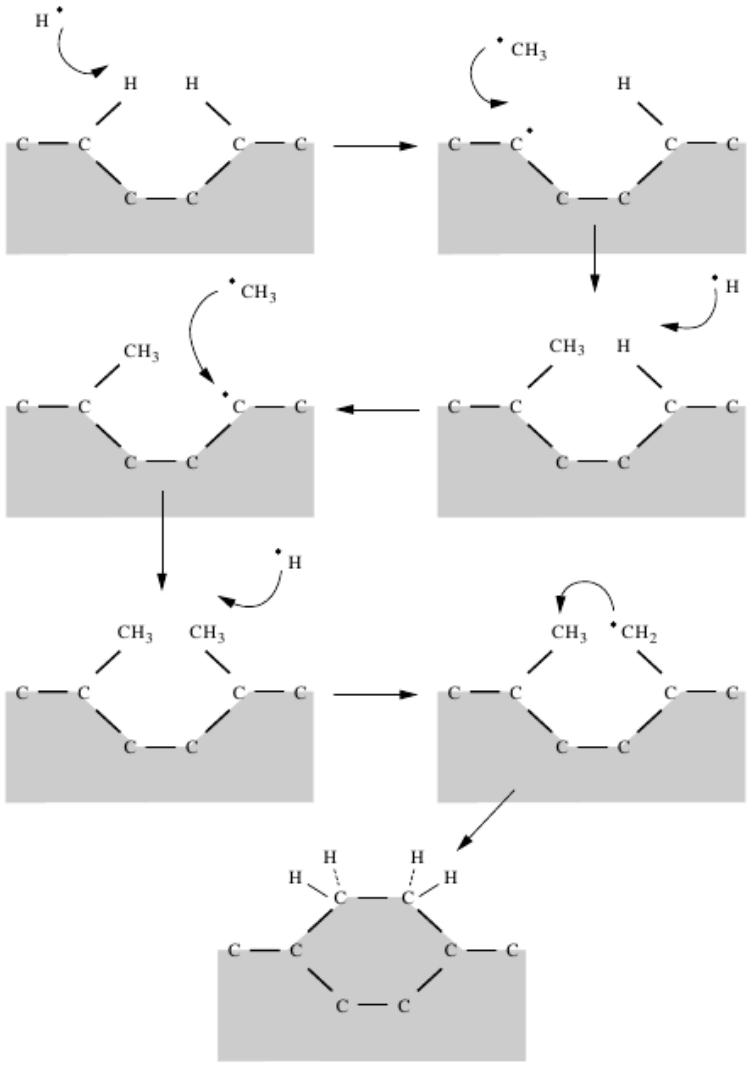


Figure 4.5: Schematic of the reaction process occurring at the diamond surface leading to stepwise addition of CH_3 species and diamond growth. (from [133]).

4.4 SUBSTRATES

CVD diamond can be either grown on HPHT diamond stones or on foreign substrates, among which single-crystal (100) and (111) silicon wafers are the most adopted mainly due to the availability and low cost. The diamond grown by *homo-epitaxial growth* on HPHT stones is single-crystalline, whereas the deposition on foreign substrates (*hetero-epitaxial growth*) generally results in poly-crystalline layers. The hetero-epitaxial growth is usually preceded by a nucleation pre-treatment of the substrate, as described in details in Section 4.5. Despite their small size of approx. 5x5 mm width and 0.5 mm thickness, HPHT diamond stones do not require any specific treatment before CVD growth and are the most suitable substrates to grow single crystal diamond with high purity and low density of defects, crucial properties for diamond in FET applications.

A promising alternative to HPHT stones for large area deposition of single-crystalline diamond is the growth on a thin iridium layer deposited on a foreign substrate, like for instance MgO or sapphire, due to the small lattice mismatch of 7% between diamond and iridium. By using an iridium/yttria-stabilized zirconia (Ir/YSZ) buffer layer, also Si(001) and Si(111) wafers can be used as a substrate [141, 142], hence making such a technique extremely attractive for large area applications of single-crystalline diamond films. Although thermal mismatch problems between the different layers in the stack, namely diamond, iridium and substrate, may be detrimental for the stability of the diamond layer, MESFET devices fabricated on diamond grown on iridium have already been demonstrated [143].

Substrates for the growth of *PCD* do not have the size restrictions of HPHT stones (e. g. diamond grown on 8“ ZnS discs in [144]) and are by no means limited to silicon, although any candidates for diamond growth must satisfy a number of important criteria. One requirement is obvious: the substrate must have a melting point (at the process pressure) higher than the temperature required for diamond growth (normally larger than 700 °C). In order to form adherent films, it is a requirement that the substrate material be capable of forming a carbide layer to a certain extent. This is because diamond CVD on non-diamond substrates usually involves the formation of a thin carbide interfacial layer, upon which the diamond then grows.

Another criterion is that the substrate material should have a thermal expansion coefficient comparable with that of diamond. This is because the substrate tend to expand at the high growth temperatures used, and thus the diamond coating is grown upon an expanded substrate. Upon cooling, the substrate contracts back to its room temperature size, whereas the diamond coating, due to its small thermal expansion coefficient, is relatively unaffected by the temperature change. Therefore the diamond film is subject to compressive stress from the shrinking substrate, with a magnitude proportional to the relative thermal mismatch. High residual stress may lead to cracking, flaking or even delamination of the entire film.

Figure 4.6 shows a theoretical calculation of the built-in stress in the diamond film when grown on Si, sapphire, $SrTiO_3$ and MgO substrates at different deposition temperatures upon cooling down to RT [145]. Diamond films grown on sapphire at 700 °C develop an intrinsic stress of ~4 GPa, a value four times higher than the one of diamond grown on a Si (or SiC) substrate in the same growth conditions. As a consequence, while diamond can be grown on Si and SiC substrates up to

thicknesses of several hundreds microns, diamond on sapphire is normally limited to thin, submicron thick layers.

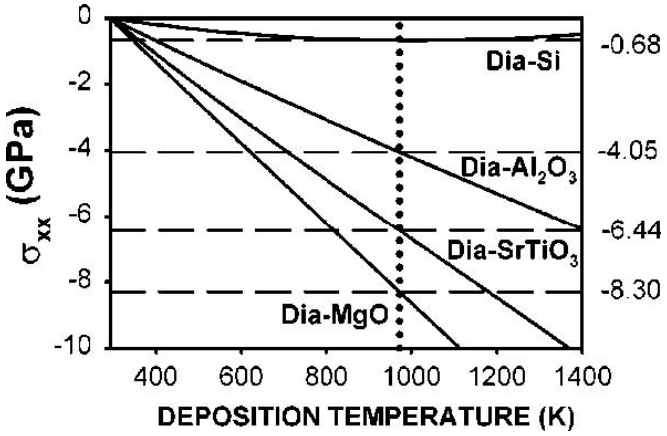


Figure 4.6: Calculated residual stress in the overgrown diamond film on different substrates after cooling down to room temperature. The line and the given values correspond to a diamond growth temperature of 700 °C (from [145]).

4.5 NUCLEATION

Diamond growth on a foreign substrate normally comprises two distinct phases: a nucleation phase, during which diamond crystallites are embedded into the substrate to act as seeds for the subsequent growth cycles, and the actual growth.

Not only the nucleation step is essential for the CVD process, which would otherwise result in the deposition of graphite or amorphous-carbon due to the lack of a proper diamond template, but it also has significant impact on the microstructure of the polycrystalline diamond film, as will be discussed in the next chapters.

Nucleation can be achieved by several methods. When using Si as a substrate, a common technique consists of mechanically scratching the substrate surface with a powder of hard, µm-sized particles like sapphire, SiC or diamond; as the particles scratch the surface they break down into smaller fragments, which stick onto it. Although with such a method high nucleation densities can be reached, the mechanical abrasion may damage the substrate by creating a rough surface with µm-sized pits and defects. This method is therefore unsuitable for those diamond applications in which the substrate surface should be preserved, either because it hosts electronic devices whose circuit geometries are on a sub-micrometer scale, or because a high surface roughness is detrimental for the thermo-mechanical properties of the interface between the diamond film and the substrate.

An alternative, milder technique is the nucleation by seeding with diamond nanoparticles, which due to its ease of use and applicability to various substrates is today the most commonly used method [146, 147]. The nucleation procedure varies according to the carrier, in which the nano-particles are dispersed, which can be either a liquid (water or isopropanol), a gel, or a slurry. In the former case, the substrate is dipped into an ultrasonic bath containing a colloidal solution of nm-sized diamond particles (the smallest measure ~3–5 nm, created by explosive detonation [148]) highly diluted in water. After several minutes of agitation the substrate is then rinsed in

de-ionized water and dried with N2. Gel and slurry instead are normally deposited on the substrate by spin coating.

As reported by Arnault and Williams [149, 150], the nanodiamond seeds left on the substrate surface show excellent stability under diamond growth conditions (i. e. hydrogen plasma at temperatures above 700 °C), thus allowing the subsequent overgrowth. With this technique nucleation densities larger than 10^{11} $nuclei/cm^2$ can be achieved on various substrates (e. g. silicon, quartz) [151]. However, reaching such high densities depends upon several factors, namely the crystallinity, the size of the nanodiamond particles and most importantly the control of their level of dispersion; indeed nanodiamond particles from detonation, which have size of few nanometers, tend to spontaneously aggregate in large clusters with size of 100–200 nm, which would prevent to achieve uniform, high nucleation densities. In addition, diamond layers nucleated in such a way may suffer from poor adhesion with the substrate due to the van der Waals nature of the bond.

Nucleation can also be achieved by promoting the formation of a carbide layer in the topmost few layers of the substrate (e. g. a silicon carbide layer in case of a silicon substrate), upon which the diamond then grows. Besides hosting the first diamond nuclei, such a layer greatly improves the adhesion of the diamond film by partially relieving interfacial stresses caused by lattice mismatch with the substrate.

The bias enhanced nucleation (*BEN*) method is indeed based on this approach, whereby carbon-containing ions present in the CVD reactor are accelerated towards the substrate by a negative potential (typically of 200 V) applied to it at the beginning of the deposition process. These ions sub-implant beneath the substrate surface, hence creating a carbon-rich layer which leads to homogeneous, high nucleation densities of more than 10^{10} diamond $nuclei/cm^2$. The covalent bond established between the diamond nuclei and the substrate atoms has two important consequences: 1) strong mechanical adhesion and enhanced thermal contact between substrate and diamond film can be achieved; 2) on Si and SiC substrates the diamond films can be grown with a preferred orientation, thus called highly-oriented diamond (*HOD*) [152, 153].

Compared to the other nucleation methods the BEN has the disadvantage that the substrate must be conductive in order to be biased, however, insulating substrates can also be nucleated with BEN by means of a thin conductive interlayer, as discussed in section 4.7.1.

4.6 GROWTH

Once individual diamond crystallites have nucleated on the surface, growth proceeds in three dimensions until the crystals coalesce. At this point a continuous film is formed, and the only way growth can proceed is upwards. The resulting film is polycrystalline with many grain boundaries and defects, and exhibits a columnar structure extending upward from the substrate. Furthermore, as the film becomes thicker, the crystal size increases while the number of defects and grain boundaries decreases. This means that the outer layers of thicker films are often of much better quality than the initial nucleating layers. For this reason, if the diamond film is to be used as a heat spreader or optical window (applications where good quality and small number of grain boundaries are paramount), the film is often separated from its substrate and the lower 50–100 μm are removed by mechanical polishing.

The surface morphology of the diamond film obtained during CVD depends critically upon the various process conditions, especially the gas mixing ratio, which determines the value of the α-parameter, as described by Wild and coworkers in [154, 155, 156]. They were the first to systematically investigate the way diamond crystals are arranged in a polycrystalline diamond film and correlate the microstructure which develops with film thickness to the growth parameters. To characterize the outgrowth velocity dependence on the crystal orientation they introduced the α-parameter, defined as the ratio of the growth rates on {100} and {111} faces:

$$\alpha = \sqrt{3}\,\frac{V_{100}}{V_{111}}. \tag{4.5}$$

On the one hand, the value of the α-parameter describes the shape assumed by a single diamond grain (Figure 4.7), as it changes stepwise from cubic (for $\alpha = 1$), to octaedral (for $\alpha = 3$). On the other hand (Figure 4.8), when correlated to methane

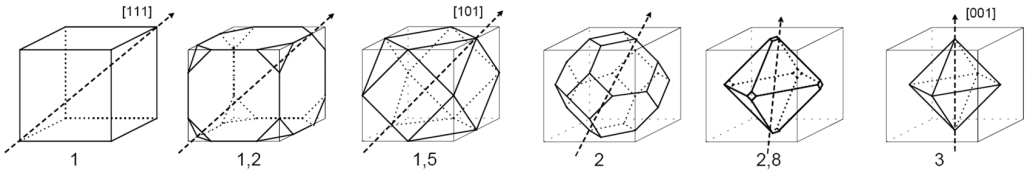


Figure 4.7: Diamond crystal shape for different values of the α-parameter.

concentration and substrate temperature, the α-parameter allows to predict whether the diamond film will develop a 2D/columnar texture (for $\alpha < 1.5$) or a 3D/fine-grained texture (for $\alpha > 3$). From the α-parameter map, low α values, and hence columar-structured films, are obtained when low methane concentrations are used (<0.5% in H_2 for substrate temperatures < 850 °C), while concentrations above ~1.0% in H_2 will yield high α, and thus the resulting film will exhibit a fine-grained texture. With increasing methane concentrations in fact, the crystal size decreases, until above ca. 3% CH_4 in H_2 the crystalline morphology disappears altogether. Such a film is referred to as ultra nanocrystalline diamond (*UNCD*), and may be considered to be an aggregate of diamond nanocrystals and disordered graphite.

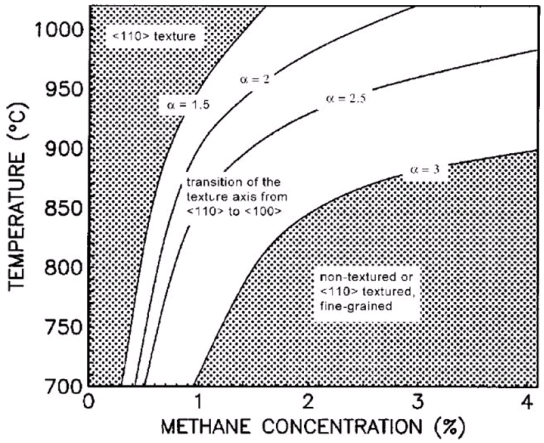


Figure 4.8: α-parameter map as a function of methane concentration and substrate temperature (from [155]).

Although this type of film might be considered inferior to the more crystalline and therefore better quality diamond films, it still possesses many of the desirable properties of diamond, while being much smoother and considerably faster to deposit.

Thus, by the simple expedient of changing the growth conditions, diamond films can be deposited with properties ranging from almost graphitic to essentially those of natural diamond. This allows the quality, appearance and properties of a diamond film, as well as its growth rate and cost, to be tailored to suit particular applications.

4.7 HOT-FILAMENT CVD

All CVD techniques for producing diamond films share a number of common features, i. e. normally the precursor gas (usually CH_4) is diluted in excess of hydrogen, in a typical mixing ratio of 1% vol. CH_4 and the temperature of the substrate is higher than 600 °C to ensure the formation of diamond rather than amorphous carbon.

What differentiates each method from the other is the means of activating gas phase carbon-containing precursor molecules. This activation may be achieved by thermal methods (e. g. a hot filament), electric discharge (e. g. DC, RF or microwave), or a combustion flame.

The hot-filament CVD (*HFCVD*) technique uses a metal filament (or a set of filaments), electrically heated to temperatures in excess of 2100 °C, to produce atomic H from H2 and to break the gas precursors into C_yH_x radicals. The sketch of a HFCVD reactor is presented in Figure 4.9. The process gases are introduced in the chamber at controlled rates (typically a total flow rate of a few hundred sccm), while throttle valves maintain the pressure at typically 1.5–4 kPa (ca. 10–30 Torr).

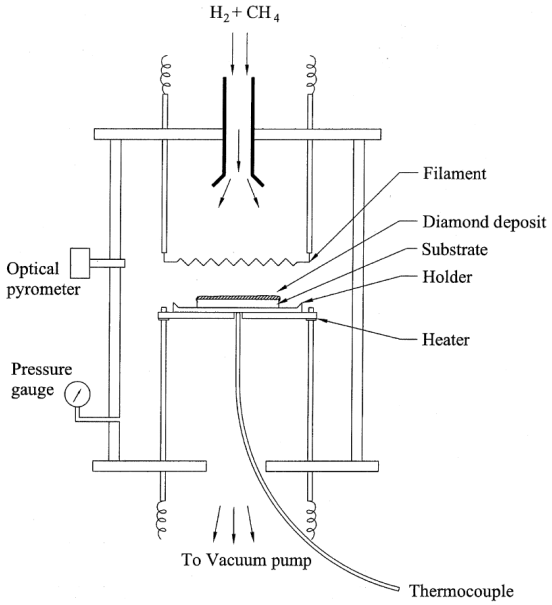


Figure 4.9: Schematic of a hot-filament-assisted CVD diamond growth system ([214], p. 205).

The substrate to be coated is fixed to a holder, located beneath the filament(s) at a distance between few millimeters to some centimeters, which is within the range of the diffusion length of the radicals. The substrate is heated at temperatures between 650 and 900 °C by means of either a separate heater or directly by the filament(s); in

the latter case the substrate heats up due to radiative heat transfer from the filaments and due to convective heat transfer from the gas molecules.

The filaments are made from a metal, which has a melting point higher than 2200–2300 °C, has a low evaporation coefficient and does not react with atomic hydrogen. In addition, the metal has to be carburized during growth to form a metal carbide. The inertness to atomic hydrogen is necessary to avoid hydrogen recombination, while the low evaporation coefficient of the carburized alloy allows to reduce metal contamination of the gas phase during diamond growth.

Metals such as tungsten and tantalum are most often used; the latter has a lower evaporation coefficient and is easier to manipulate in respect to tungsten, which is however cheaper.

It is noteworthy to mention that the filaments undergo a carburization process during the CVD process at high temperatures in presence of carbon, hence promoting diamond formation around each filament. Such a process may induce stress in the filaments, besides it changes their resistivity and makes them brittle, reducing their lifetime and thus the maximum deposition time for a single growth run.

The mechanism of atomic hydrogen formation in the proximity of the filaments can be described as follows:

$$H_2 + z^* \longleftrightarrow H + zH \tag{4.6}$$

$$zH \longleftrightarrow H + z^* \tag{4.7}$$

where H_2 is the molecular hydrogen, H the atomic hydrogen, z^* an active site on the filament surface and z a saturated site.

From left to right equation 4.6 represents the formation of atomic hydrogen and the adsorption of one hydrogen atom by the active site, while from right to left it represents the desorption of one hydrogen atom from the saturated site and the formation of molecular hydrogen. Equation 4.7 represents from left to right the formation of atomic hydrogen by desorption from the saturated site, while from right to left it represents the saturation of the active site with H on the filament.

The two reactions are promoted from left to right only when the filament temperature is high enough to effectively break molecular hydrogen into atomic H (reaction 4.6) and to release hydrogen from the saturated site (reaction 4.7). Moreover, the effectiveness of such reactions is also influenced by the gas mixture inside the CVD reactor. In fact, according to the simulation of Figure 4.10 [157], where the radical concentration in a HFCVD environment is plotted against the filaments temperature, the concentration of atomic hydrogen is higher than that of the carbon radicals only for filaments temperatures above 1900 °C.

Therefore filament temperature and CH_4 concentration are parameters of fundamental importance for diamond growth in a hot filament reactor.

The HFCVD method is relatively cheap, easy to operate and produces polycrystalline diamond films at a rate of 0.1-1 μm/h on large area substrates (from 4″ up to 8″) and even on three dimensional objects (for which the diamond layer serves as a protective coating). In addition, in contrast to the microwave plasma CVD (*MWPCVD*) method, HFCVD achieves lower ionizing rates and powers due to the thermal nature of the activation process; lower are hence the ions/molecules ratio and the ion energies in proximity of the substrate surface. On the one hand this leads usually to lower growth rates compared to *MWPCVD*; however, on the other hand the lower ion

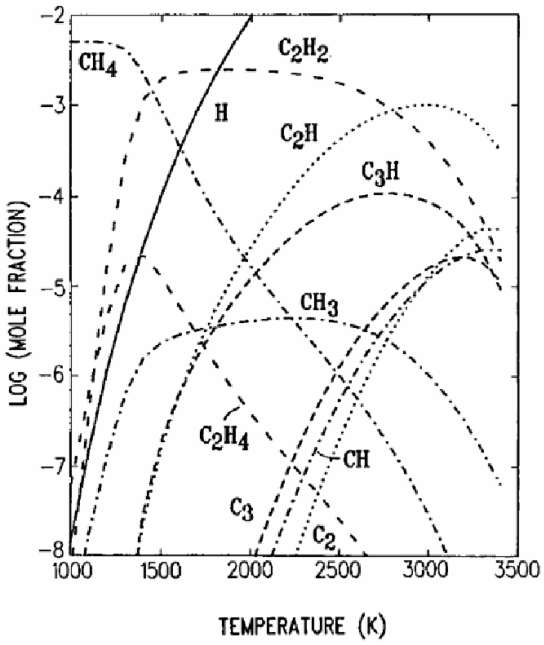


Figure 4.10: Densities of atomic hydrogen and other radicals generated in a *HFCVD* reactor as a function of filaments temperature (from [157]).

energies allow growing diamond on a larger variety of substrates, including the ones, which are etched or degraded by the stronger hydrogen microwave plasma.

A custom-made hot filament system has been used in this study; designed and realized by K. Janischowsky, this systems is equipped with in-situ *BEN* capability to nucleate and grow diamond on substrates of 2, 3 and 4 inches diameter [153]. The reactor is depicted in Figure 4.11, where a detailed sketch of the inner parts of the CVD chamber is also shown. The substrate wafer is held vertically by a pressure difference to avoid dust particle depositing on it; facing the substrate, at a distance of approx. 15 mm, 20 tungsten filaments are vertically placed, spanning an area of 4".

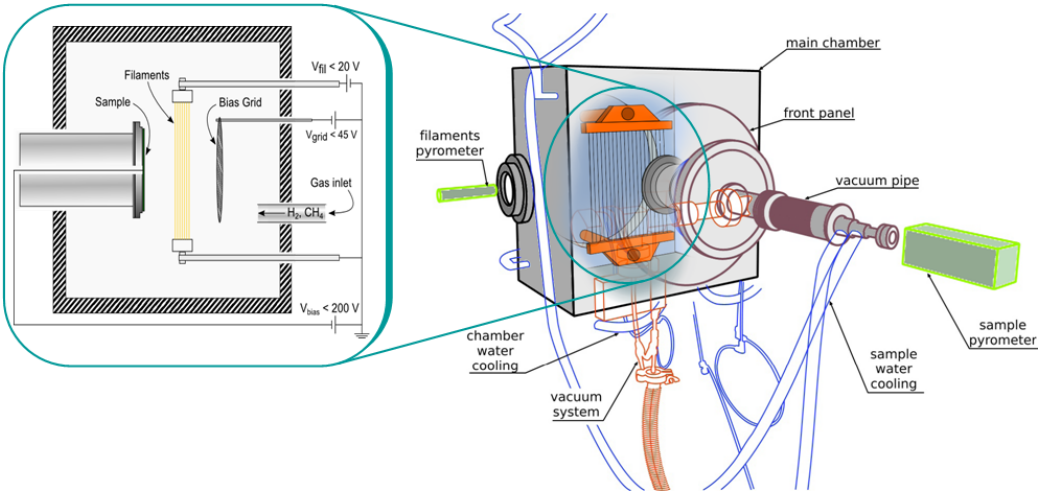


Figure 4.11: Schematic of the custom-made *HFCVD* designed by K. Janischowsky, with in-situ BEN capability (left inset reprinted from [153] with permission from Elsevier).

A tungsten grid is located close to the filaments, on the opposite side in respect to the substrate, at a distance of approx. 10 mm; this grid is used to increase the gas ionization rate in proximity of the filaments, which would otherwise be too small to allow performing *BEN* on foreign substrates in a reasonable time. In fact, in the case of HFCVD, the ion concentration in the plasma is much lower than in MWCVD, therefore ion bombardment of the substrate during *BEN* is usually less effective; to avoid this problem a second bias voltage is commonly used for *BEN* in HFCVD. This second bias is positive and is applied to the metal grid placed behind the hot filaments; the positive bias attracts and accelerates electrons thermally emitted from the filaments, hence increasing largely the gas ionization. During *BEN* process the substrate is biased at -200 V and the grid at +45 V.

Fig. 4.12 shows the ion current collected at the substrate as a function of time during a typical *BEN* process. The value assumed by the ion current at a certain time can be used to monitor the progress of the nucleation process: the current remains constant while a carbide layer gradually forms in the topmost part of the substrate due to the bombardment of the carbon-containing ions. As the first diamond nuclei appear on the substrate surface, the current increases due to the fact that diamond has higher electron emission than the substrate [153]. Continuing the process up to a complete coverage of the substrate with diamond nuclei leads to a maximum in the ion current (whose value varies according to the type and size of the substrate), after which it starts to saturate. At this point the substrate and grid biases can be turned off and the subsequent growth cycle follows. With the described setup, uniform, high nucleation densities in the range $10^{10} - 10^{11}\ nuclei/cm^2$ over a 4″ area can be achieved.

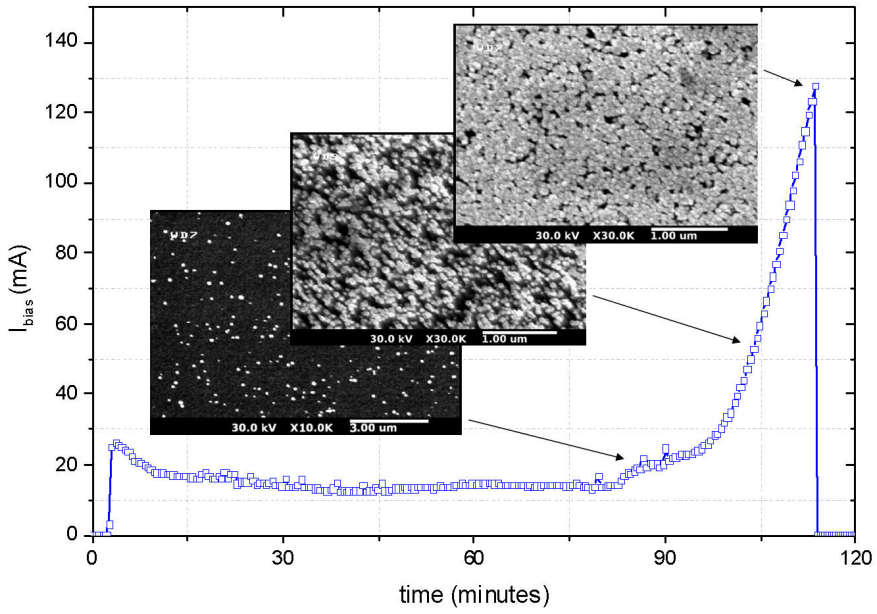


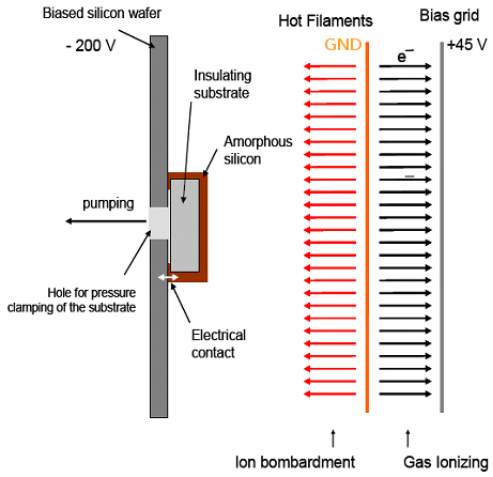
Figure 4.12: Trend of BEN bias current with process time and correlation with nucleation density. The SEM insets show the progressive coverage of the substrate with diamond nuclei.

4.7.1 *BEN on insulating substrates*

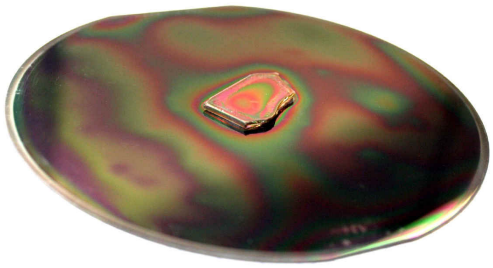
As described in Section 4.5, diamond growth by *BEN* requires a carbide-forming, electrically-conductive material to be used as a substrate, doped-Si being the preferred choice. Therefore *BEN* is not effective to initiate diamond growth on an insulating substrate like bare sapphire or quartz, since their high electrical resistivity prevents to apply the nucleation bias to the sample surface. Moreover, sapphire does not react with C to form a carbide layer, hence any diamond layer will not adhere well to the surface and delaminate easily.

To address these problems an intermediate, carbide-forming layer can be deposited on the substrate surface to act as diamond nucleation layer. The first step toward diamond growth is therefore the investigation of a suitable inter-layer for diamond nucleation. The single, most important requirement for the interlayer material is the carbide formation in order to promote diamond growth; in addition, the inter-layer thickness and its electrical resistivity have to be considered. Moreover, the interlayer should not influence the resulting multi-layer system, i. e. in optical applications it should not absorb light in the useful part of the light spectrum (visible, UV or IR), while in electrical devices (as surface coating) it should not introduce conductivity.

A Si-based inter-layer represents a suitable material since it can be deposited amorphous by means of a *PECVD* process at ~300 °C and the diamond nucleation conditions on silicon are already known. The nucleation configuration shown in Figure 4.13 has been adopted to perform *BEN* in the HF reactor used is this study.



(a)



(b)

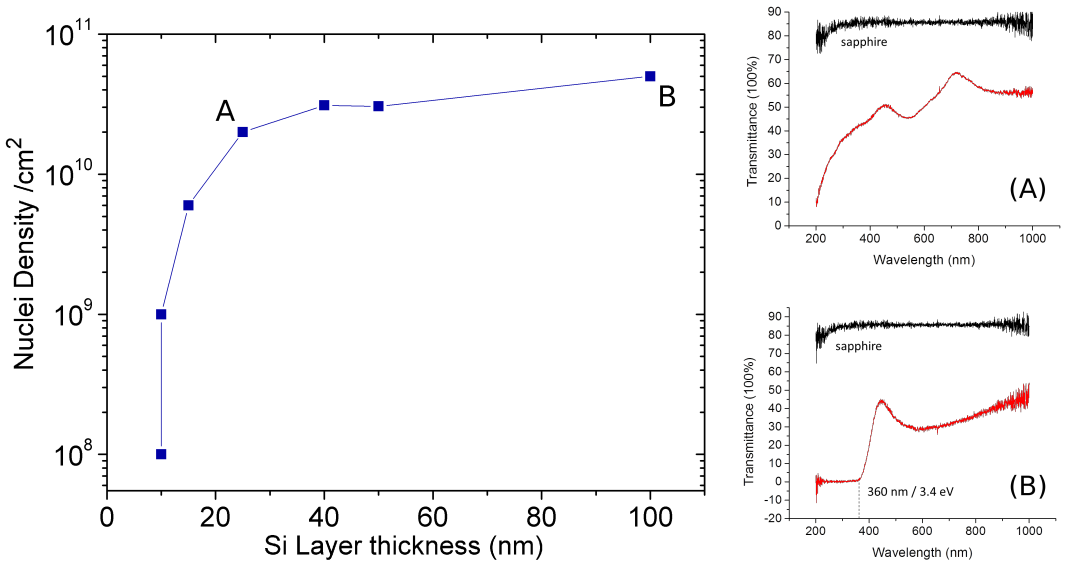
Figure 4.13: (a) Schematic of the sample arrangement when performing a BEN pre-treatment on an insulating substrate (from [158]); (b) picture of the wafer used as a holder and the sample after BEN.

Prior to the BEN treatment, the substrate is coated with a thin amorphous silicon film 50–100 nanometers thick, in a way that the surface and the sides and a part of the backside are coated. Although intrinsic (i. e. unintentionally doped), at the high temperatures of diamond growth the conductivity of this thin film is sufficient to assure uniform bias distribution over the sample surface. A 4" silicon wafer is used as sample carrier, clamping it to the graphite holder by pressure difference. When the

sample is clamped to the graphite holder, the nucleation bias is applied to the sample surface via the silicon wafer and the amorphous silicon on the sample backside.

In this way the ions accelerated toward the substrate see a whole 4″ silicon surface, namely the silicon wafer plus the amorphous silicon on the sample; this allows to monitor and to control the BEN nucleation process by the ion current in the same way as it is done for standard BEN nucleation on 4″ silicon wafers.

Z. Gao in [159] investigated the relationship between the nucleation density and the thickness of the silicon interlayer by performing several *BEN* experiments at a substrate temperature of 800 °C on sapphire substrates coated with an amorphous silicon film of thickness varying from 10 to 100 nm. The result of such a calibration is plotted in Figure 4.14a. As can be seen from the figure, the thinnest silicon layer which may be used to achieve a high nucleation density at this temperature is around 50 nm. Although partially consumed during the process by conversion to SiC, in this range of thickness residual Si phases are still present after *BEN*, as optical absorption measurements performed by Gao *et al.* [160] on diamond-on-sapphire samples showed (see Figure 4.14b). The strong absorption across the wavelength spectrum exhibited by diamond films nucleated on a 100 nm thick interlayer may indeed be ascribed to SiC or Si direct bandgap absorption. Since no Si-related absorption is instead detectable on the films nucleated on the thinnest interlayer (~25 nm), it can be inferred that if thin enough, the Si interlayer may supply the bias in the initial phase and be completely consumed at the end of the *BEN* process (ideal case for both optical applications and diamond coating of devices).



(a) (b)

Figure 4.14: (a) Nucleation density vs. silicon interlayer thickness at a substrate temperature of 800 °C (calibration performed by Z. Gao [159]); (b) optical transmittance of diamond films nucleated by *BEN* on a-Si/sapphire with varying interlayer thickness: 25 nm (top-A) and 100 nm (bottom-B) (from [160]).

However, very thin PECVD layers are less homogeneous and have a higher electrical resistivity, thus preventing a uniform bias distribution over the sample surface. This problem is particularly evident when nucleating large area substrates, like 2″ wafers.

In this case an additional coating step with a-Si on the wafer back-side, as sketched in Figure 4.15a, improves the BEN efficiency. Such a layer assures a better contact to the substrate holder and thus a more uniform bias distribution at the nucleation temperature and can be readily etched away after the growth process is terminated.

Figure 4.15b shows a 2″ sapphire wafer overgrown with 250 nm of diamond after the removal of the back-side Si layer. As can be seen in the figure, uniform diamond growth could be achieved over the whole wafer due to a high nucleation density above $10^{10}\,nuclei/cm^2$.

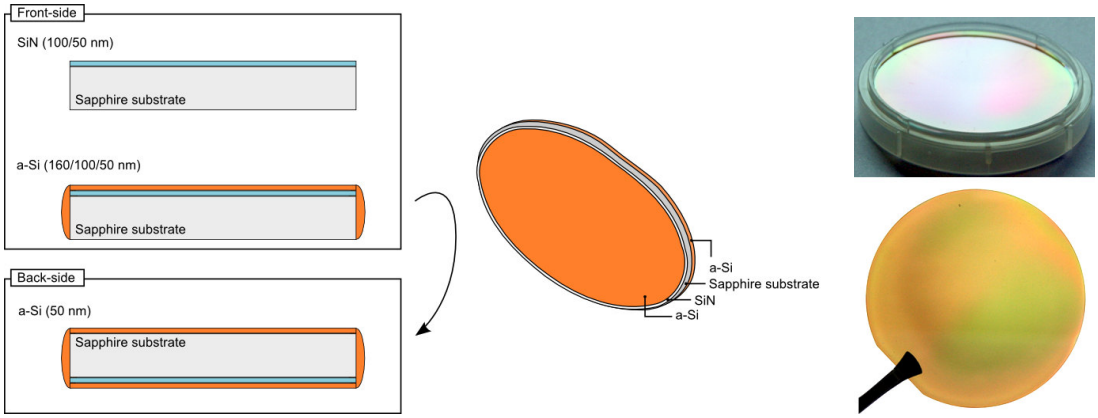


Figure 4.15: (a) Sketch illustrating the processing steps to deposit the Si nucleation layer on the front and on the backside of a 2″ sapphire wafer. (b) The wafer nucleated and overgrown with 250 nm of NCD.

4.8 MICROWAVE PLASMA CVD

A microwave plasma CVD (*MWPCVD*) reactor uses very similar conditions as compared to a HF reactor, and despite being significantly more expensive, this type is among the most widely used for diamond growth.

In an MW reactor, electric discharge produces the radicals necessary for diamond growth. The microwave power is coupled into the growth chamber via a quartz window in order to generate a discharge. According to the design and the size of the chamber cavity, only one microwave mode is permitted in order to create one plasma ball directly above the substrate surface. The microwave energy is transferred to electrons which oscillate and accelerate, thus ionizing the gas molecules.

In respect to HFCVD, MWPCVD is an intrinsically cleaner technique since there is no metal contamination. Furthermore the growth conditions are more reproducible in a MW reactor than in a HF one, because in the latter the filaments age with deposition time, hence changing their properties. Moreover each set of filaments is unique since it consists of several filaments, each similar, but not identical to each other. Therefore MWPCVD is the preferred system to grow diamond films with high phase purity, suitable e. g. for electronic applications.

On the other hand, HF allows diamond deposition on large area substrates greater than 2″, while MW systems are usually limited to smaller samples due the plasma ball size. Additionally, the plasma generated in a MW system may be too harsh acting

on the substrate surface, thus limiting the number of materials which can be coated with this technique. For instance, SiO_2 or Si_3N_4 films used as masks for selective diamond growth or passivation dielectrics in electronic devices are quickly etched in MWPCVD, as well as the Si-based interlayer used in this work to nucleate on insulating substrates.

5

DIAMOND THERMAL CONDUCTIVITY: REVIEW OF THE MAIN EXPERIMENTAL RESULTS

At temperatures above 50 K, diamond has the highest thermal conductivity of any known material. Gem-quality diamond exhibits values of room temperature thermal conductivity k in the range of 2000–2300 $Wm^{-1}K^{-1}$ [161], which are 5 times higher than that of copper.

Whereas electrical current flows in a material by means of charge carriers only, heat may be transported by both charge carriers and vibrations of the lattice ions. In a metal with high electron density like copper, nearly all of the heat conduction occurs via charge carrier transport. In this case the electronic contribution to the thermal conductivity masks the one of the lattice, which is present, yet small relative to the electronic term. In a material like diamond, where there are no free electrons to carry heat, the lattice thermal conductivity is the only mode of heat transport available.

This chapter will briefly review the main results of thermal conductivity measurements performed by various groups on single and poly-crystalline diamond materials and will refer to the theory of lattice thermal conductivity presented in Appendix A.1 for their interpretation.

5.1 THERMAL CONDUCTIVITY OF SINGLE-CRYSTALLINE DIAMOND

The thermal conductivity data of single-crystalline diamond obtained on several samples is plotted in Figure 5.1 [162], where the effect of different concentrations of the isotope ^{13}C on the thermal conductivity is also shown. The theoretical curves were calculated in the Debye approximation (see Eq. A.13 in the Appendix A.1) by employing a simplified form of the phonon scattering rate τ_U^{-1}, empirically adjusted for three-phonon processes.

As predicted by the theory of lattice thermal conductivity, at low temperatures the boundary scattering dominates, hence the conductivity increases as T^3. As the temperature increases, isotope scattering becomes important and reduces the T^3 dependence, until a temperature around 100 K is reached, at which three-phonon processes become the dominant scattering mechanism, and the conductivity starts to decrease. The precise value of the maximum depends on the ^{13}C isotope concentration in the crystal; indeed the 99.9% pure ^{12}C crystal exhibited the highest thermal conductivity of the batch, with $k = 41,000\ Wm^{-1}K^{-1}$ at ~80 K. Well above room temperature, the conductivity decreases nearly linearly with temperature, in agreement with the theory.

Harris *et al.* in [163] suggested the following equation for estimating the thermal conductivity of type IIa natural diamond and CVD-grown single-crystalline diamond in the range 300–1200 K:

$$k(T) = (2.833 \times 10^6)/T^{1.245}, \tag{5.1}$$

where k has the units $Wm^{-1}K^{-1}$ and T is in Kelvin.

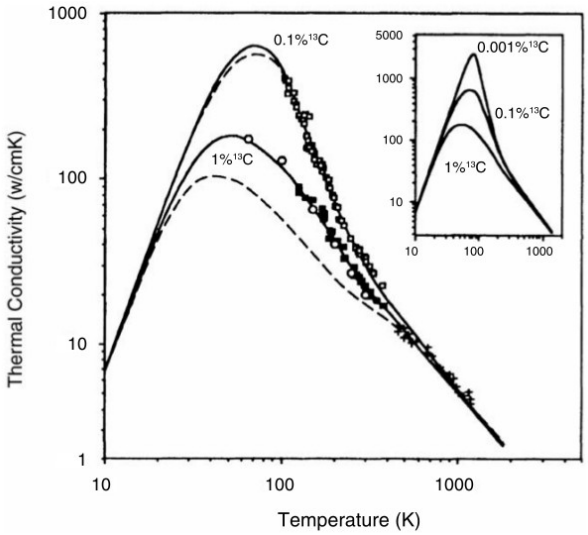


Figure 5.1: Thermal conductivity of single crystalline diamond with natural abundance of ^{13}C (1.1%) and for isotopically enriched samples (0.1% ^{13}C). Theoretical results for some other isotopic concentrations are shown in the inset (from [162]).

Equation 5.1 yields a k of 2340 $Wm^{-1}K^{-1}$ at room temperature, 1300 $Wm^{-1}K^{-1}$ at ~200 °C and 416 $Wm^{-1}K^{-1}$ at ~900 °C.

Knowing the temperature dependence of diamond thermal conductivity in the high temperature range is crucial to correctly evaluate its thermal management capabilities. In fact, the working temperature of a HEMT device is of approx. 200 °C, as shown in the previous chapters, and hence a diamond heat-spreader will exhibit a 40% lower k at that temperature compared to its RT value of ~2200 $Wm^{-1}K^{-1}$.

Despite this significant drop, diamond is still superior to other materials commonly used for thermal management purposes, like Cu, graphite, AlN or SiC. Referring to the data reported in Section A.1.2 of the Appendix, where the thermal conductivity of the above mentioned materials is plotted as a function of temperature, at 200 °C only graphite has a k of ~1000 $Wm^{-1}K^{-1}$ (and only in the lateral direction) while for Cu, AlN and SiC the thermal conductivity does not exceed 300–350 $Wm^{-1}K^{-1}$.

Besides the temperature dependence of k, it is important to consider the impact of the film microstructure on diamond thermal conductivity, as discussed in the next section.

5.2 THERMAL CONDUCTIVITY OF POLY-CRYSTALLINE DIAMOND

As described in Chapter 4, the heteroepitaxial growth of diamond by CVD on a foreign substrate results in an heterogeneous film with poly-crystalline structure in which the diamond crystals are embedded into a grain boundary matrix. According to the theory of lattice thermal conductivity, phonon scattering at the grain boundaries, by defects, dislocations and impurities will limit phonon diffusion lengths in such a material in a wide temperature range (0–500 K). Thus the thermal properties of poly-diamond may differ from the properties of the single-crystal counterpart and may vary significantly according to the thickness of the film, size, shape and arrangement

of the diamond crystallites (i. e. grains), as well as to size, orientation and composition of the grain boundaries.

The highest thermal conductivities have been measured on poly-diamond films grown with a columnar-structure [164, 34, 33, 165, 166, 167, 168, 169]. Figure 5.2a shows the cross section of one of such films (~280 μm thick), accompanied by top-view SEM micrographs taken at different distances from the substrate [34].

As explained in Section 4.6, by using growth conditions which result in a low α-parameter value, a columnar microstructure develops with film thickness as a consequence of the growth dynamics: the individual diamond crystallites, which nucleate on the substrate during the nucleation phase, enlarge and coalesce at the beginning of the growth process; after coalescence, through competitive coarsening of the grains, some of the initial nuclei eventually dominate and continue to grow assuming a columnar shape in which the average in-plane dimension of the grains increases with separation from the substrate while the out-of-plane dimension may reach several microns, up to the film thickness.

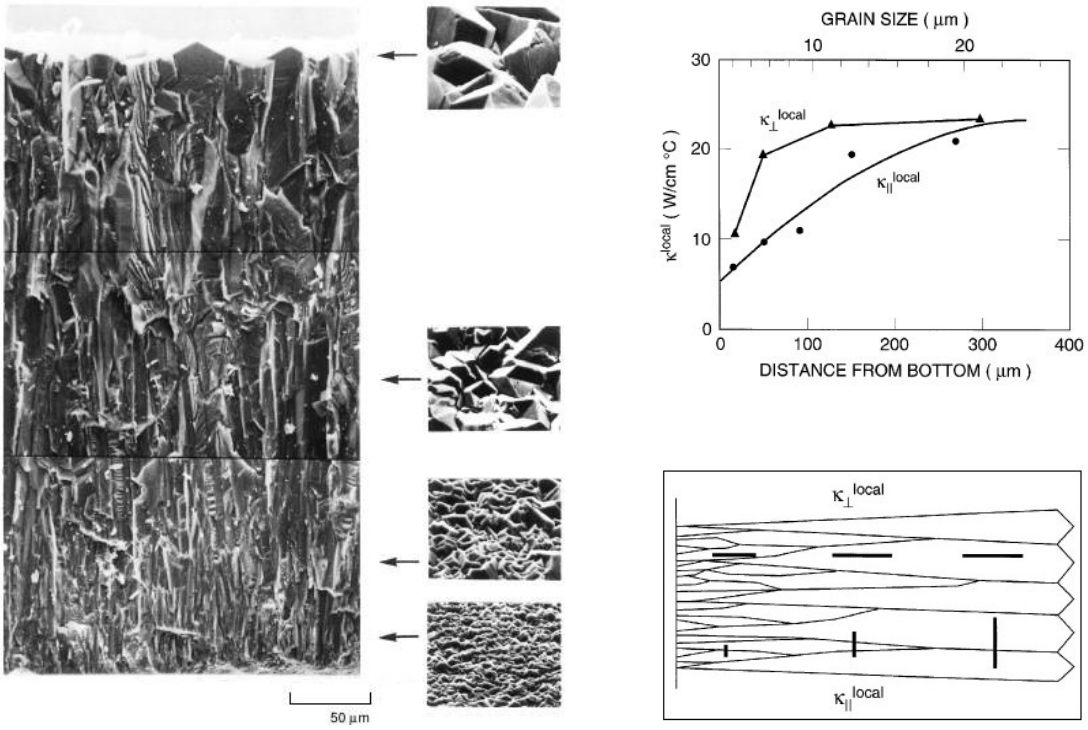
Thermal transport properties in the film are thus thickness-dependent and anisotropic, with a different conductivity for heat flowing perpendicular to the growth direction – the in-plane conductivity $k_{\parallel}$ – and for heat flowing parallel to the growth direction – the cross-plane (out-of-plane) conductivity $k_{\perp}$. Furthermore, the fine-grained less-perfect material near the substrate represents a boundary of high thermal resistance for the heat flowing into or out of the diamond. Since the total thermal resistance of the diamond film can be seen as the sum of the volume (bulk) resistance and interfacial resistance, when analyzing diamond thermal properties both the volume and the boundary contributions must be considered.

5.2.1 *Volume (bulk) properties*

Graebner et al. [33] investigated the volume contribution to the thermal properties of columnar poly-crystalline diamond films by means of *PCD* layers grown stepwise to a thickness of several hundreds microns. For measuring the in-plane thermal conductivity $k_{\parallel}$ with an accuracy of 1–2% they adopted a DC heated-bar technique on five samples prepared by microwave plasma CVD all under the same conditions, but differing in thickness (14, 48.5, 90.5, 145, and 285 μm). The cross-plane thermal diffusivity was measured with a fast version of the laser flash technique [165, 166] for four samples with thicknesses of 28.4, 69.1, 185, and 408 μm. The diffusivity values were then converted into thermal conductivity by multiplying with the heat capacity per unit volume, ρC.

As can be seen in Figure 5.2b, both thermal conductivities strongly depend on the film thickness, reaching single-crystal values ($2300 \pm 200\ W m^{-1} K^{-1}$) at large z (>350 μm), while being four times lower (~$550\ W m^{-1} K^{-1}$) at small z (~5 μm). In addition, the cross-plane conductivity is constantly larger than the in-plane one, with an anisotropy ratio $k_{\perp}/k_{\parallel} \sim 2$ for z in the range 30–100 μm.

Such trends correlate well with the film microstructure, with phonon scattering rates significantly higher in the fine-grained region of the film near the substrate than in the large-grained region close to the surface (for $z \sim 300$ μm), as well as for phonons diffusing across the columns rather than along them.



(a) (b)

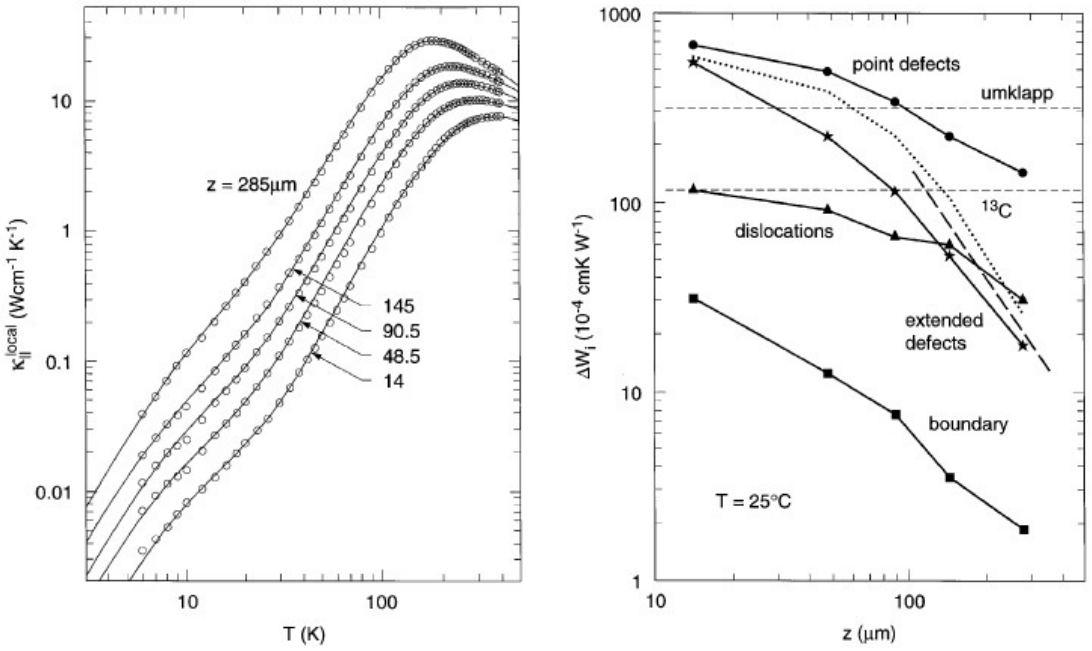
Figure 5.2: (a) Cross-sectional SEM micrograph of a 280 μm thick *PCD* film showing the dependence of grain size on the height above the substrate. (b) Local thermal conductivity vs. height (distance from the bottom) for heat flowing parallel ($k_{||}$) or perpendicular ($k_{\perp}$) to the plane of the specimen, with a schematic illustration of the nonuniform, anisotropic microstructure of CVD diamond films (from [34]).

Measurements of k over a wide temperature range shed light on the type and location of the defects responsible for thermal resistance in the film. Due to the different frequency dependences of the scattering processes (as described in Section A.1), by analysing k *vs* T curves it is indeed possible to differentiate between the effects of intra-grain/inter-grain defects and grain boundaries on the heat conduction.

The in-plane thermal conductivity $k_{||}$ of the above mentioned samples, measured from above room temperature to liquid helium temperature [165, 166], is plotted in Figure 5.3a.

In Figure 5.3b the partial resistivities due to a number of distinct phonon-scattering mechanisms (by phonons, by point/extended defects, by dislocations, by grain-boundaries) have been calculated by applying the phonon-scattering model of the thermal conductivity to the data. The plot shows that most of the resistivity in the poly-diamond film originates from phonon-scattering at defects and dislocations, besides phonon-phonon scattering events, but it does not tell where these defects may be located (i. e. within the grains or/and at the grain boundaries).

As suggested by Goodson and coworkers [170, 171], the factor of two in the anisotropy in the thermal conductivity at small film thicknesses observed by Graebner may be explained only if the extrinsic defects responsible for thermal resistance were preferentially located at the grain boundaries (hence called *dirty grain-boundaries*).



(a) (b)

Figure 5.3: (a) Local in-plane thermal conductivity $k_{||}$ vs. absolute temperature at five different heights z above the substrate. (b) Partial thermal resistivities ΔW at T=25 °C for the five different heights z, deduced from the fits to the data (from [167]).

Due to the amount of defects concentrated at the boundaries, phonon transmission through grain boundaries is very unlikely in the dirty grain-boundary model.

The dirty grain-boundary model predicts that in columnar-structured diamond films the phonon mean free path within each grain will be substantially longer than the one across several grains, since the latter will involve scattering at defect-laden grain boundaries. Moreover, it expresses all the extrinsic scattering mechanisms as a function of the film's grain size d.

Although the experimental data collected on poly-crystalline diamond films show significant scatter in the thermal conductivity values, the model gives a reasonably good fit over a wide range of grain sizes, as shown in Figure 5.4, where RT thermal conductivity data from nine separate reports are plotted [167].

Theoretical calculations considering clean and dirty grain-boundaries (dashed and solid line respectively) predict that at large d, where boundary scattering is negligible compared with intrinsic scattering, the in-plane thermal conductivity $k_{||}$ approaches 2500 $Wm^{-1}K^{-1}$, while at small d it decreases rapidly, with a gradient proportional to the cleanliness of the boundaries.

For dirty grain-boundaries, grain sizes smaller than ~10 μm may reduce the RT conductivity significantly, while with clean grain-boundaries the limitation to the thermal conductivity occurs only when the grain size is below ~1 μm. This discrepancy is due to the different phonon transmission coefficient across dirty and clean grain-boundaries. In the former case phonons diffusion is mostly limited to the intra-grain area, such that the thermal conductivity becomes very sensitive to the film's in-plane grain size when it drops below 10 μm. With clean grain-boundaries instead, the phonon/grain boundary transmission coefficient is high, thus the lateral size of the

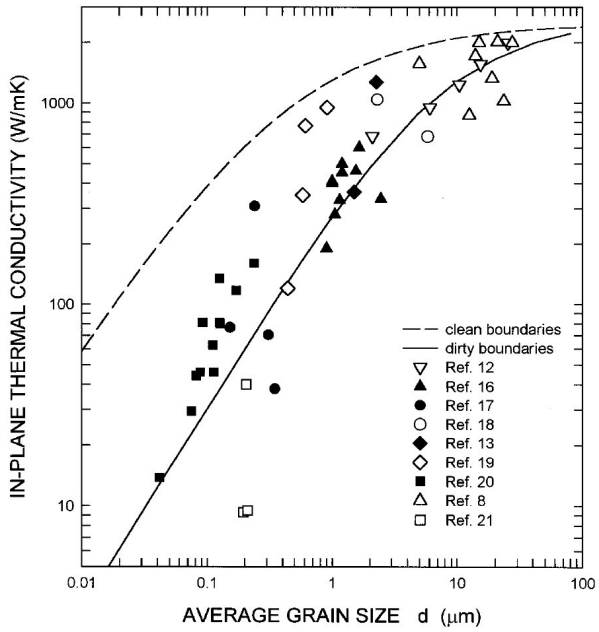


Figure 5.4: In-plane thermal conductivity $k_{||}$ vs. grain size for CVD diamond specimens. The dashed line is calculated on the assumption of clean grain boundaries; the solid line is for grains at which defects are collected (plot and references in the inset from [167]).

grains is less important than their phase-purity. In these conditions the phonon mean free path at RT is close to the natural diamond value of ~0.3 μm, therefore limitation to the conductivity are expected for grain sizes smaller than 1 μm.

Deviations of the experimental data from the two lines may be interpreted as *"cleaner"* or *"dirtier"* grain boundaries in the film, according to the growth conditions.

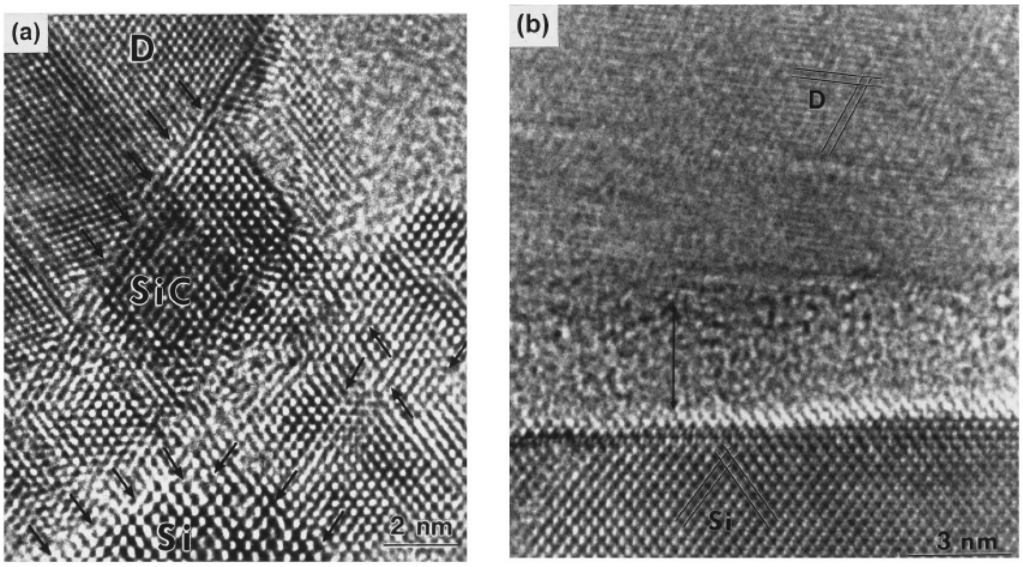
5.2.2 *Film/substrate interfacial properties (thermal boundary resistance)*

A major contribution to the total thermal resistance of poly-diamond films comes from the nucleation layer, i. e. the part of the film at the interface with the substrate, < 10 nm thick, where the diamond crystallites bond to the surface and initially nucleate. In this region a high rate of phonon scattering due to microstructural disorder, mixed carbon phases and fine-grained microstructure results in boundary resistances, which are in the range of $10^{-9} \div 10^{-7}$ m^2KW^{-1} when diamond layers are deposited on Si [172].

Nucleation method, nucleation density and grain dimension near the interface all contribute to determine thickness and structure of the nucleation layer, and thus its thermal boundary resistance (R_{th}) (*TBR*) with the substrate [173, 174, 29, 175].

As for the nucleation method, BEN and mechanical scratching for instance result in rather different interfaces, as described in the TEM study of Verhoeven *et al.* [29], from which the high-resolution pictures in Figure 5.5 are taken. Sample (a) was nucleated by BEN in a *MWPCVD* reactor, while sample (b) was mechanically scratched with 0.1 μm diamond powder.

Although small near-interfacial disorder can be observed for both samples, with a nm-thick interlayer between the Si substrate and the diamond film, each sample has a



(a) (b)

Figure 5.5: HRTEM of the interface CVD diamond and (001)-Si for a sample nucleated by *BEN* in a *MWPCVD* reactor (a) and one mechanically scratched with 0.1 µm diamond powder (b). Terminating lattice planes at the interface are indicated by arrows (from [29]).

different microstructure and a different phase-composition. In the case of sample (a) (Figure 5.5a), the interlayer has an average thickness of 10 nm and mainly consists of epitaxially oriented β-SiC nanocrystals, whose thermal conductivity is of ~ 340 $Wm^{-1}K^{-1}$. In addition, five diamond lattice planes match with four SiC lattice planes and five SiC lattice planes match with four Si lattice planes. Furthermore, the interface plane between the diamond grain and the β-SiC crystallites is smooth on an atomic scale.

For sample (b) instead, the initial phase of the growth after the scratching pre-treatment results in a thin, amorphous interlayer (~3 nm, marked by the arrow in Fig. 5.5b), which has poor heat transport properties ($k_{am} \sim 1\ Wm^{-1}K^{-1}$) and thus strongly impedes phonon transmission through the interface. Within this layer, no β-SiC could be identified.

Other important factors influencing the thermal boundary resistance are nucleation density and grain size at the interface, as detailed in the theoretical work of Touzelbaev and Goodson [176], in which a model for the thermal resistance caused by microstructural disorder near the substrate interface has been developed.

The model relies on phonon transport theory and a multi-layer subdivision of the near-interfacial region (see Figure 5.6), which is consistent with the electron micrographs shown above, and consists of:

A. an initial amorphous layer of mixed stoichiometry (non-crystalline and nanocrystalline combinations of carbon and substrate atoms) of thickness z_N up to a few nanometers (0–10 nm typically) and k of 1 $Wm^{-1}K^{-1}$;

B. a second region, for $z_N < z < z_N + \Delta z_C$, where the nucleated grains widen laterally, with increasing distance from the substrate, until they coalesce at the height $z = z_N + \Delta z_C$. The region between grains is supposed to be filled with amorphous material of stoichiometry increasingly dominated by carbon with increasing z. The thickness Δz_C depends on the nucleation density, on the initial size of the grains $d(z_N) = d_0$ and on the γ-parameter (slope of increase of grain size with the separation from the substrate) according to a linear increase in grain size $d(z) = d_0 + \gamma z$;

C. a region above the closure height, for $z > z_N + \Delta z_C$, where some of the grains terminate, while others grow larger and the grain boundary orientation is practically random. The thermal conductivity of this region is considerably larger than that of the regions below the closure height, which contain also amorphous material, and is a function of the grain size *d*;

D. a columnar region, for $z > z_N + \Delta z_C + \Delta z_R$, where the structure of the grains eventually becomes columnar and all the defects are considered to be located at the grain boundaries.

The thermal resistance is calculated as a function of the nucleation density, of the γ-parameter and of the concentration of imperfections near the grain boundaries.

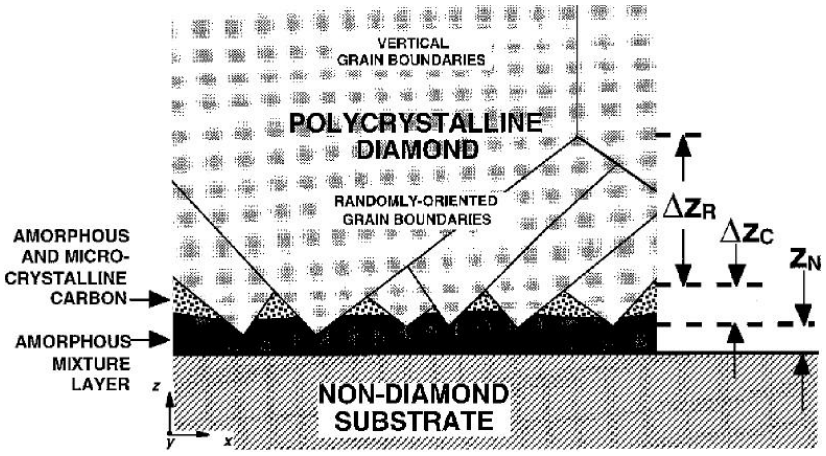
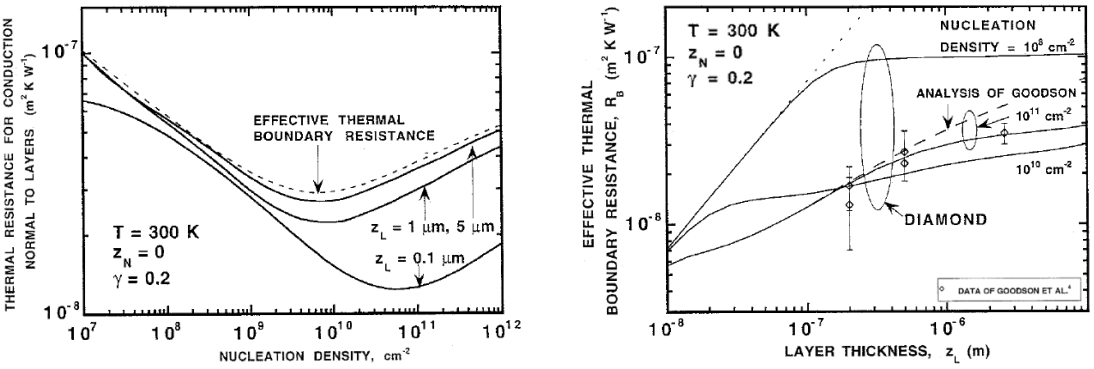


Figure 5.6: Subdivision of the disordered region near the interface diamond/non-diamond substrate (from [176]).

Figure 5.7a shows the impact of the nucleation density on the interfacial resistance for different thicknesses z_L of the diamond film (0.1, 1 and 5 μm) as predicted by the model (with parameters T=300 K, $z_N = 0$, $\gamma = 0.2$).

The general trend is that of a lower thermal resistance at higher nucleation densities, but the minimum *TBR* is also a function of the final thickness of the diamond layer. The size of the grains at the interface depends on the nucleation density, and on this initial size in turn depends the subsequent development of the columnar structure. While for thin films < 100 nm it is preferable to have a high density of small grains to assure a close, continuous diamond layer in the shortest distance from the interface, thicker films would benefit from larger grains near the interface (and thus from a lower nucleation density), which reduce the phonon scattering rate and allow a

faster lateral development of the columns. But a low nucleation density may reduce the direct contact area between the diamond crystallites and the substrate and may increase the volume fraction of amorphous material near the interface, both of which increase the final boundary resistance. Therefore a minimum boundary resistance can be reached only as trade off between these two competing approaches. According to the model the optimal nucleation density for μm-thick films is of approx. 10^{10} cm^{-2}.



(a) (b)

Figure 5.7: (a) Thermal resistance normal to layers as a function of nucleation density for different thicknesses z_L of the diamond film; (b) variation of the resistance normal to layers with nucleation density and film thickness z_L (from [176]).

In Figure 5.7b the effective boundary resistance is plotted against layer thickness z_L and nucleation density for columnar-structured thin diamond films, where experimental data [173] have been fitted by the model (with parameters T=300 K, $z_N = 0$, $\gamma = 0.2$). The predicted resistances are consistent with the measured values considering the experimental uncertainty and well reproduce the trend of an effective *TBR* increasing with the film thickness, which was also observed in other studies [29, 172]. According to the model, such a trend results from the the sum of the contribution of each region.

Layers with low nucleation density close at higher distance from the interface, thus the low thermally conductive regions below the closure height have the greatest influence on the resistance, which initially increases steadily with thickness till saturating at the height, where the closure takes place. The regions above closure have indeed large grains, whose contribution to the total resistance is relatively small.

In contrast, layers with high nucleation densities ($> 10^{10}$ cm^{-2}) close at very small values of z, but have smaller grains at the closure height, and thus experience a slower widening of the in-plane grain size, which results in a gradual increase of the thermal conductivity with increasing thickness. For this reason, the resistance is in this case distributed across the whole layer – where the topmost (columnar) region has the smallest contribution – and thus follows a monotone trend with film thickness.

In conclusion, depositing high thermally conductive poly-diamond films with low interface resistance critically depends on the nucleation pre-treatment and on the set of parameters chosen for the initial overgrowth.

When bias enhanced nucleation is followed by growth under ideal conditions, the pristine diamond nuclei are either in direct contact with the substrate, establishing

covalent bonds, or separated from it by a thin layer of β-SiC, which is crystalline and is a good thermal conductor. Under these conditions, the boundary resistance may be as low as 4×10^{-9} m^2K/W [29], while films prepared with less ideal conditions may exhibit two orders of magnitude higher resistances [172].

5.2.3 *Influence of the growth reactor on the thermal properties*

Besides film microstructure and interface composition, also the CVD technique chosen for the deposition of a poly-diamond film may have an impact on its thermal properties. As discussed in Chapter 4, diamond films deposited in a *MWPCVD* reactor are usually of higher crystalline quality than the ones grown in *HFCVD*, and thus may show higher thermal conductivities. Morelli *et al.* [177, 178] measured and compared the thermal conductivity of thick (600 and 250 μm) poly-diamond layers produced by microwave plasma and hot-filament CVD methods, for temperatures between 0.15–300 K.

Figure 5.8 shows the thermal conductivity and phonon mean free path data for the two samples, compared to natural diamond. In the explored temperature range, the MWP sample followed more closely a Debye model and it showed indeed higher thermal conductivity than the HF sample. The slight deviation from the Debye model observed for the HF sample, with a dip in the thermal conductivity curve between 20–60 K, is due to phonon scattering from extended defects. These defects, attributed to regions of disordered carbon material at a very low level of concentration, are present also in the MWP sample, but show up at lower temperatures due to their different size (~15 vs 5 Å).

Therefore, although MWPCVD-deposited diamond films may outperform HFCVD layers in the low temperature range, above RT, where grain-boundaries and phonon-phonon scattering domitate, the difference between HF and MWPCVD-deposited diamond films is expected to be negligible, both in terms of thermal conductivity and phonon mean free path.

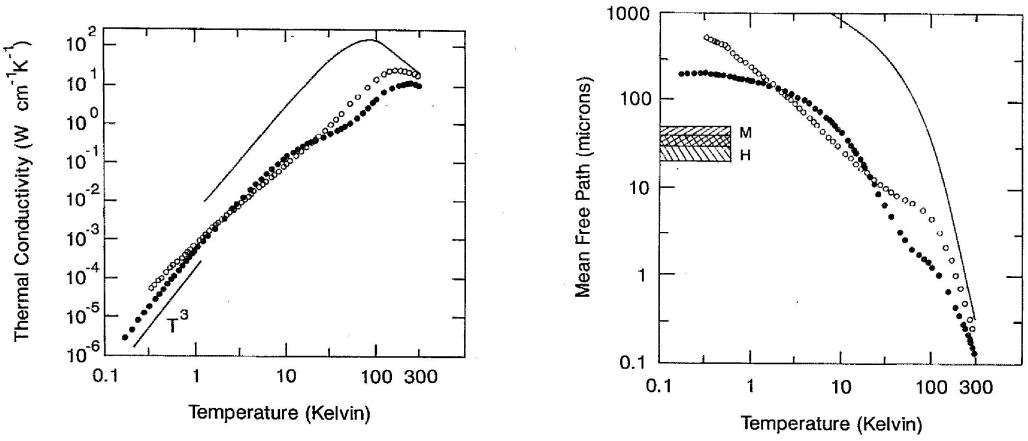


Figure 5.8: Thermal conductivity (left) and phonon mean free path (right) of two diamond films deposited by HF-CVD [sample H, closed circles] and MW-PCVD [sample M, open circles] from 0.15 to 300 K, compared to single-crystalline diamond [solid line] (from [177]).

6

GROWTH OF THIN NANOCRYSTALLINE DIAMOND FILMS

As described in Chapter 4, poly-crystalline diamond films, whose grains have dimensions spanning from a few nanometers up to several hundreds nanometers, are commonly identified with the term nanocrystalline diamond (*NCD*).

With a sp^3-C content between 95% and 99.9%, the balance made up from other forms of carbon (sp^2-C, α-C), this class of material embraces a continuous range of composition, morphology and properties, which depend on the nucleation and growth conditions, as discussed earlier [179, 180, 146, 30]. After a nucleation stage, in which individual diamond crystallites nucleate on the substrate, during the outgrowth the initial nuclei develop into vertical columns or spherical nanocrystallites according to the growth conditions, the difference being the suppression or the enhancement of re-nucleation processes respectively. Based on their microstructure, a convenient way to classify these films is therefore in either 2D-/columnar-NCD or in 3D-NCD.

2D-NCD. It is deposited by making use of a highly dilute concentration of methane in hydrogen (< 1%) and high growth temperatures (> 600 °C). In such conditions a small re-nucleation rate limits the competitive coarsening of the grains as they enlarge and merge, leading to columnar grains, whose maximum in-plane size does not exceed a few hundreds of nm, whereas the vertical size may extend to the full thickness of the film. The local grain size in this material will depend on the distance from the nucleation layer and on the growth conditions. This particular structure has important consequences on the physical properties of 2D-NCD films.

3D-NCD. Such a structure is obtained by allowing a strong re-nucleation, which leads to cauliflower-like crystals and a small-grained diamond film with an extended grain boundary network and a significant sp^2-bonded carbon content (up to 5% for *UNCD* [181]). This is achieved either by increasing the methane content [182, 183] or by adding inert gases in the reactor [181, 184], both of which reduce the hydrogen concentration in the plasma, hence allowing some sp^2-bonding to create new nucleation sites on the facets of growing crystals. The diamond grain size in this growth mode typically does not exceed tens of nanometers in all three dimensions, independent of the film thickness, similar to the type of ultra nanocrystalline diamond grown by Gruen *et al.* [180].

Figure 6.1 shows a comparison between the surface morphology and the film microstructure of a *PCD* film and of nanocrystalline diamond films grown in 2D and 3D mode. The plots indicate, for each film structure, the variation of the in-plane dimension of the grains d (as measured at the surface) with film thickness.

As said, shape and average size of the grains in nanocrystalline diamond are critical for the thermal properties of these films. According to the dirty-grain-boundary model described in Chapter 5, in such nano-structured materials phonon scattering will mostly take place at the grain boundaries, where defects, dislocations, impurities and non-diamond phases are preferentially accumulated.

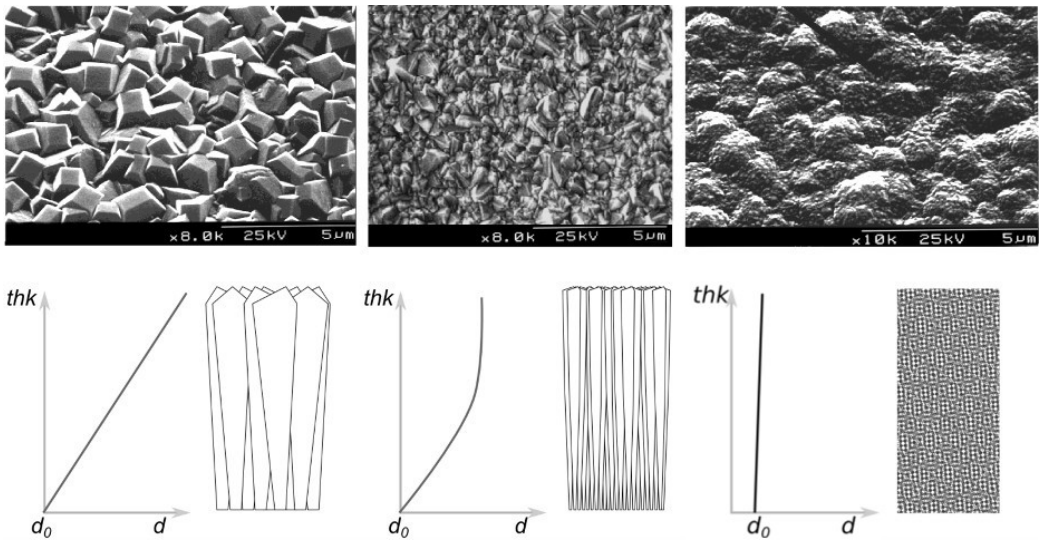


Figure 6.1: Comparison between the different microstructures of a CVD diamond film: *PCD* (left), 2D-/columnar-structured *NCD* (middle) and 3D-*NCD*. For each case, morphology at SEM, sketch of the structure and plot of film thickness vs grain size are provided.

Due to their fine-grained structure, the thermal conductivity of NCD films grown in 3D-mode is indeed rather low and isotropic, independent of the film thickness, with k of ~5–20 $W m^{-1} K^{-1}$ [185, 186, 187]. With the columnar grain structure instead, the average thermal conductivity for 2D-NCD films may reach ~1300 $W m^{-1} K^{-1}$– which is nearly 60% of the single crystal value – even for thin films in the micrometer range [30], but it is highly anisotropic and thickness dependent.

It is therefore clear that the thermal properties of these films (as well as the mechanical, optical and electrical ones) can be controlled and tuned to a large extent by manipulating the growth parameters. For the thermal management application pursued in this work, in which a NCD film would serve as a heat-spreading layer directly deposited atop GaN-based HEMTs, we have relied on thin, micrometer-thick, columnar-structured NCD films.

6.1 FILM MICROSTRUCTURE OF 2D-NCD

The nanocrystalline diamond films studied here were deposited in the custom-made HFCVD reactor described in Section 4.7 by a two-step process, consisting of a nucleation phase by in-situ *BEN* followed by an outgrowth phase whose parameters have been properly tuned to obtain the columnar structure sketched in Fig. 6.2.

Observing the development of the grain structure with increasing distance from the substrate, three characteristic regions can be identified:

1. The nucleation layer, i.e. the part of the film at the interface with the substrate, characterized by small grains with average size d_0 and high concentration of grain boundaries.

2. A coalescence/transition region, where the transition from single diamond nuclei to a columnar structure takes place; in this part of the film the in-plane

dimension of the grains at a certain thickness z can be expressed by the linear relationship $d(z) = d_0 + \gamma z$, where γ is the grain growth gradient.

3. A columnar-structured region, characterized by columnar-shaped grains of constant lateral size d_c (in the hundreds of nanometers range), independent of the layer thickness, and nearly vertical grain boundaries.

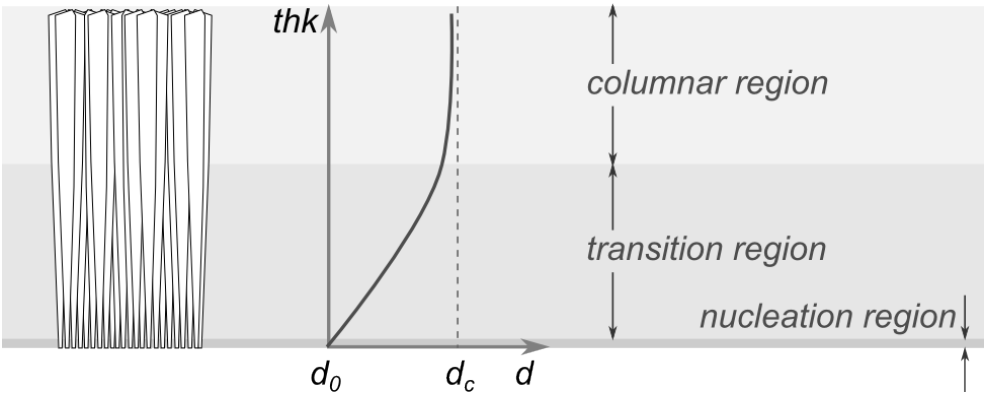


Figure 6.2: Microstructure of a 2D-/columnar-structured NCD film indicating the different regions in the layer.

As mentioned, the structure, and hence the thermal resistance of each of these regions may vary significantly according to the nucleation method and to the set of growth parameters used to outgrow the initial nuclei. For instance, the dimension of the grains at the interface varies depending on the nucleation density and on the initial stage of overgrowth. This in turn reflects on the transition region, whose thickness can be small or large depending on how much the lateral coarsening of the pristine crystals is favored compared to the vertical one (i. e. on the α-parameter), which in turn is a function of the growth parameters.

Therefore, prior to attempting the overgrowth of GaN HEMTs, the effect of the deposition parameters on the film microstructure must be carefully studied both at the nucleation and at the overgrowth stages.

6.2 GROWTH STEP 1: NUCLEATION PHASE

During the nucleation phase, diamond crystallites are embedded into the substrate to act as seeds for the subsequent growth cycles. We adopted in-situ *BEN* (see Section 4.5) to initiate diamond growth on a Si-based substrate (i.e. Si wafers as well as a Si interlayer used for NCD deposition on GaN-based HEMTs on sapphire or SiC substrates). The main reason to rely on this method is the creation of a covalent bond between diamond nuclei and the Si-based substrate and homogeneous, high nucleation densities of more than or equal to 10^{10} nuclei/cm^2. Due to the resulting strong mechanical adhesion, good phonon coupling across the interface, as well as enhanced thermal contact between substrate and diamond film may be achieved.

In order to obtain the lowest possible thermal boundary resistance (R_{th}) with the substrate (see Section 5.2.2) an optimized BEN pre-treatment was adopted, which aimed at achieving:

A. the optimum nucleation density, which for sub-μm thick films lays in the range $10^{10} - 10^{11}\,cm^{-2}$;

B. a smooth transition between substrate/NCD film, ideally through SiC crystals and without any interstitial amorphous phase.

To ascertain the features of *BEN*-nucleated films in respect to point A and B, a series of nucleation experiments were conducted, in which two key parameters for the *BEN* process in the HF reactor were varied, namely the filaments temperature T_{fil} and substrate temperature T_{sub}, while the other parameters (i. e. CH_4 concentration, reactor pressure and bias voltage) were kept constant (see Table 6.1). Fine control over both filaments and substrate temperature during *BEN* is crucial to satisfy conditions A and B.

The amount of atomic-H and carbon-containing ions generated in proximity of the filaments and subsequently accelerated towards the substrate depends on filaments temperature. The C-containing ions act as seeds for the formation of diamond nuclei, while the H-radicals preferentially etch the non-diamond phases concurrently forming on the substrate's surface. However, the combined effect of ion-bombardment and H-plasma etching is very harsh for any kind of material used as substrate, and may easily result in surface roughening with the creation of nm-deep pits in the areas where the etching is more intense. These pits are prone to originate voids or to be filled with amorphous material, both of which are detrimental for the heat transport properties of the interface. Therefore, a temperature window for the filaments had to be identified, in which the H-plasma density is not destructive to the sample surface (i. e. no pits) and in which the amount of C-radicals produced is high enough to assure a high and uniform nucleation density.

The initial development of the diamond seeds gradually forming on the surface depends on the substrate temperature during *BEN*. In fact, the temperature of the substrate affects the mobility of the radicals in proximity of the surface, and it hence drives the surface reactions, which determine the growth dynamics of the diamond nuclei. However, substrate temperature becomes critical when *BEN* is performed on a device, because it sets the thermal budget, which the device has to withstand for the duration of the process, and thus it has to be as low as possible not to damage the device itself due to an excessive heat load.

Table 6.1: Process parameters used during the BEN pre-treatment of the different samples.

process parameter[*]	UTEM3	UTEM2	UTEM8
T_{fil}(°C)	2100	2120	2150
T_{sub}(°C)	770	800	730
nucleation layer properties			
η^1 ($10^{10}\,cm^{-2}$)	1	1.2	1.1
α-C thickness (nm)	~ 20	~ 10	< 3

[*] other BEN parameters kept constant: $CH_4/H_2 = 1.3\%$, $P_{CVD} = 1.5$ kPa, $V_{fs} = 200$ V.
[1] average value, calculated from SEM micrographs.

Samples with an InAlN/GaN heterostructure on sapphire were used as substrate for the experiments. *BEN* took place on a PECVD-deposited interlayer stack consisting of a-Si/SiO2, 50 and 100 nm thick respectively (an approach described in details in Section 4.7.1). The filament temperature was set at 2100, 2120 and 2150 °C, while the substrate was kept at 770, 800 and 730 °C respectively (see Table 6.1).

As can be seen from the SEM micrographs of the samples surface, taken immediately after the *BEN* phase (Figure 6.3), the nucleation was uniform, with an estimated density η constantly above 10^{10} cm^{-2} for all the samples, regardless of filament and substrate temperature during the *BEN* process.

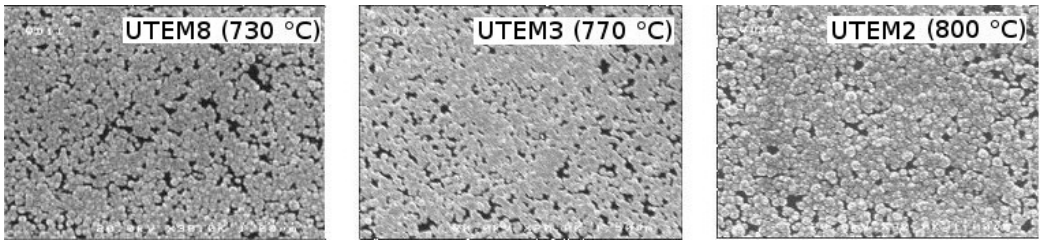


Figure 6.3: SEM images of the samples surface after performing the *BEN* treatment at different substrate and filament temperatures.

To investigate the impact of the process variables on the interface NCD/substrate, the samples were then subsequently overgrown with 250 nm of 2D-/columnar-NCD and cut to be analyzed by TEM[1]. From the high resolution TEM analysis of the interface presented in Figure 6.5, it can be seen that all the three samples exhibited (laterally) homogeneous layer structures on top of the interlayer stack deposited onto the InAlN/GaN heterostructure, with no voids between the Si interlayer and the diamond film. The originally amorphous Si layer recrystallized during the diamond *BEN* and outgrowth process, showing a nanocrystalline microstructure, thus the label *poly-Si* in the picture.

A transition layer can be observed between the poly-Si and the diamond film consisting of nanometer-sized cubic SiC particles intermixed with amorphous-C on top of which the diamond film started to grow. The thickness of this transition layer is different among the samples, passing from ~ 20 nanometers of sample *UTEM3*, nucleated at the lowest filament temperature (2100 °C), to a few nm for sample *UTEM8*, nucleated at a filament temperature of 2150 °C.

To explain the observed correlation between filaments temperature and thickness of the transition layer, the elemental maps of Figure 6.4 – where the oxygen and carbon content in the two samples UTEM3 and UTEM8 is shown – provide useful complementary information. Particularly interesting is the oxygen map of *UTEM3*, where a thin SiO2 film is clearly visible on top of the poly-Si layer. Such native oxide film normally forms when the Si is exposed to air, and should be etched away in H-plasma during the early stage of the nucleation phase, since it impedes effective biasing of the Si surface and it also prevents carbon diffusion through the layer, both crucial to allow a successful *BEN*.

1 analysis performed by L. Toth and B. Pécz at the Research Institute for Technical Physics and Materials Science (MFA), Budapest, Hungary.

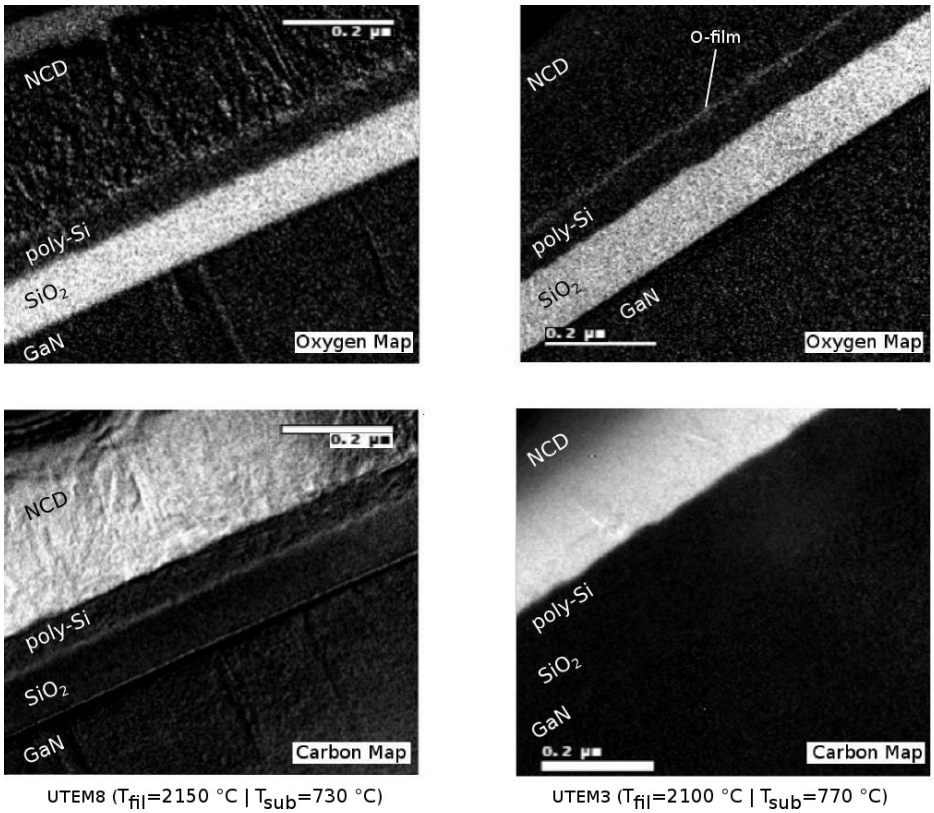


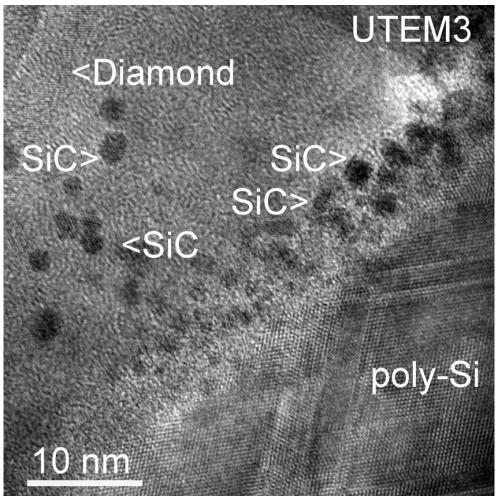
Figure 6.4: Oxygen and carbon EELS elemental maps obtained by TEM on samples UTEM8 and UTEM3.

During the nucleation of *UTEM3*, the filament temperature was most likely too low to produce enough H-radicals and the SiO2 layer was only partially etched, when an amorphous-C film started to form on top of it. Indeed in the C-map of Figure 6.4 no carbon could be detected below the surface of the poly-Si layer and the separation between the phases poly-Si/SiC/α-C is quite sharp. SiC particles embedded within this amorphous-C film probably acted as seeds for the first diamond nuclei.

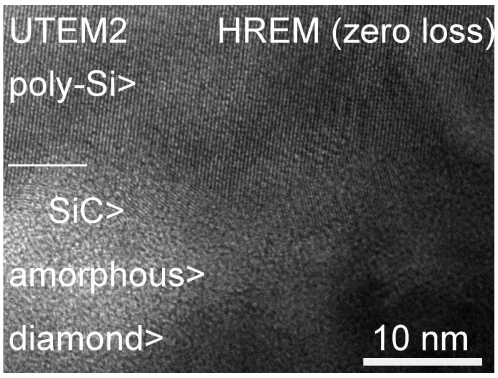
For *UTEM8* instead, the higher filament temperature allowed efficient etching with complete removal of the native SiO2 layer. Thus carbon from the chamber could diffuse into the Si, bonding with its surface atoms and forming SiC, on which diamond nuclei started to form with almost no transition layer in-between.

These results prove that the *BEN* method allows high nucleation densities and fine control over the disordered region at the interface with the substrate. Composition and thickness of this high thermally-resistive part of the film depend strongly on the process parameters.

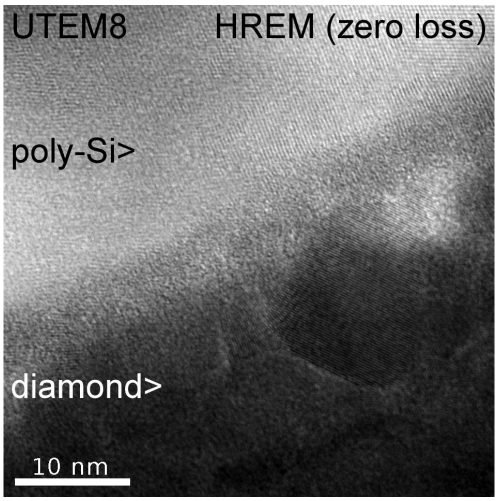
NCD films nucleated by in-situ *BEN* in our HFCVD at $T_{fil} = 2150$ °C and $T_{sub} > 730$ °C exhibited high nucleation densities above 10^{10} cm^{-2} and a smooth transition between Si substrate/diamond overlayer, with practically no disordered region between the two.



(a) High resolution (zero loss) image of the interface region of UTEM3 showing that the formation of diamond film starts with cubic SiC particles of 2-3 nm size on the surface of the polycrystalline silicon layer. The characteristic spacing of diamond phase can only be observed above this 10-20 nm thick transition layer.



(b) High resolution (zero loss) image of the interface region of UTEM2 showing a 3-4 nm thick SiC layer covering the rough surface of the polycrystalline Si. The diamond particles start to grow together with an amorphous phase on the top of this intermediate layer.



(c) High resolution (zero loss) image of the interface region of UTEM8 with practically no interlayer between the polycrystalline Si layer and diamond phase.

Figure 6.5: High resolution TEM images of the interface between diamond and the poly-Si nucleation layer for samples UTEM3 (a), UTEM2 (b) and UTEM8 (c) [analysis performed by L. Toth and B. Pécz at the Research Institute for Technical Physics and Materials Science (MFA), Budapest, Hungary].

6.3 GROWTH STEP 2: OUTGROWTH PHASE

After nucleation, the surface of the substrate is covered with nearly coalesced, nm-sized diamond crystallites with random orientation. In the subsequent outgrowth phase, the deposition parameters need to be properly tuned to outgrow these nano-nuclei in 2D-/columnar-mode. Moreover, to improve the lateral heat transport, the growth should take place with conditions allowing to reach the columnar growth regime in the shortest distance from the interface.

The outgrowth task consists therefore in identifying the *HFCVD* process parameters, which have the greatest influence on the grains structure, and in gaining then a comprehensive knowledge about the range in which these key parameters can be suitably adjusted. The main growth parameters for a *HFCVD* system are: gas precursors concentration (methane and hydrogen in our case), filament and substrate temperature, reactor pressure and filament-substrate distance. The role of each of these parameters may vary substantially depending on the reactor, in which the growth is performed. Filament temperature, chamber pressure and distance between filament(s) and substrate influence mostly the film deposition rate [188, 163, 189, 190, 191, 182], while methane concentration and substrate temperature directly affect size and configuration of the diamond crystallites by controlling the re-nucleation rate and the content of non-diamond phases embedded in the film.

In the following, the influence of these two key parameters on the microstructure of the NCD film, on grain boundary density and on non-diamond content are evaluated by means of SEM/AFM microscopy and Raman spectroscopy. The information provided by such an analysis was crucial to define a growth recipe allowing high-thermally conductive films to be deposited within the thermal budget constrains imposed by a GaN HEMT device.

6.3.1 *Influence of* CH_4 *concentration on the microstructure of NCD*

According to the α-parameter model described in Section 4.6, during the outgrowth phase a highly dilute concentration of methane in hydrogen (< 1%) and high substrate temperatures (> 650 °C) are needed in order to develop a 2D/columnar-texture in a *NCD* film.

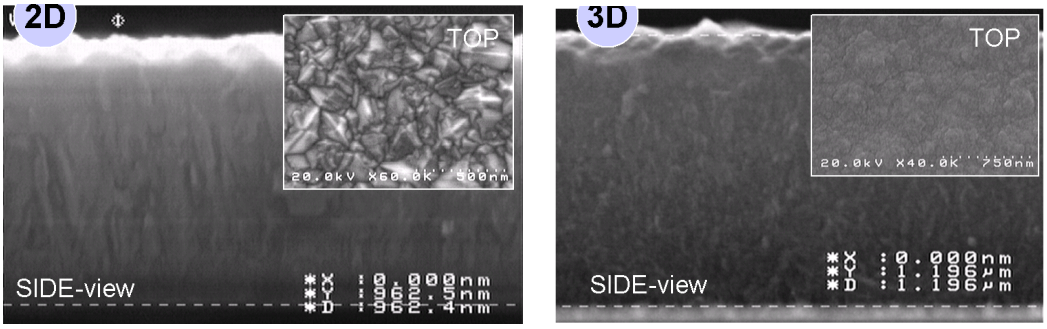
To verify the applicability of this model for the hot-filament reactor used in this study, a series of NCD overgrowth experiments was conducted, in which nucleated samples were overgrown stepwise to several thicknesses by using two different methane concentrations (0.4 and 2.0%), while keeping the other parameters constant (CVD pressure of 1.5 kPa, filament temperature of 2150 °C, substrate temperature of 730 °C). For each sample, the average in-plane grain size d at the surface was calculated from SEM micrographs and AFM surface maps taken after each growth step, while the layer thickness was estimated from SEM cross-sections.

In the plot of d vs. film thickness, each growth mode should result in a different trend, as illustrated in the sketches of Fig. 6.1 and 6.2 at the beginning of this chapter. In fact, in 2D-mode the in-plane size of the grains increases steeply within a short distance from the interface with the substrate (the part of the film labeled as *transition region*) and then, when the in-plane dimension of the grains can not grow further, it

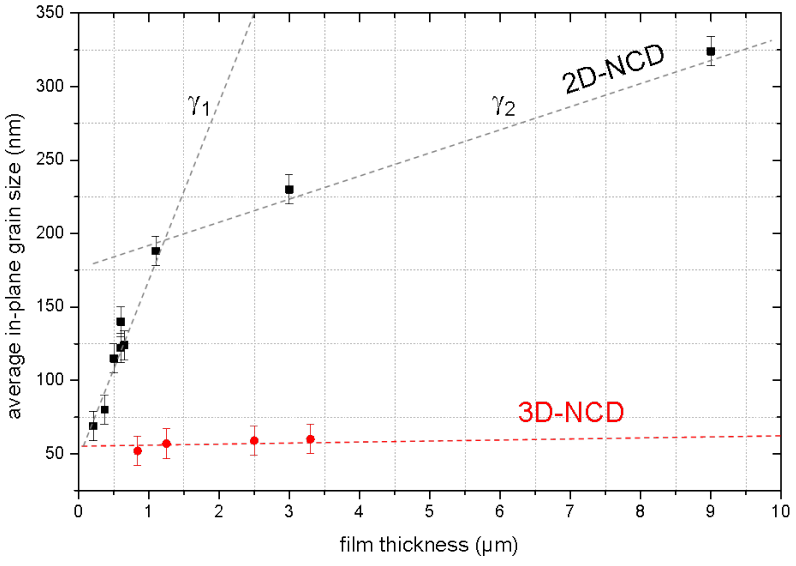
saturates to a constant d_c in the *columnar region*. In 3D-mode instead, the in-plane size of the grains does not depend on the film thickness, and it is not significantly different from the initial size of the grains d_0 measured after the initial nuclei have coalesced to form a closed film.

The plot of the experimental data collected on the actual samples (shown in Figure 6.6c) indeed confirms the expected trends. For the films grown at a methane concentration of 2%, the in-plane grain size remained constant with thickness at a value of approximately 50 nm, which indicates the growth was in 3D-mode with resulting fine-grained microstructure. When the methane concentration was set to 0.4% instead, the films exhibited an in-plane grain size which increased steeply with thickness in the first µm and gradually saturated to ~300 nm within 10 µm. The mode was therefore 2D, resulting in a film with typical columnar structure.

The difference in microstructure and morphology for two of these films at the thickness of ~1 µm can be clearly seen from the side- and top-view SEM micrographs in Fig. 6.6.



(a) (b)



(c)

Figure 6.6: (a,b) SEM micrographs of two NCD films overgrown in 2D (a) and 3D (b) to the same thickness of ~1 µm. (c) Average in-plane grain size versus film thickness. The transition from single crystallites to columnar grains takes place in the 1st micron of material, as the change of slope from γ_1 to γ_2 shows.

In the graph of Fig. 6.6c a linear interpolation of the experimental points for the 2D/columnar-structured films is also indicated, which is based on a linear relationship between the in-plane dimension of the grains d and the film thickness z: $d(z) = d_0 + \gamma z$. The γ-parameter in the formula, which can be estimated from the slope of the interpolating line, describes the pace at which the in-plane dimensions of the grains grow with thickness, and thus is it also referred to as *spatial grain-size gradient* [176]. It is worth noticing that after an initial phase of fast in-plane growth in the *transition region* (characterized by a spatial grain-size gradient γ_1) at a film thickness of approximately 1 µm the rate with which the grains grow laterally started to reduce significantly, most probably due to re-nucleation phenomena. During the outgrowth new grains start to form and compete with the ones which have developed from the initial nuclei, such that after a certain thickness the in-plane dimensions of the grains increase only slightly, with smaller gradient γ_2. Since in this part of the film the growth continues mostly along the out-of-plane direction, with cylinder-like columns, we call this the *columnar region*. The distance from the substrate at which the two trend lines intersect may vary according to γ_1, whose value depends on factors such as nucleation density, initial grain size at the interface with the substrate and α-parameter.

By properly controlling these factors during the deposition process, NCD films could be grown, which have a thinner transition layer with larger columns in close proximity of the interface with the substrate, and thus potentially lower thermal resistance. For instance, further experiments in which the outgrowth step was performed with a lower methane concentration of 0.3% showed a steeper increase of the in-plane size of the grains (i. e. a higher γ_1) in the first µm, with d of ~300 nm already at a thickness of ~3 µm (while with 0.4% a similar size was reached at 8 µm, see Fig. 6.6c).

However, lower methane concentrations imply lower growth rates, and hence longer deposition times for films of the same thickness. Furthermore, a film with larger grains has also a higher built-in stress due to a reduction in the density of grain boundaries, across which stress relaxation normally takes place. When coating HEMT devices with diamond, the stress component has to be taken into account since it could have detrimental effects on the electric performances of the device (e. g. by altering the piezo polarization) and it may even damage the gate contact, as discussed in Chapter 7, where GaN HEMTs were coated with more than 2 µm of NCD.

In addition to driving the grain development towards a 2D mode, growing the film at low methane concentrations and high temperatures has a series of relevant consequences on its crystalline quality, as discussed in the following.

6.3.2 *The role of methane concentration on the phase purity*

The amount of carbon radicals above the substrate surface depends on the concentration of methane in the hydrogen atmosphere, which therefore affects primarily the carbon deposition rate on the substrate [192]. However, as reported in [193], the methane concentration affects also the amount of atomic hydrogen present in the reactor chamber at a given filament temperature. The higher the methane concentration, the lower the atomic hydrogen content in the growth environment, because of the higher recombination rate between hydrogen and carbon radicals.

At high methane concentrations the decrease of atomic hydrogen leads to a low efficiency of graphite etching, which results in a high density of defects and non-diamond phases in the diamond layer. Defects and graphitic clusters can in turn promote diamond re-nucleation, hence interrupting the growth of a diamond grain (either in the in-plane or in the out-of-plane direction).

Therefore, the methane concentration affects not only the diamond growth rate and maximum size of the diamond crystals, but also the phase purity and the amount of grain boundaries in the NCD layer.

The crystalline quality of three NCD samples (*M1,M2,M3*) outgrown to a total thickness of 3 μm with different methane concentrations[2] (respectively 0.3, 0.6 and 1.5%) was evaluated by Raman spectroscopy and correlated with the film surface morphology by M. Dipalo in [158] (see Figure 6.7).

The decrease in grain size with increasing methane concentration is evident from the SEM pictures of Figure 6.7, where the average grain size passes from 300 nm of sample *M1*, to 50 nm of sample *M3*. It is interesting to note that, even though the grains are randomly oriented, samples *M1* and *M2* show a preferential growth orientation, respectively <110> and <100>. This orientation transition (already reported by Janischowsky *et al.* [194]), is in agreement with the α-parameter model described in Section 4.6.

The Raman spectra of samples *M1, M2 and M3* obtained by using a green laser (514 nm wavelength) as light source are shown on the right side of Figure 6.7, where the characteristic diamond shift peak at 1332 cm^{-1} is indicated.

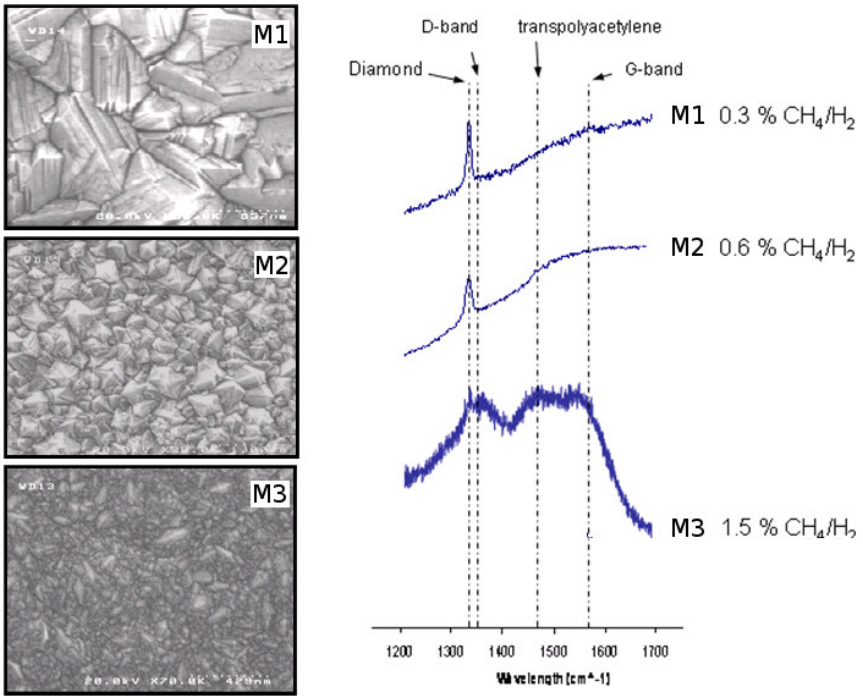


Figure 6.7: (left) Morphology at SEM of the samples overgrown with different methane concentrations; (right) correspondent green Raman spectra (from [158]).

2 Details are reported in Table 6.2.

Samples *M1* and *M2* show a similar spectrum with a pronounced diamond peak and the presence of the G-band at 1580 cm^{-1}, which is characteristic of the graphitic content; the additional shoulder at 1480 cm^{-1} is related to transpolyacetylene [195]. The diamond peak of sample *M1* is sharper and more intense than the one of sample *M2* because of the smaller grain boundary density. The diamond peak is only slightly appreciable for sample *M3*, the reason being the pronounced rising of the D-band at 1355 cm^{-1} due to the decrease of grain size. The D-band is in fact shown to be related to small size graphite clusters, which in turn are found to be present in NCD with small grain size [196]; the higher intensity of the D-band peak is therefore an indication of higher content of graphitic phases in the grain boundaries of the NCD layer. Sample *M3* also features sharper G-band and transpolyacetylene peaks.

6.3.3 *The role of substrate temperature on the phase purity*

A similar experiment was conducted to analyze the impact of the substrate temperature on the crystalline quality. Here, three NCD samples (*T1*,*T2*,*T3*) outgrown to a total thickness of 1 µm at low methane concentration[3], but at different substrate temperatures (respectively 650, 700 and 750 °C) were characterized by Raman spectroscopy and the results were correlated with their surface morphology.

The SEM micrographs in Figure 6.8, taken at the same magnification, highlight the change in size and shape of the grains induced by the different deposition temperatures. Whereas sample *T1*, grown at 650 °C, has grains in the order of 100 nm randomly oriented, sample *T3*, grown at 750 °C, has grains nearly double the size with a preferential <100> orientation.

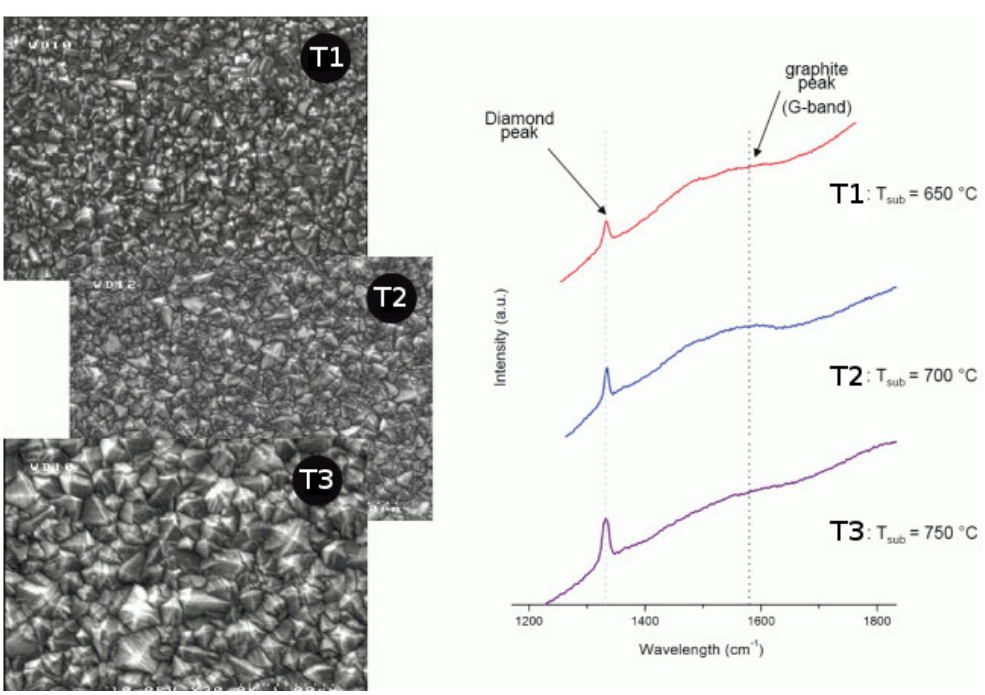


Figure 6.8: (left) Morphology at SEM of the samples overgrown at different substrate temperatures; (right) correspondent green Raman spectra.

3 Details are reported in Table 6.2.

Table 6.2: Details of the recipes adopted for the growth of the NCD films characterized by Raman sprectroscopy.

sample[*]	CH_4/H_2 (%)	T_{sub}(°C)	P_{cvd} (kPa)	thk (μm)
M1	0.3	810	2.0	3
M2	0.6	810	2.0	3
M3	1.5	810	2.0	3
T1	0.4	650	1.5	1
T2	0.4	700	1.5	1
T3	0.4	750	1.5	1

[*] $T_{fil} = 2150\,°C$ for all the samples.

Although the main features of NCD films, namely the diamond peak at 1332 cm^{-1} and the graphite G-band at 1580 cm^{-1}, are clearly visible in all the Raman spectra shown in Figure 6.8, differences in intensity exist among the samples. For instance, *T1* and *T2* have a G-band of similar shape and intensity, but the diamond peak is sharper and higher for *T2*, because of the lower density of grain boundaries.

T3's diamond peak has the highest intensity of the three and the G-band is only slightly appreciable, both indicating the film has lower graphite content than *T1* and *T2* and thus higher purity of the diamond phase. Furthermore, the transpolyacetylene band at 1480 cm^{-1}, well recognizable in the spectra of *T1* and *T2*, is only barely visible for *T3*.

Summary

The results of the experiments described in the previous sections point out how controlling methane concentration and substrate temperature during the outgrowth stage allows fine control over the NCD film microstructure both in terms of shape of the crystals (i.e. spherical or columnar) and size, as well as in terms of non-diamond components embedded in the layer (i.e. graphite content and grain boundary density).

The analysis of the microstructure performed by means of SEM/AFM microscropy on NCD films grown by *HFCVD* with different methane concentrations indicated that for methane content below 1% in H2 and substrate temperatures above 650 °C the film develops a 2D/columnar structure. In this growth-mode the average in-plane dimensions of the grains depend on the film thickness and reach a few hundreds nanometers within the first microns of material. It also indicated that the lower the methane content and the higher the substrate temperature, the larger is the in-plane size of the grains in the transition region of the film (i. e. the higher is the γ-parameter), and the higher is their crystalline quality (as the analysis of the Raman spectra showed).

However, it is worth noting that a high crystalline quality comes at the price of a low deposition rate; moreover, the NCD film will be grown directly on top of a GaN

HEMT, which could be damaged by an excessive heat load and a prolonged exposure to the H-rich atmosphere in the CVD reactor.

In the current work a deposition recipe with 0.4% concentration of methane in hydrogen at a substrate temperature of 750 °C was chosen as best trade-off between crystalline quality, growth rate (~0.1 μm/hour) and thermal budget applied to the device. The NCD films outgrown with such a recipe exhibit a columnar structure with grains of high crystalline purity, whose average in-plane dimensions reach ~150–200 nm within the first micron of material.

7

DIAMOND-COATED GAN HEMTS

As discussed in the introduction and in Chapter 3, diamond can be integrated with GaN-based electronics in several configurations, all aimed at mitigating the self-heating-effect. Among the proposed solutions, a NCD cap layer directly deposited on top of the device passivation is at the same time the most attractive and the most challenging one. On one hand in fact, with its high thermal conductivity, a NCD thin film as top heat-spreading layer would provide a path of low thermal resistance close to the hot-spot of the device, separated only by the device passivation. On the other hand, the conditions in which diamond deposition is carried out are extremely harsh for the device, with high risk of damage while depositing the NCD overcoat.

This chapter will describe the technical approach, which allowed to coat fully processed InAlN/GaN HEMTs with NCD films, and will cover in detail the strategies adopted to improve the thermal stability of each component of the HEMT structure such that it could withstand the diamond deposition process. The work here presented is the result of the close collaboration between the GaN technology group (F. Medjdoub, M. Alomari and D. Maier) and the diamond growth group (M. Dipalo, Z. Gao and S. Rossi) of our institute, which spanned several years. Discussed here are the optimization results relevant to HEMT overgrowth; further details on the high temperature stability and operation of InAlN/GaN-based HEMTs can be found in [75, 74, 22, 73].

7.1 DEVELOPMENT OF NCD-CAPPED HEMT DEVICES

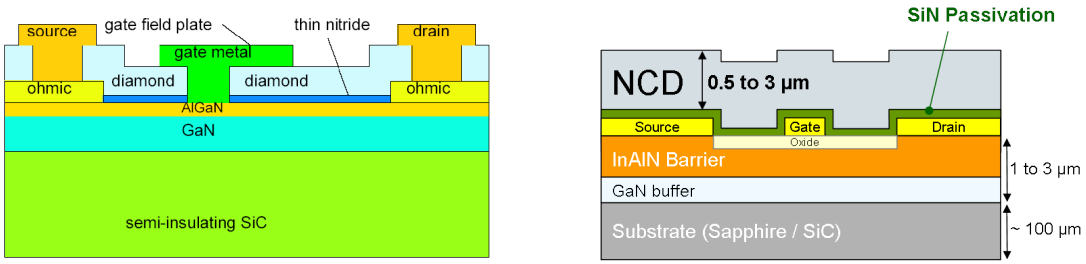
Diamond overgrowth on top of AlGaN/GaN FETs for the purpose of local heat spreading was originally proposed in 1991 by S. Rotter [197] and was attempted for the first time in 2001 by Seelmann-Eggebert and coworkers [31]. They coated a fully-processed HEMT including the Schottky gate contact with CVD diamond deposited at a temperature below 500 °C. Although such a low temperature allowed to avoid the decomposition of the GaN buffer, which is likely to happen above 600 °C [198] if the layer is not adequately protected, and to maintain a reasonable gate contact quality, it also sacrificed NCD crystalline quality, and thus its thermal conductivity.

In 2010 Tadjer et al. [123] overgrew AlGaN/GaN HEMTs with 0.5 µm NCD at 750 °C following a "diamond-before-gate" approach, i. e. by depositing the NCD heat-spreading film prior to HEMT gate fabrication, which was subsequently evaporated in a recess etched into the diamond film (see Figure 7.1a). In this way, thermal damage to the device contacts was minimized and functional devices were obtained, whose channel temperature was ~20% lower compared to an un-capped control device, even without a top heat-sink. The challenge in this approach lies in the difficulty to etch micrometer-thick diamond layers with high resolution in the sub-micron range. This will limit the gate length, which can be implemented. In addition, care has to be taken

when etching the diamond not to induce any damage to the underlying surface of the barrier layer.

Our approach adopts Seelmann-Eggebert's concept of coating the gated-HEMT with NCD and focuses on improving the thermal stability of the complete device so that it could withstand a diamond deposition process performed at 750 °C. The sketch of the diamond-coated HEMT structure is shown in Figure 7.1b, where the thin native oxide formed by thermal oxidation at 800 °C is also indicated. The oxidation step prior to the gate formation is part of our standard processing routine, since it allows the realization of a high thermally stable Schottky contact, which is crucial to enable the high temperature operation of InAlN/GaN-based HEMTs (as discussed in Section 2.4.3 and in the work of Maier *et al.* [74]).

The main processing challenge for the realization of such a NCD-coated HEMT is to fabricate a device, whose functionality is preserved after prolonged diamond growth carried out at high temperature in a highly reducing (H* rich) atmosphere. In fact, since a nanodiamond film of high crystalline quality is grown at rates of approx. 0.1 µm/h in our HFCVD reactor, the thermal budget acting on the device structure will be 750 °C × 10 hours for 1 µm overgrowth and ~50 hours (i. e. approx. 3 days) for a 5 µm NCD film. This budget has then to be tolerated by the GaN buffer and the heterostructure, the ohmic and blocking contacts, the passivation and nucleation layer, and by all the respective interfaces.



(a) (b)

Figure 7.1: Schematics of a NCD coated HEMT according to the fabrication procedure developed by Tadjer and coworkers at NRL (a) and in the current work (b).

The development of NCD-coated HEMTs presented here proceeded by means of diamond deposition experiments which aimed at verifying and improving the stability of each of the HEMT building blocks in several steps, following the complexity of FET device fabrication, namely:

1. overgrowth of the InAlN/GaN heterostructure coated with the interlayer stack, with FET fabrication after the removal of the NCD overlay – to test GaN buffer and heterostructure stability;

2. overgrowth of the InAlN/GaN heterostructure with TLM structures (i. e. without gate) and coated with the interlayer stack – to test the thermal stability of the metals forming the ohmic metallization stack;

3. overgrowth of the InAlN/GaN heterostructure with TLM structures and coated with different passivation layers – to test the high temperature behavior of the

dielectric used as passivation layer and the insulating properties of the interlayer stack;

4. overgrowth of InAlN/GaN fully-processed HEMTs coated with the interlayer stack – to optimize the gate metallization stack.

The interlayer stack consists of a thin dielectric layer (i. e. SiO_2, SiN or Al_2O_3), which protects the InAlN/GaN surface and serves as device passivation, and of a Si-based nucleation layer, which is needed in order to perform *BEN* on a foreign, insulating substrate (as explained in Section 4.7.1). This layer is an amorphous α-Si film, tens of nanometers thick, deposited by PECVD onto the HEMT passivation. Although undoped, its intrinsic electrical conductivity at high temperatures enables to provide bias to the sample surface. When thin enough, this layer is largely consumed during the *BEN* process by H-plasma etching, with the formation of silane, or by conversion to SiC (see Section 6.2), such that the interface remains electrically insulating.

InAlN/GaN heterostructures grown on sapphire and SiC substrates by several GaN research groups[1] were used as active material for these experiments.

7.1.1 *Heterostructure stability*

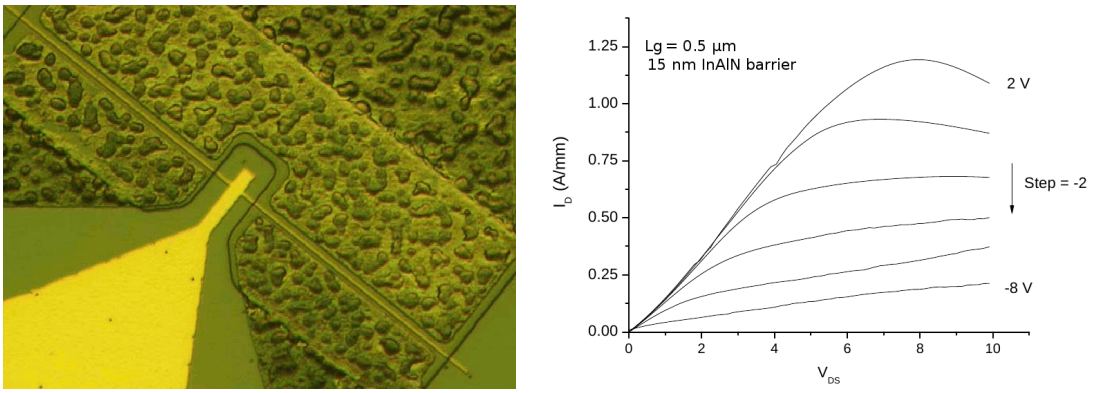
As shown in Section 2.4.3, the lattice-matched InAlN/GaN heterostructure is exceptionally stable at high temperature. However, to verify the heterostructure stability under the actual diamond growth conditions an experiment was designed, in which a thin NCD film was firstly deposited on a virgin InAlN/GaN wafer and then completely removed by plasma etching without removing the InAlN/GaN material. HEMT structures were subsequently fabricated to test the electrical performance of the heterostructure after the diamond growth process.

For this experiment unprocessed InAlN/GaN heterostructures on sapphire with 15 nm barrier were used. It is worth mentioning that the GaN buffer was not optimized for high electrical insulation. After coating the sample with a PECVD SiO_2/Si interlayer, the nucleation step and subsequent outgrowth of a 500 nm thick nanodiamond layer were performed (with a thermal budget of ~5 hours at 740 °C). After growth, the diamond film and the Si-based interlayers were removed by plasma etching, followed by the fabrication of the HEMT structure. The NCD film was etched in Ar/O_2, while the interlayer was etched in CF_4 plasma.

After the complete removal of the NCD film and interlayers, the InAlN/GaN was patterned by MESA etching in Ar plasma. Subsequently, ohmic contacts were deposited using a standard metal layers stack, comprising Ti/Ni/Al/Au, which was then annealed at 900 °C with a rapid thermal annealing (*RTA*); the channel dimensions were 3× 50 µm. At last, a 0.5 µm Ni/Au gate was deposited using e-beam lithography. In Figure 7.2 a photograph and the DC output characteristic of the device are shown.

Despite the high buffer leakage (related to the buffer material) the maximum output current density of 1.2 A/mm was identical to the one measured on control devices from the same wafer, thus indicating that the polarization of the heterostructure was entirely preserved.

1 Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland; Alcatel Thales III-V lab, Marcoussis, France; Aixtron, Aachen, Germany.



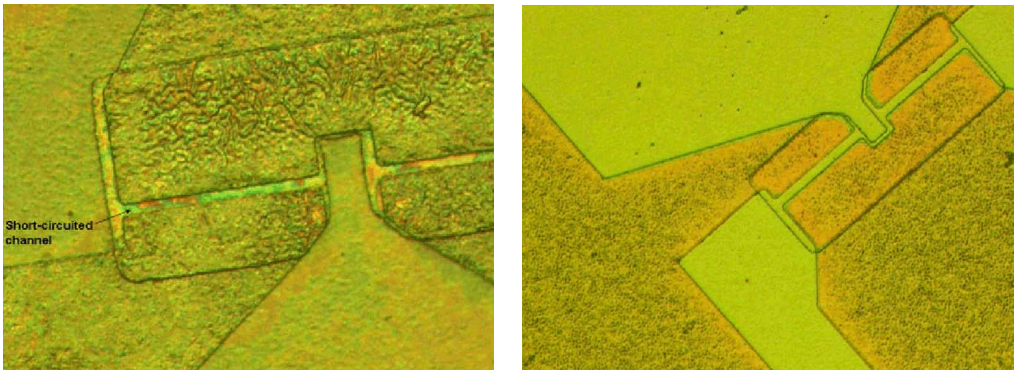
(a) (b)

Figure 7.2: (a) Micrograph and (b) output characteristic of the HEMT fabricated after overgrowth of the InAlN/GaN heterostructure with NCD and its removal.

7.1.2 *Metallization stability*

After the assessment of heterostructure stability in the harsh conditions of diamond deposition, we turned our attention to the ohmic and gate contacts.

The ohmic contacts commonly used in GaN-based electronics consist of a stack of metals (Ti/Al/Ni/Au) optimized for low contact resistance, rather than for high temperature operation or storage. Diamond overgrowth experiments performed on gateless HEMTs using this type of ohmic contacts showed a poor thermal stability of the stack already after 2 hours of BEN, with an overflow of metal taking place during the subsequent growth step (3 hours), which resulted in short-circuit between the source and drain contacts (Fig. 7.3a).

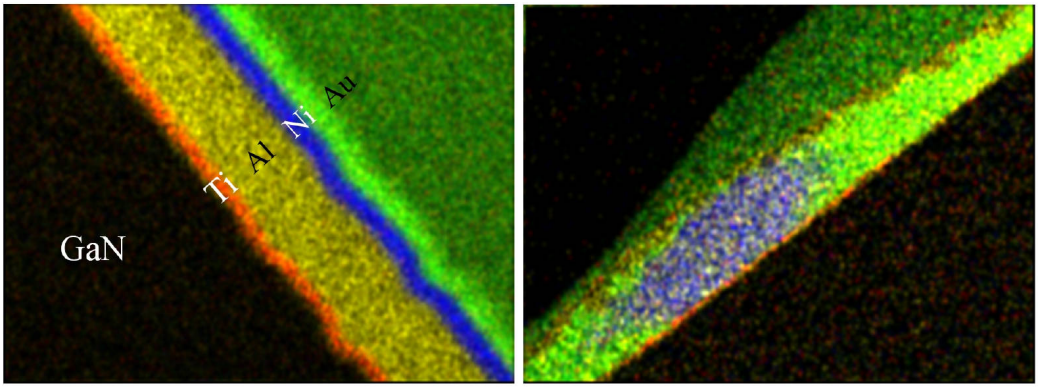


(a) Au (b) Au-free

Figure 7.3: Effect of NCD growth on ohmic contacts containing Au (a) and Au-free with Ta cap.

The experiments reported in Section 2.4.3 on storage/operation at high temperature showed that an excess of non-alloyed Au is the main cause of contact degradation, although also Al, which has the lowest melting temperature among the used metals (680 °C), could be affected by the same problem. During diamond deposition, the high thermal budget combined with a harsh environment rich of H-radicals accelerates

a degradation process, which starts already during the high temperature anneal in the RTA system (see TEM[2] in Figure 7.4), with inter-mixing of the four metals and segregation of non-alloyed Au.



(a) (b)

Figure 7.4: TEM color-coded elemental maps of the ohmic contact stack (a) before and (b) after annealing at 850 °C for 30 seconds. Ti largely remains at the interface with the HEMT, while Al spreads everywhere. Au and Ni tend to segregate causing an excess of non alloyed metal which could later out-diffuse at high temperatures (in particular if ductile, like Au.)

To overcome this problem the Al thickness was reduced from 200 nm to 100 nm, and the Au layer was replaced by a top 25 nm tantalum layer, which is less ductile and protects the Ni surface from oxidation. Tantalum has a very high melting point (~3000 °C) and is commonly used as diffusion barrier in high temperature processes; however it has a high contact resistance R_c. The ohmic contact layers stack was then Ti/Al/Ni/Ta (15/100/40/25 nm thick).

The removal of Au from the stack allowed diamond overgrowth without degradation of the ohmic contacts, which presented sharp edges and no sign of short-circuit (see Figure 7.3b). Overgrowth tests on devices with Cu/Ta and Cu/Pt capping showed that these metals are equally suitable to encapsulate and protect the Ti/Al/Ni stack.

A similar strategy was adopted for the gate contact, where substituting the standard Ni/Au metallization with Cu, or refractory metals molybdenum and tantalum, allowed fully fabricated HEMT structures to be coated with NCD (see Section 7.2).

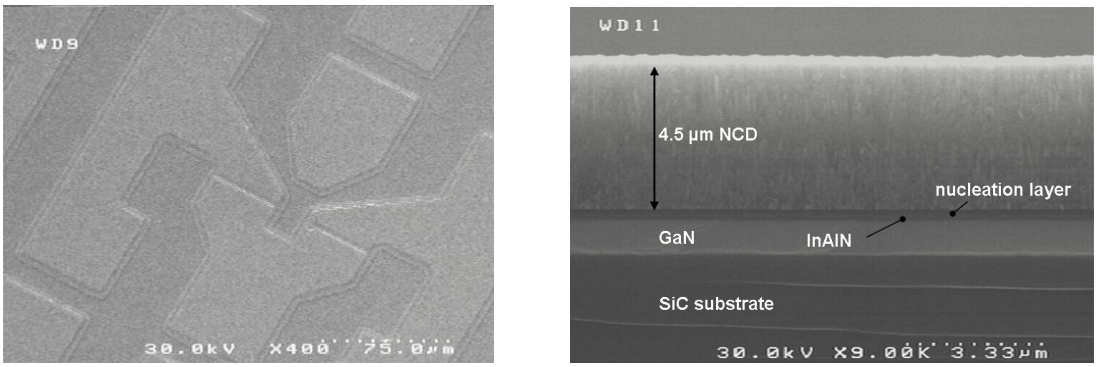
7.1.3 *NCD coating of gate-less HEMTs*

To ascertain the thermal stability of the ohmic contact scheme developed in Section 7.1.2 to the prolonged thermal stress of diamond deposition, diamond overgrowth experiments were conducted firstly on gate-less HEMT structures.

The HEMT devices used in these experiments were fabricated on a 10 nm InAlN/-GaN heterostructure on SiC substrate by using the optimized, Au-free, Ti/Al/Ni/Ta ohmic contacts stack and a SiO2 passivation. The NCD capping layer was overgrown stepwise to a total thickness of 4.5 µm, periodically interrupting the growth to monitor the 2DEG channel current density.

2 performed at the department of Electron Microscopy, Ulm.

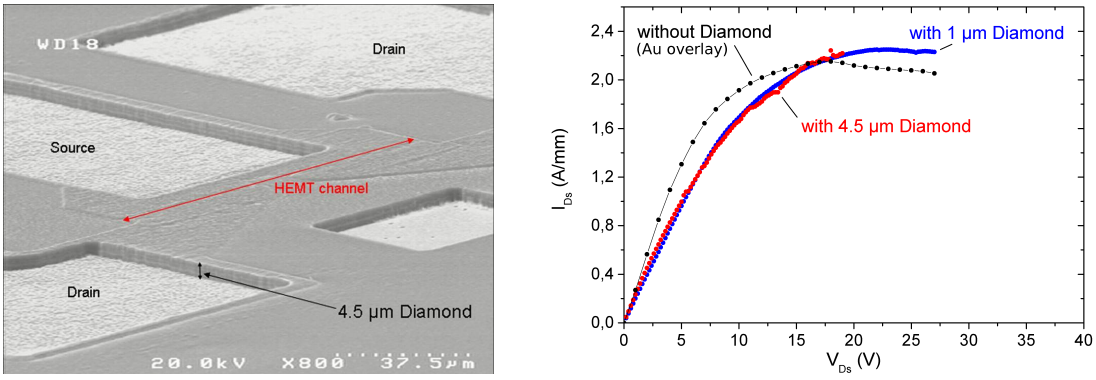
The surface morphology and cross section of the InAlN/GaN device after NCD growth are illustrated in the SEM images of Figure 7.5, taken after 43 hrs of overgrowth at 750 °C. The pictures show that the InAlN barrier, the GaN buffer and the ohmic contacts are homogeneously covered by a conformal diamond layer, which preserves the sharpness of the edges and shows neither cracks or bubbling. Moreover, the ohmic contacts showed no structural degradation despite the long growth time at high temperature and repeated thermal cycling.



(a) (b)

Figure 7.5: SEM images of 4.5 µm NCD overgrowth on gateless InAlN/GaN HEMT: (a) showing that the diamond growth was conformal and homogeneous across the sample and that the ohmic contacts were stable during the growth process. (b) Cross section of the heterostructure and the diamond layer.

As can be seen in Figure 7.6, where the DC output characteristics of the overgrown ungated HEMT and a reference device fabricated on the same InAlN/GaN layer with standard process are plotted, the full current density of around 2 A/mm could be maintained after growth of 1 µm and also after growth had continued to 4.5 µm. The increase in the access resistance of the overgrown HEMTs is due to the higher



(a) (b)

Figure 7.6: (a) SEM micrograph of the gate-less InAlN/GaN HEMT structures after diamond growth and contact pads etching by O-plasma; (b) DC-characteristics of the HEMT before and after the growth of 1 and 4.5 µm of NCD compared to a reference device from the same wafer.

resistivity of the Ta ohmic contact cap layer compared to the Au top layer of the control sample.

7.1.4 *Passivation stability*

For the initial attempts to overgrow GaN-based HEMTs with nanocrystalline diamond, we adopted a thin PECVD-deposited SiO_2 film (100–150 nm thick) as dielectric for passivating the device prior to diamond growth. Such a passivation proved to be highly thermally stable during the diamond overgrowth, as reported in [199] by Irwin and coworkers, who proved that nucleation of diamond on amorphous SiO_2 surfaces is promoted by formation of a SiC surface layer. Indeed, we were able to coat gate-less as well as fully processed SiO_2-passivated InAlN/GaN HEMTs with µm-thick NCD layers (as shown later in this chapter).

However, in this work the stability of other passivation schemes was also investigated by means of overgrowth experiments, where the SiO_2 layer was replaced by another dielectric, namely:

A. silicon nitride, PECVD-deposited (Si_xN_y);

B. silicon oxy-nitride, PECVD-deposited;

C. silicon nitride, deposited in-situ (Si_3N_4);

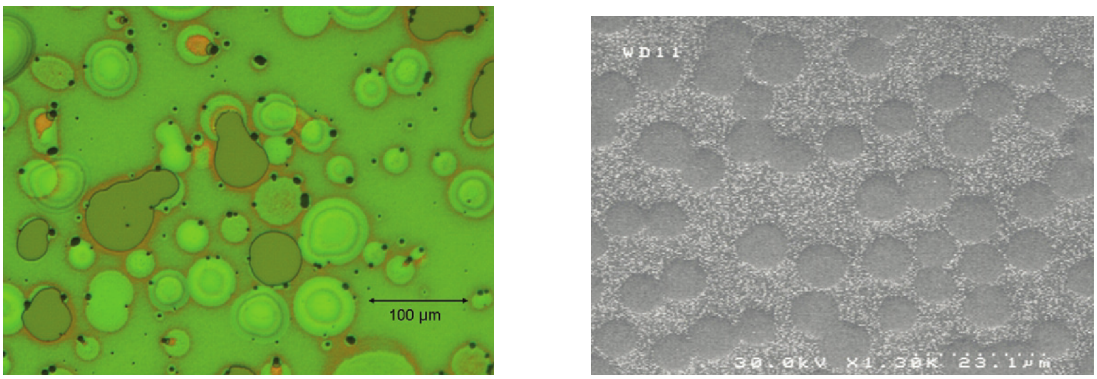
D. Al_2O_3, ALD-deposited.

Silicon nitride is currently the dielectric of choice for the passivation of GaN HEMTs, while a thin Al_2O_3 layer (5 to 15 nm) could be particularly suitable as passivation for the MOS-HEMT configuration discussed in Chapter 2. In addition, such passivation schemes are attractive under the thermal point of view, since SiO_2 thermal conductivity is very low, especially for thin amorphous layers in the tens/hundreds of nm range, which have k values below 1 $Wm^{-1}K^{-1}$ [200, 201].

PECVD-deposited silicon nitride (Si_xN_y)

Traditionally, surface passivation of GaN-based HEMTs is performed by means of a thin *PECVD*-deposited Si_xN_y layer. It applies also to our standard HEMT fabrication routine, as described in section 2.4.2. However, first experiments of diamond overgrowth on top of an interlayers stack consisting of Si_xN_y/α-Si (100/100 nm) both deposited by PECVD, were not successful and resulted in the formation of bubbles after the nucleation step, which indicated outgasing from one of the materials of the stack (see Figure 7.7). In the regions where outgasing took place the diamond nuclei could not be outgrown to a coalescent layer, even after a subsequent growth cycle lasting for several hours. At first it was not clear whether both the Si_xN_y and the α-Si were the source of outgasing, or if the top Si layer acted as non-transparent cap to the outgasing flux originating from the underlying silicon nitride film.

The two films are normally deposited sequentially in the same PECVD reactor at 300 °C from gas precursors $SiH_4/NH_3/N_2$ (for Si_xN_y) or SiH_4 (for α-Si) according to the parameters listed in Table 7.1, where the silicon nitride layer is labeled as *reference*-Si_xN_y.



(a) (b)

Figure 7.7: (a) Optical image of a Si_xN_y-based interlayer after nucleation, where bubble-like rupture appeared and (b) SEM images indicating that nucleation does not occur uniformly due to removal of the nucleation layer/passivation where the rupture occurred.

Unlike silicon nitride films deposited at high temperature, plasma nitride films grown at low temperatures (200–400 °C) are not a stoichiometric Si3N4 compound, but incorporate large concentrations of hydrogen [202]. In fact, due to the low preparation temperature, the decomposition of the hydrogen-containing molecules is not complete, and Si- as well as N-bonded H is embedded in the PECVD-deposited layers. The state in which hydrogen is incorporated and its concentration depend on the details of the plasma deposition conditions (i. e. gas-phase compositions, temperatures and radio frequencies). In nitrogen-rich films most of the hydrogen is bonded to nitrogen, whereas for nitrogen-poor films most of the incorporated H is found in Si-H configurations [202].

Spectroscopic analysis of such films deposited at 300 °C with SiH4/NH3/N2 precursors showed that the concentration of molecular-bonded hydrogen is of approx. 25–30 at.% [203]. It is therefore very likely that the high temperature and the high density of H-radicals present in the diamond reactor during the diamond deposition process triggered the out-diffusion of such H-containing molecules, thus leaving blisters in the silicon nitride film.

To address the problem, two alternative approaches were followed, namely:

A. annealing the sample passivated with the *reference*-Si_xN_y for 2 hrs at 700 °C in vacuum or N2 prior to the diamond nucleation step, in order to allow the outgasing of excess hydrogen from the silicon nitride layer;

B. modify the silicon nitride deposition process, removing NH3 as nitrogen precursor in favor of higher content of N2, and increasing the deposition temperature to 340 °C (process recipe labeled *NH3-free* Si_xN_y[3]).

While approach (A) focuses on enhancing the stability of the silicon nitride film by means of a post-deposition thermal treatment, the silicon nitride layer of approach (B) is, as-deposited, less rich of molecular-bonded hydrogen due to the removal of the NH3 precursor.

3 Details are reported in Table 7.1.

A virgin InAlN/GaN heterostructure was used in this experiment. Diamond nucleation by BEN was performed for 2 hrs at 750 °C on samples coated with *reference*-Si_xN_y, previously annealed, and on samples with *NH3-free* Si_xN_y.

While the samples with *reference*-Si_xN_y did not show any improvement over the non-annealed ones, exhibiting the same characteristic bubbles after the BEN step, nuleation was instead successful on the samples passivated with *NH3-free* Si_xN_y, with no sign of uncontrolled hydrogen outdiffusion and with a uniform, high nucleation density of $1 \cdot 10^{11}$ cm^{-2} which allowed a continuous, crack-free NCD film to be grown.

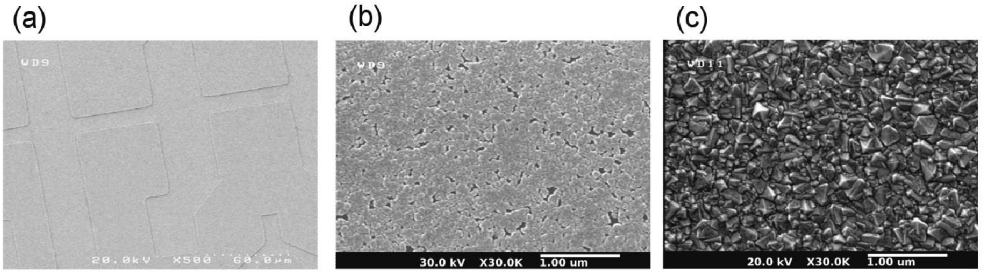


Figure 7.8: (a,b) SEM micrographs of the Si/Si_xN_y nucleated surface at different magnifications; (c) SEM image of the surface after 300 nm diamond overgrowth.

Figure 7.8 shows SEM images of one of these samples after the diamond nucleation step and after subsequent 300 nm nanodiamond outgrowth (3 hrs at 750 °C).

The outcome of these experiments led to an important conclusion: the excess of molecular-bonded hydrogen in the as-deposited films can not be removed sufficiently by a post-deposition thermal treatment (T<1000 °C) and does still present a problem during NCD nucleation and growth. Hence initial low hydrogen content in the as-deposited passivation films is critical for these layers to withstand the NCD growth process.

Furthermore, these experiments indicate that the thermal stability of any dielectric film at temperatures similar to the NCD growth temperature is a necessary, but not a sufficient criterion to indicate stability under actual NCD nucleation and outgrowth conditions (where, besides the high temperature, the sample surface is exposed also to an atmosphere rich of H-radicals and methane).

PECVD-deposited silicon oxy-nitride (SiO_xNy*)*

The thermal stability issues affecting the *reference*-Si_xN_y spurred intense work on the PECVD deposition process, as discussed above.

A different way of depositing silicon nitride films in a PECVD equipment is by using nitrous oxide (N2O), nitrogen (N2) and silane (SiH4) as precursor gases. The addition of N2O would allow the excess Si to bond to O-radicals generated during break-up of the N2O molecule. The result is a silicon oxy-nitride (SiO_xN_y) (*SiON*) film, SiO_xN_y, whose stoichiometry can be varied from silicon dioxide ($y = 0\%$) to silicon nitride ($x = 0\%$), by properly setting the gas flow ratio [204, 202].

Silicon oxy-nitride layers deposited at 340 °C on virgin heterostructures according to the recipe reported in Table 7.1 were able to withstand diamond growth conditions without developing bubbles. The value of 1.8 for the film's refractive index, which is

Table 7.1: Details of the recipes used to deposit silicon nitride films in the PECVD reactor.

parameters	*reference*-Si_xN_y [1]	*NH3-free* Si_xN_y [2]	SiO_xN_y [2]
SiH4 (2% in He)	800	120	400
NH3	20	-	-
N2	250	900	250
N2O	-	-	500
T_{sub} (°C)	300	340	340
P_{CVD}(Torr)	1.0	0.6	0.5
RF power (W)	25	40	40
refractive index (1.4 for SiO2)	1.9	1.9	1.8

[1] Unstable in NCD growth conditions.
[2] Stable in NCD growth conditions.

close to 1.9 obtained for stoichiometric silicon nitride, indicates that the silicon oxynitride acts like oxygen-rich silicon nitride. This feature proved to be of fundamental importance in the overgrowth of fully-processed HEMTs with thick diamond layers, as discussed in a later section, but further work is required in order to understand whether N2O has any effect on the InAlN surface in the initial stage of the deposition in the PECVD chamber.

In-situ silicon nitride (Si_3N_4*)*

In-situ silicon nitride layers are deposited at temperatures of ~800–900 °C in the same reactor chamber where the III-Nitride heterostructures are grown, immediately after the barrier layer growth [54, 205, 206], and thus before the contacts are made.

The advantages of silicon nitride films deposited at such high temperatures are twofold. On one hand, the high temperature allows to efficiently break the N-H molecules contained in the NH3 precursor, such that in-situ silicon nitride layers contain as-deposited only ~3% of hydrogen [54], which is a concentration at least 10 times lower than the one found in layers prepared ex-situ at low temperature by PECVD. In addition, any outgasing phenomena may happen only when the film is heated above the deposition temperature, hence in-situ silicon nitride layers are thermally stable, without any phase transformation in a range, which may extend up to ~900 °C.

To ascertain the thermal stability of such a passivation, NCD overgrowth tests were performed on samples diced from a 2" SiC wafer with a $In_{0.15}Al_{0.85}N$/GaN heterostructure passivated by 30 nm in-situ Si_3N_4 grown at 800 °C using silane and ammonia precursors. The integrity of the passivation was evaluated after the NCD nucleation and overgrowth steps by means of surface analysis using optical and SEM microscopes. After a BEN treatment performed for 2 hours at 780 °C the passivation did not show any blistering or bubbling effect, such that closed films with typical NCD morphology (see Fig. 7.9) could be grown in the subsequent overgrowth step (3 hours at 740 °C) to a final thickness of 300 nm.

These first results proved that an in-situ silicon nitride passivation is intrinsically stable and able to withstand higher temperatures than traditional, ex-situ silicon nitride dielectric films, and thus it is more suitable for realizing NCD-coated HEMTs. In addition, in-situ-deposited Si_3N_4 films may exhibit high thermal conductivities and good dielectric properties even when just a few nanometers thick [207, 208], thus offering little thermal resistance to the heat extraction from the active area of the device.

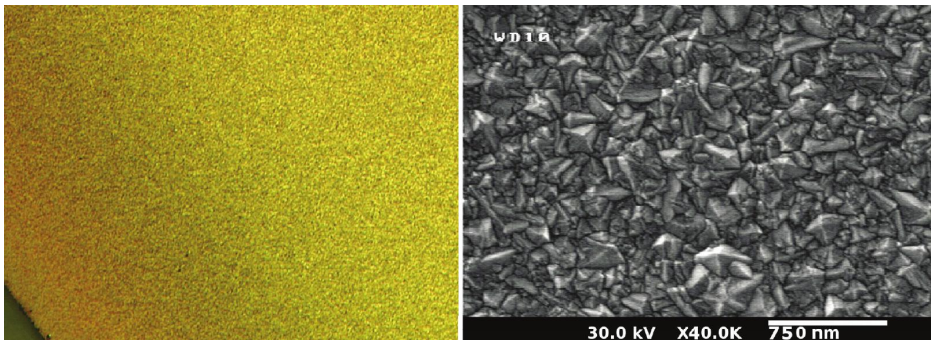


Figure 7.9: (left) Optical microscope image and (right) SEM image of InAlN/GaN heterostructure passivated with in-situ Si_3N_4 and overgrown with 300 nm NCD film.

ALD-deposited Al2O3

Thin layers of Al2O3 (5 to 15 nm) can be deposited by atomic layer deposition (*ALD*) to serve as device passivation for GaN-based HEMTs. In a MOS-HEMT configuration, such a layer can be a natural extension of the native oxide, which is grown at 800 °C and is α-Al2O3 (i. e. sapphire) [209]. *ALD*-deposited Al2O3 layers grown at temperatures of 200–300 °C are instead a metastable/amorphous phase of Al2O3, and hence undergo a phase transformation at the high temperatures used for the diamond growth, which may compromise the integrity of the film.

Once again, controlling the hydrogen content in the as-deposited film proved to be the key for the ALD-deposited Al2O3 passivation used in this work to survive the diamond deposition process. Indeed, experiments performed on a set of samples passivated with 15 nm ALD-deposited Al2O3 were initially unsuccessful, despite a post-deposition annealing treatment performed for 5 minutes at 500 °C in RTA. During the 2 hours of BEN at 720 °C, highly volatile gas evolution similar to the one observed for the *reference*-Si_xN_y was locally disrupting the film, thus preventing a closed, continuous diamond seed layer to be formed on the surface.

Only by modifying the AL2O3 deposition recipe it was possible to obtain films with as-deposited low hydrogen content, which were then able to withstand the conditions of diamond growth. For the new recipe, ozone (activated by UV light) was used as oxygen precursor [210] instead of water, which has the drawback of being also a hydrogen carrier.

First experiments of NCD nucleation and growth using this modified recipe were encouraging, with no blistering and homogeneous growth over the whole surface of the sample. Figure 7.10a shows the optical image of a sample passivated with 10 nm of such Al2O3, taken after 2 hours of BEN at 750 °C. The SEM micrograph on the right shows the same sample after subsequent 10 hours at 750 °C, which were

necessary to outgrow 1 µm NCD. The improved thermal stability of the Al_2O_3 layer during the BEN and the outgrowth phases of the diamond deposition allowed the diamond nuclei to cover the surface with a high, uniform density of $\sim 1 \cdot 10^{11}$ cm^{-2} and a closed diamond film to be outgrown.

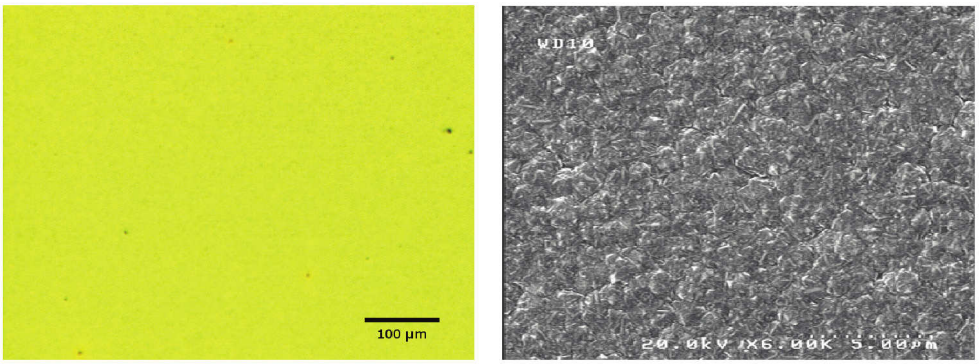


Figure 7.10: (left) Optical image of ALD-deposited Al_2O_3 using the new recipe; (right) SEM of the surface after 1 µm diamond overgrowth.

At this point all the key elements needed for the overgrowth of a working device, i. e. a thermally stable heterostructure and buffer, as well as robust contacts metallization and device passivation, are finally in place.

7.2 DIAMOND-COATED HEMTS

7.2.1 *NCD coating of fully processed HEMTs*

Following the encouraging results presented in the previous sections, the NCD overgrowth of fully processed HEMTs was attempted, initially with thin diamond films 0.5 µm thick not to stress the devices with the high thermal budget, which is necessary for thicker films.

HEMT with 0.5 µm NCD

Here an heterostructure with 7 nm InAlN barrier on GaN/SiC was used, which had channel charge density n_s of $1.67 \cdot 10^{13}$ cm^{-2} and sheet resistance R_{sh} of 365 Ω/□. For the fabrication of the HEMT, the stack Ti/Al/Ni/Cu was used for the ohmic contacts, Cu for the gate metallization, and 150 nm of SiO_2 were deposited as device passivation, since a highly-thermally stable Si_xN_y passivation was not yet available (see discussion in Sec. 7.1.4). The complete HEMT was coated with 150 nm of Si nucleation layer and subsequently nucleated and overgrown with 0.5 µm of diamond in 5 hrs at 770 °C. Figure 7.11 shows SEM images of the coated device.

No degradation in the DC output characteristics up to moderate drain bias levels was observable after diamond growth, as shown in Figure 7.12a, where the current values are largely identical before and after applying the diamond coating. Since neither the maximum channel current nor the pinch-off voltage changed essentially, we may argue that at the substrate side, the channel isolation and the GaN buffer layer properties were not degraded, as well as neither the interfacial polarization nor the barrier layer separation between channel and gate metal have changed. In

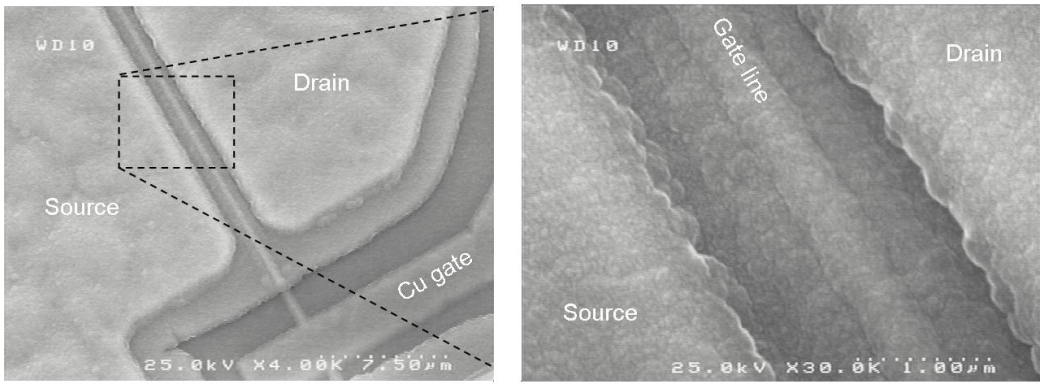


Figure 7.11: SEM images of 0.25×50 µm, 7 nm barrier HEMT coated with 0.5 µm diamond after the complete fabrication of the device.

addition, the unchanged on-resistance indicates that the source and drain contact resistances as well as the electrical potential of the free surface between the contacts did not change noticeably.

Concerning the RF performances, S-parameter measurements yielded cut-off frequencies of 4.2 and 5 GHz for f_t and f_{max} respectively (see Figure 7.12b). These relatively low values seem to be due to a high gate leakage in the RF-tested device, which may be ascribed to the presence of a residual α-Si film above the device passivation. The Si-based nucleation layer needed for the *BEN* stage of diamond deposition may indeed exhibit lossy dielectric properties when the device is operated at microwave frequencies, while having no influence on the DC output characteristics.

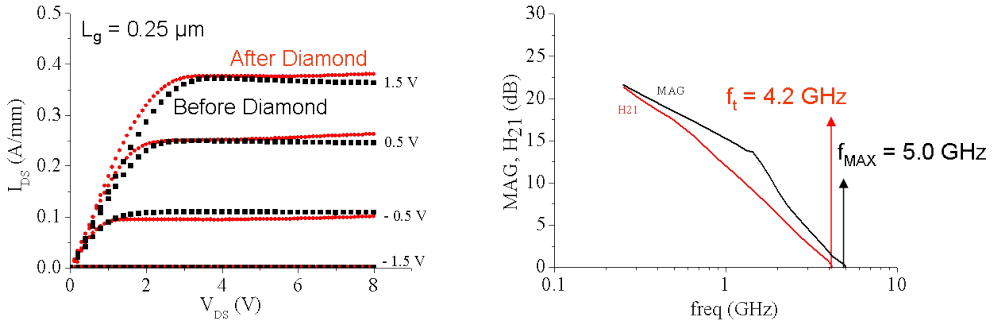


Figure 7.12: (left) HEMT DC characteristics before and after diamond overgrowth; (right) cut-off frequencies of the diamond overgrown device.

To test this hypothesis a thinner α-Si nucleation layer (50 nm instead of 150 nm) was used in the subsequent overgrowth experiments.

HEMT with 1 µm NCD

For the 1 µm overgrowth experiments of fully fabricated HEMT devices, the thermally stable, *NH3-free* Si_xN_y developed in Section 7.1.4 was used as passivation layer. In this case a heterostructure with 10 nm barrier on SiC was used, which had as-grown channel charge density and sheet resistance of $n_s = 2.76 \cdot 10^{13}\,cm^{-2}$ and

$R_{sh} = 199\,\Omega/\square$ respectively. A stack of Ti/Al/Ni/Pt (15/100/40/60 nm) annealed at 900 °C was used for the ohmic contacts, while the gate contact was Cu. The devices were passivated with 50 nm thick Si_xN_y and 50 nm of α-Si served as nucleation layer.

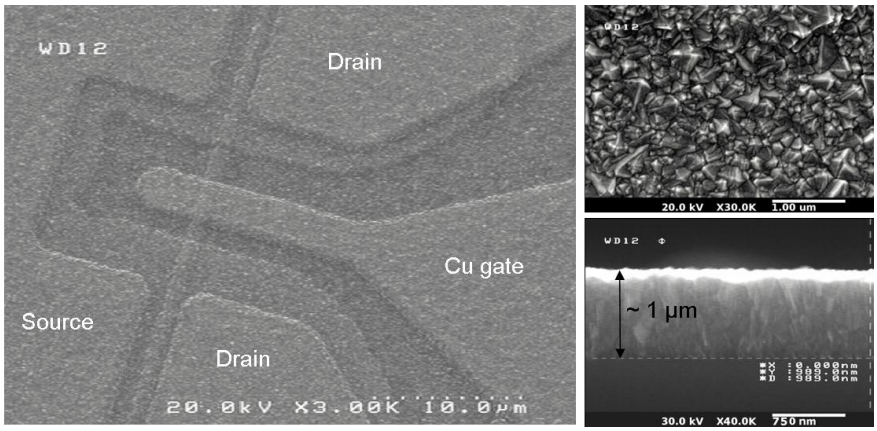


Figure 7.13: SEM images of 0.5×50 µm, 10 nm barrier HEMT coated with 1 µm NCD after the complete fabrication of the device; also shown a cross section of the NCD film.

After overgrowth with 1 µm of diamond (1:30 hrs BEN at 780 °C followed by 10 hours growth at 730 °C), the devices were still fully functional. Fig. 7.13 shows SEM images of the overgrown HEMT and a cross section of the 1 µm-thick diamond overlayer. The DC characteristics of the device before and after diamond overgrowth (Fig. 7.14a) are largely identical with no change in the maximum drain current density or in the pinch-off voltage.

The benefits of using a thinner α-Si nucleation layer and a Si_xN_y passivation instead of SiO2 are visible in the RF behavior of the coated devices, with higher cut-off frequencies of f_t=16.8 GHz and f_{max}= 6.4 GHz extracted from S-parameter measurements (Fig. 7.14b). The relatively low f_{max} is most likely due to a high resistive gate line and high on-resistances. Indeed, the Cu gate metallization is readily subject to oxidation, if not capped with Ta or Pt.

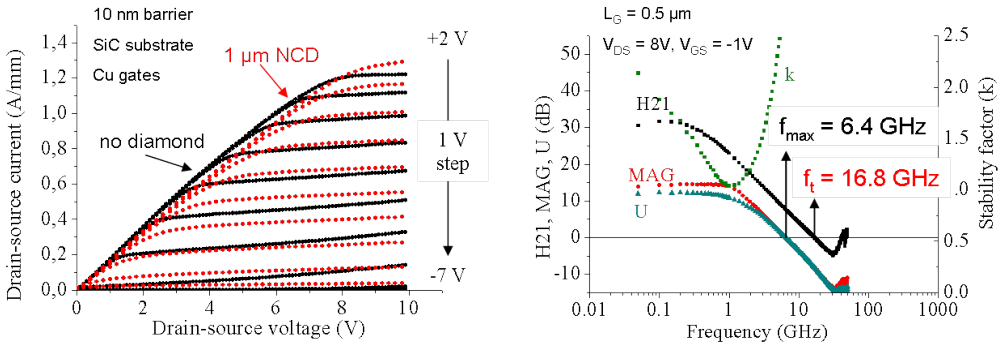


Figure 7.14: (left) HEMT DC characteristics before and after 1 µm diamond overgrowth; (right) cut-off frequencies of the diamond overgrown device.

HEMT with 2.8 µm NCD

After successfully coating HEMT devices with 1 µm of NCD, which required ~10 hours of growth at 750 °C, HEMT coating experiments were performed, in which the overgrowth time was extended to ~30 hours in the same conditions. Although after the overgrowth such devices did not show any damage at the optical inspection, when tested electrically, they either exhibited no current modulation by the gate, or in the best cases significant gate leakage currents. This could be due to degradation of the gate diode, caused by stress generated by the thicker NCD films, or by a degradation of the passivation layer due to long growth times at high temperature.

To test these hypotheses, the HEMT fabrication process was modified by replacing Cu with Mo in the gate metallization stack, and by substituting the Si_xN_y passivation with a silicon oxy-nitride[4] layer. Molybdenum has a higher melting temperature and lower thermal expansion coefficient than Cu, thus a Mo gate could have better chance to withstand the thermal budget of a long growth process and the mechanical stress induced by the diamond film upon cooling to room temperature. Concerning the passivation, the incorporation of oxygen in the nitride lattice for silicon oxynitride films leads to lower mechanical stress [211], which may hence improve their stability at high temperatures.

The designed fabrication process was tested on InAlN/GaN epi-layers with 10 nm barrier, on which HEMTs featuring Mo gates and 50 nm SiO_xN_y passivation were fabricated and subsequently coated with 2.8 µm of NCD in 25 hours at 750 °C (see Figure 7.15).

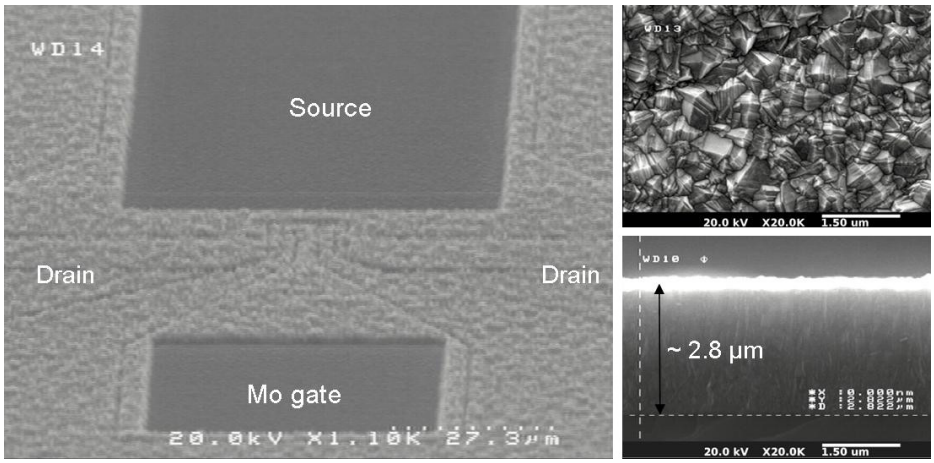


Figure 7.15: SEM micrographs of the HEMT coated with 2.8 µm of NCD taken after opening the pads, accompanied by top and cross-sectional views of the grown NCD layer.

From the DC characteristics (Figure 7.16) it can be seen that, although affected by leakage, these devices exhibited gate-controlled current modulation, with current saturation and an open channel current density similar to that of un-coated control devices.

The high leakage may be ascribed either to an early gate breakdown (resulting in an unmodulated channel, still with current saturation) or to the SiO_xN_y passivation, whose excess Si [211] is prone to react with the metals contained in the contacts stack during the diamond deposition, thus creating parallel conduction paths.

4 see Section 7.1.4 and Table 7.1 for details on the deposition recipe.

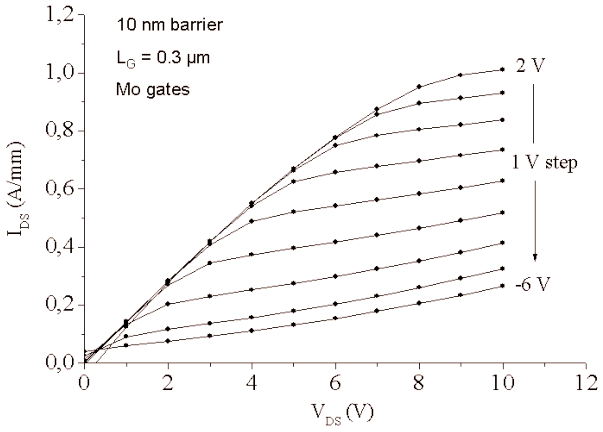


Figure 7.16: DC characteristics of the fully-fabricated HEMT coated with 2.8 µm NCD film.

Such an experiment indicates that controlling the stress, which develops within the diamond overcoat, is as important as assuring the thermal stability of all the HEMT structure components, when thick heat-spreading films need to be deposited onto fully processed HEMTs. It also indicated that HEMTs with a Mo gate and a SiO_xN_y passivation were able to (partially) cope with the thermal and mechanical stresses induced by nearly 3 µm of NCD overlay. But a further optimization of the fabrication process is certainly required for GaN-based HEMTs to be successfully coated with similar or even thicker diamond films.

8

THERMAL CHARACTERIZATION

In Chapter 7 the technological aspects crucial for the realization of *NCD*-coated HEMTs have been discussed, accompanied by the results of the electrical characterization of InAlN/GaN HEMT devices successfully overgrown with thin diamond films in the µm range. This chapter will deal with the thermal aspects of the direct-overgrowth approach, and will focus in particular on the thermal characterization of the *NCD* overlay.

Figure 8.1 depicts the cross-section of a NCD-coated HEMT, where the inset shows schematically the sequence of layers forming the overcoat. Assuming that a heat-sink is attached to the NCD side, the heat generated in the HEMT channel will flow towards the top of the device, crossing respectively:

1. the passivation layer (e. g. Si_xN_y),
2. the columnar-structured NCD film (with its nucleation/transition/columnar regions)

before reaching the ultimate heat-sink. Each of these layers has a thermal resistance R_i, which depends on the layer thermal conductivity k_i and on its thickness t_i, $R_i = t_i/k_i$.

As for the passivation layer, the smaller its thickness and the higher its thermal conductivity, the lower its thermal resistance will be. For instance, it would be preferable to use as device passivation a nm-thick in-situ Si_3N_4 layer, which is denser and has higher k than a PECVD-deposited Si_xN_y film, and which can be deposited pinholes-free even at thicknesses below 15 nm.

The α-Si nucleation layer, if not completely consumed during the *BEN* pre-treatment, will contribute with its thermal resistance. Therefore, as discussed in Section 4.7.1, it should not be thicker than ~25 nm. Such a thickness allows the Si layer to supply bias

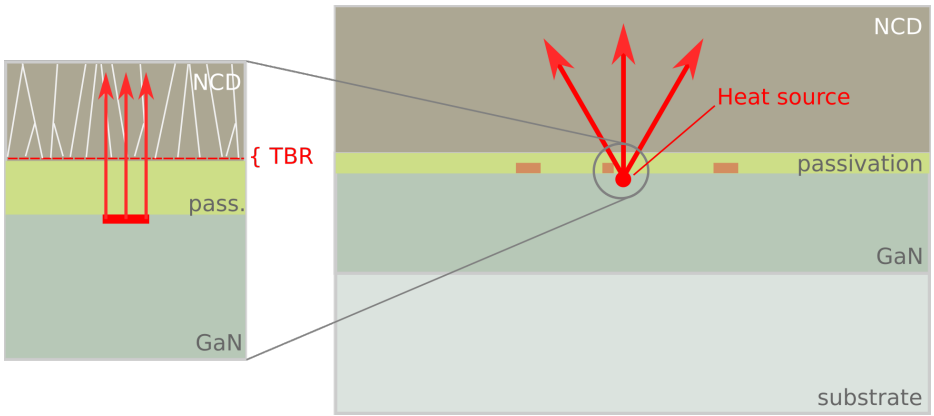


Figure 8.1: Schematic of the *NCD*-coated GaN HEMT, where the heat source in the channel is highlighted in red and the red lines indicate the direction of the heat flow. The inset on the left shows the path through the different layers coating the HEMT.

in the initial phase and to be completely consumed within the end of the nucleation process. Ideally, the lowest thermal resistance would be achieved by nucleating diamond directly on the InAlN surface, covered only with a ordered natural oxide of approx. 1.5 nm thickness.

As for the NCD film, the major contributions to the thermal resistance come from the thermal boundary resistance (R_{th}) (*TBR*) at the interface with the Si nucleation layer, and from the nucleation and transition regions of the film.

In the following, the thermal characterization of the NCD overcoat will be carried out by studying the heat transport in *test-structures* in which the NCD film is deposited on a virgin crystalline Si wafer (instead of on a HEMT) and is heated up by top metal heaters deposited on the NCD surface (instead of being heated-up from the bottom by the heat generated in the HEMT channel). On one hand such a structure simplifies the complicated task of extracting the thermal properties of the NCD film, which, due to its internal microstructure, is a strongly anisotropic material, with a thermal conductivity function of its thickness. On the other hand, it allows to identify the critical elements for the heat conduction within the film and through the interface with the substrate (i. e. for the *TBR*), which need then to be implemented into the device-coating process with the Si-interlayer technology.

The measurements and the data analysis presented in the following sections were performed by Y. Zhang and J. Weaver at the *Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow (UK)* and by J. Anaya and M. Kuball at the *Centre for Device Thermography and Reliability, University of Bristol, Bristol (UK)*, with the collaboration of S. Bychikhin and D. Pogany at the *Institute for Solid-State Electronics, Vienna University of Technology, Vienna (Austria)* for the modeling, simulation and interpretation of the results.

8.1 THERMAL CHARACTERIZATION OF THE NCD OVERLAY

As explained in Section 5.2, the poly-crystalline structure of diamond films deposited by CVD on a foreign substrate has important consequences on their thermal properties, with RT thermal conductivity values spanning over two orders of magnitude, roughly from 20 to 2000 $W m^{-1} K^{-1}$, according to the geometry of the grains and to the concentration of defects and impurities embedded within the grains and in the grain boundaries.

Although several experimental techniques were successfully adopted to characterize thick *PCD* films [168], it proved very difficult to gather information on the heat conduction properties of thin nanodiamond films like the ones developed to cap GaN HEMTs, whose thickness is limited to a few microns only (or it may not even exceed 1 μm). Indeed, only little information is available on the anisotropic thermal properties of NCD films in the submicron range of thicknesses [173, 212, 213].

Many factors contribute to make the thermal characterization a challenging task. Firstly, the thermal properties of such thin films are greatly influenced by the nucleation layer, which is the region of the film with the highest thermal impedance, due to its fine-grained structure and high content of defects and non-diamond phases (i. e. a-C, graphite). Therefore, to separate the actual contribution of the film from the one

of the interface, films of different thicknesses need to be analyzed and their results carefully evaluated.

Second, the anisotropy in the shape of the grains in columnar-structured NCD films, with an out-of-plane (i. e. vertical) size larger than the in-plane (i. e. lateral) size, should reflect in an anisotropy between lateral and vertical values of the thermal conductivity, with the latter most likely higher than the former due to the different scattering rates for phonon diffusing in the two directions. However, gaining information on the local heat transport properties in lateral and vertical direction as a function of the film thickness, instead of a spatially-averaged value, requires specifically designed test structures, like for instance membranes, bridges, and suspended bars, which are not easy to fabricate on diamond films hundreds of nanometers thick.

Third, the high thermal diffusivities, which these films may exhibit even at small thicknesses, make mandatory the adoption of thermal characterization techniques with sensitivity and resolution (either spatial, for the steady-state methods or temporal, for the transient ones) high enough to be able to detect values of k above 1000 $Wm^{-1}K^{-1}$ for $\sim$3 μm of material, as reported by Philip *et al.* in [30].

The strategy followed in this work to address the challenges posed by the characterization task consists in:

A. studying the thermal transport in films grown stepwise to different thicknesses;

B. establishing directional heat fluxes in the NCD film by properly tailoring the geometry and boundary conditions of the test structures;

C. adopting several temperature detection techniques, namely *SThM*, μ-Raman thermography and time domain thermo reflectance (*TDTR*), to detect the temperature gradients created within the NCD films by top metal heaters;

D. relying on thermal simulation to analyze the experimental data and extract the thermal parameters (i. e. lateral and vertical component of the thermal conductivity, and *TBR* with the substrate).

Normally each characterization technique has different resolution and different sensitivity in the in-plane and in the out-of-plane directions, thus combining the information coming from different characterization sources becomes necessary to overcome these limitations, while analyzing strongly anisotropic materials like NCD. In this sense, *SThM* and μ-Raman/*TDTR* provide complementary information: while the former has a very high lateral resolution and is mostly sensitive to the topmost part of the film, the latter two are better suited for studying the vertical heat transport in the film and the *TBR* with the substrate.

8.2 TECHNICAL APPROACH

The thermal characterization of thin films usually consists in the determination of the film's thermal conductivity. This requires to generate a heat flux through the film and to detect the resulting temperature gradient. The heat generation as well as the temperature detection part of the measurement can be accomplished by means of either electrical or optical methods.

Direct measurement of the thermal conductivity typically requires the determination of the heat flux and the temperature drop between two points of the sample, and when the film has anisotropic thermal properties, measurements should be carried out in both the in-plane (i. e. lateral) and out-of-plane (i. e. vertical) directions.

For the in-plane thermal conductivity measurement, it is important to limit any heat leakage through the substrate, since it makes it difficult to determine the actual heat flow in the plane of the film. This can be achieved by tuning the geometry of the heat source (if the heat is generated electrically) to enhance lateral heat spreading and by either depositing the film on low thermally-conductive substrates, which minimize heat leakage, or whenever possible by completely removing the substrate (and thus creating membranes, bridges or suspended bars), such that the heat flux through the film can be determined.

For the out-of-plane direction, a reasonable temperature drop across the film must be created, which is high enough to be detected, but not too high to induce a large temperature rise in the substrate. To this scope, a feasible approach is to use a geometry for the heat source, which limits the lateral heat-spreading and induces a strong vertical flux in the film, and to pattern the film in MESAs by eliminating selectively the material lying outside of the heater's area. Another approach is to use transient or modulated heating, which limits the heat-affected region to small volumes within the film or its immediate surroundings.

Following these guidelines, in this work the anisotropic heat conduction properties of sub-µm NCD films were analyzed in steady state conditions by measuring the temperature gradients induced in three kinds of test structures (see Figure 8.2), where the NCD film is: (a) deposited on a low thermally conductive substrate, (b) deposited on Si and patterned into membranes and (c) deposited on Si and patterned into MESAs. Each of them was specifically designed to enhance either a lateral or a vertical heat flux within the film, when electrical power was applied to metal heaters fabricated on its surface.

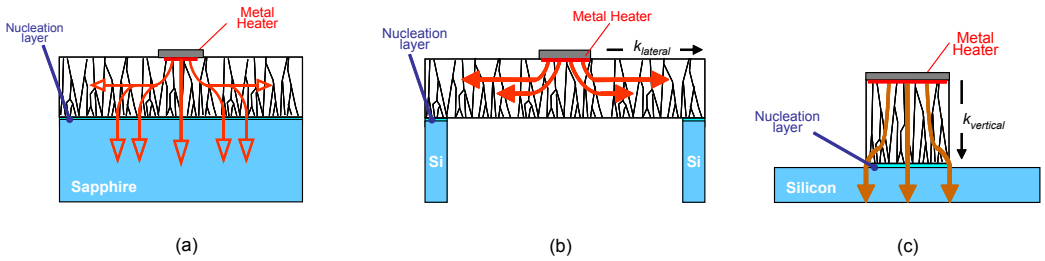


Figure 8.2: Schematic of the test structures used for the characterization of NCD thermal conductivity by *SThM* and µ-Raman: (a) structure used to study the thickness dependence of k; (b) and (c) structures used to isolate lateral and vertical components of k/TBR respectively. The red lines indicate schematically the direction of the heat flow (reprinted from [38] with permission from Elsevier).

8.2.1 *Technology of the test structures*

In the first test structure (a) the thin NCD film is deposited on a substrate, whose thermal properties are homogeneous and well known. In order to enhance the

heat transport inside the NCD layer and limit heat losses to the bottom of the sample, substrates with low thermal conductivity are preferable. In this work sapphire was chosen because besides having a rather low thermal conductivity (k_{sapph}=34 $Wm^{-1}K^{-1}$, three times lower than Si), it can be coated with NCD films of good crystalline quality up to a thickness of ~700 nm by using the inter-layer technique described in Section 4.7.1.

The sample is fabricated by coating a sapphire wafer with PECVD-deposited, 100 nm thick SiO_2 insulating inter-layer and 50 nm α-Si nucleation layer, onto which the NCD film is subsequently nucleated by BEN and overgrown.

In the second test structure (b) the NCD film is nucleated and grown directly on a Si substrate, which is subsequently removed selectively by wet or dry etching (i. e. in KOH at 80 °C or in an ICP reactor using a Bosch process) to leave thin diamond membranes of different sizes (e. g. 100×200, 90-150×500 μm^2) underneath the metal heaters, the diamond itself being the etch-stop layer.

In such a membrane structure, the heat generated by the heater located at the center is constrained to flow laterally inside the diamond membrane, thus avoiding vertical losses through the substrate (neglecting the heat transfer to the surrounding environment), and allowing to isolate the lateral component of NCD thermal conductivity, $k_{lateral}$.

In the third test strucure (c) the NCD film is initially grown on silicon and subsequently mesa-etched to the substrate by RIE in Ar/O_2 using a hard etch-mask (either Al, or Ti, or even the metal heaters fabricated on the surface), thus leaving the NCD film sandwiched between the top metal heater and the substrate. Since the heat crosses the structured NCD film flowing in the direction parallel to the columnar grain structure, the heat losses due to lateral conduction are minimized.

This structure was used to study the vertical heat transport properties of the NCD film. By measuring the temperature rise over the diamond step relative to the silicon substrate, the vertical component of NCD thermal conductivity, $k_{vertical}$, and the *TBR* with the substrate could be extracted.

8.2.2 *Design of the heat source*

A rather simple and easily controllable way to induce a time-independent heat flux in the sample consists of applying a DC-power to a metal resistor fabricated on its surface. The geometry of the metal stripe (i.e. its width *W* and length *L*) in respect to the film thickness *D* has a major impact on the type of properties, which can be extracted from the measurements. As Figure 8.3 shows, a planar heater induces a strong vertical flux in the film, and thus it is the preferred design to analyze the heat transport properties in the out-of-plane direction. Line and point-like sources instead, are more suitable for studying the in-plane component of the thermal conductivity, because they enhance the lateral heat spreading in the film.

The choice of the metal used to fabricate the resistor is based upon several factors; the fabrication capabilities and the power supply equipment, which will be used to apply the electrical power indicate a suitable range for its electrical resistance. Among the possible candidates, metals with the lowest thermal contact resistance with the diamond film should be preferred [215, 216]. In addition, the thickness of the metal

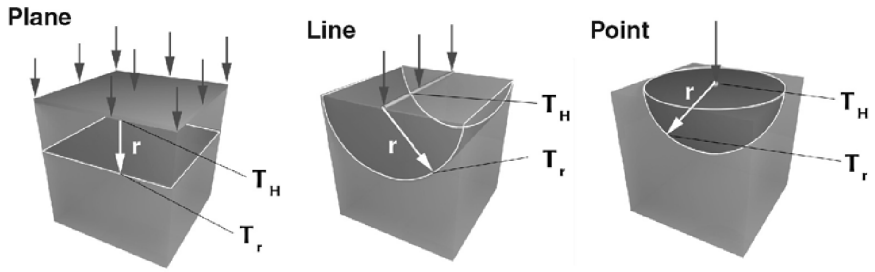


Figure 8.3: Heat flux generated in the film under study, according to the geometry of the heat source, which may have a plane, line or point-like shape (from [214]).

heater should be higher than the roughness at the film's surface in order to assure optimum thermal contact and good mechanical adhesion.

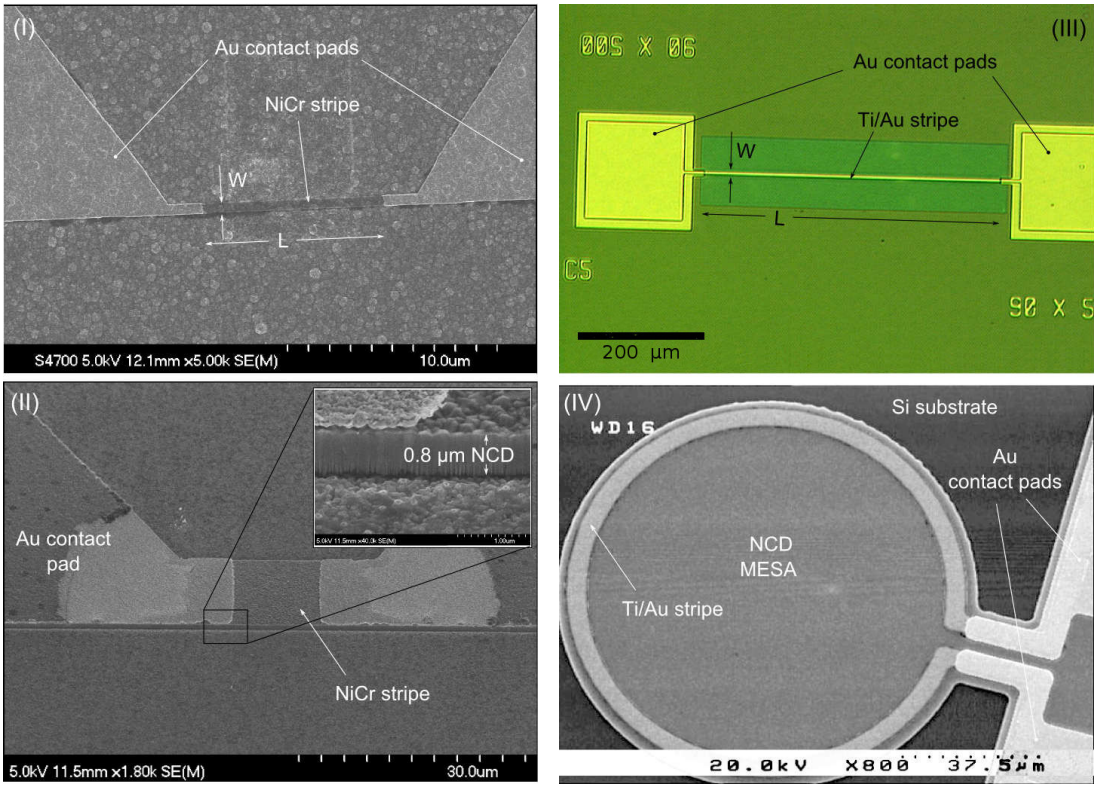
For the samples characterized by *SThM*, a thin NiCr metal stripe (~30 nm thick) and Au contact pads were patterned by e-beam lithography and evaporated onto the surface of the NCD film. For the samples characterized by μ-Raman thermography, a stack Ti/Au was used for both the heaters and the contact pads, 10/100 and 10/200 nm being their respective thickness.

The power can be fine-adjusted to induce the desired temperature gradient in the film, taking care not to overload the resistor behind its dissipation capabilities. The range of power levels suitable for the heater geometries used in this work varied between some mW and a few watts, according to the size and the material of each heater (the smallest heaters had a surface area of ~4 μm^2, the largest ones of $\sim 3 \times 10^3$ μm^2).

Figure 8.4 shows SEM pictures of the metal heaters fabricated on the surface of the NCD film in different test structures. The heaters with high aspect ratio $L/W >> 1$ were adopted to enhance the lateral spreading in the test structure of type (a) and (b) in Figure 8.2. The MESA-structured samples (type c in Figure 8.2) featured either low aspect ratio, square-like heaters with $L/W \sim 1$, which induce a strong vertical flux within the film, or ring-like heaters with different diameters. The former ones were used in the samples characterized by *SThM*, while the second ones were designed for μ-Raman thermography: the inner part of the ring is the area where the Raman laser focuses to measure the temperature in the NCD MESA and in the underlying substrate.

Heaters, where the metal stripe is replaced by a thin layer of boron-doped nanocrystalline diamond, could also be fabricated, thus avoiding the *TBR* between metal/NCD. Although such a heater requires an additional diamond growth step and has at least 2 orders of magnitude higher resistivity than the metal counterpart, it allows to achieve the lowest thermal contact resistance with the intrinsic part of the film underneath it. In addition, since it has the same thermal expansion coefficient, it is mechanically and thermally stable in all biasing conditions.

Figure 8.5 shows the SEM micrographs of a MESA-structured sample in which the ring-like heater (bright areas) is made of 200 nm boron-doped diamond.



(a) (b)

Figure 8.4: SEM and optical top views of the heaters used for the thermal characterization by *SThM* (a, from [38]) and µ-Raman thermography (b): line heaters with high aspect ratio (I) and (III), to enhance the lateral heat-spreading; plane (II) and ring-like (IV) heaters, to induce a strong vertical heat-flux in the NCD MESAs.

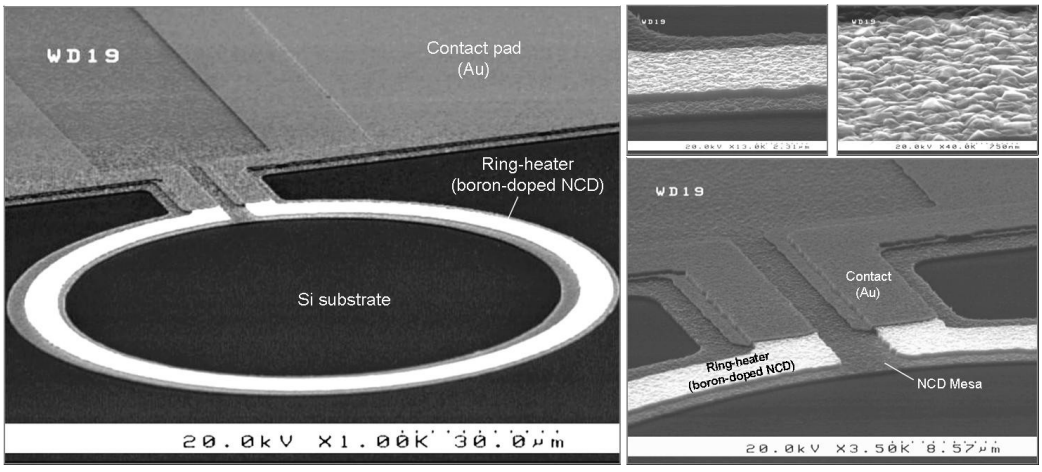


Figure 8.5: SEM micrographs of the ring-like heaters in which the metal stripe has been replaced with a boron-doped NCD stripe.

8.2.3 *Temperature detection methods*

In this work, two main thermal characterization techniques were employed, namely scanning thermal microscopy (*SThM*) and μ-Raman thermography. For some of the measurements, μ-Raman was used in conjunction with time domain thermo reflectance (*TDTR*), thus increasing the confidence in the extracted values for the film's thermal parameters.

Scanning thermal microscopy (University of Glasgow)

A scanning thermal microscope operates by bringing a nm-sized temperature-sensing tip in close proximity to a sample surface. Figure 8.6a shows a schematic diagram of a SThM, consisting of an AFM, in which a temperature-sensing tip is mounted on the AFM cantilever to be scanned across a sample surface.

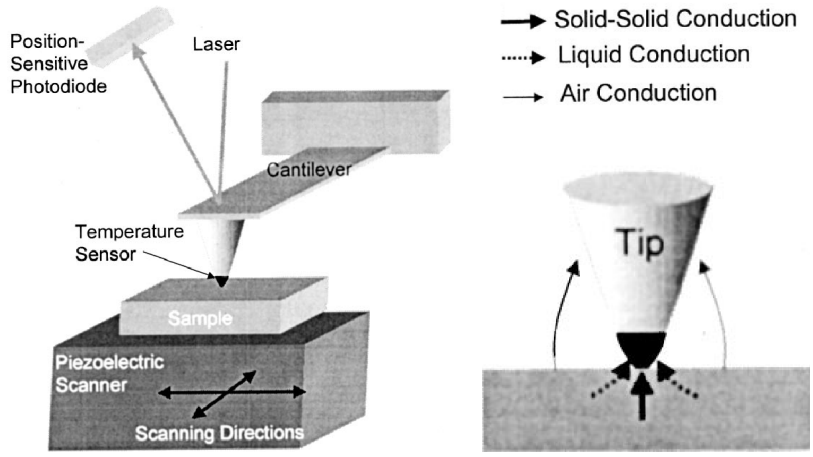


Figure 8.6: (a) Measurement setup of scanning thermal microscopy (*SThM*); (b) main heat transfer mechanisms between tip and sample surface during the scan (from [217]).

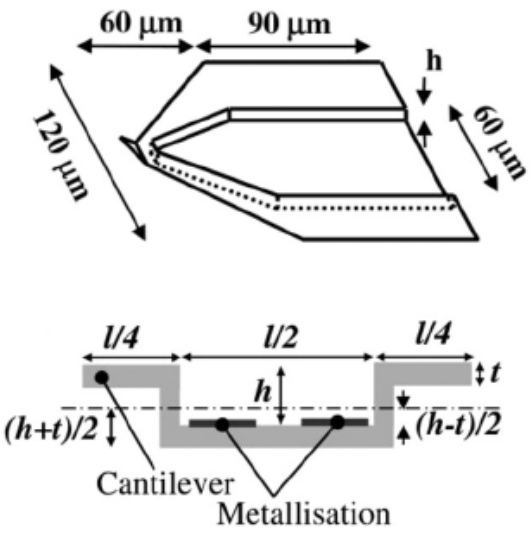
Cantilever deflections are measured by reflecting a laser beam off the cantilever and onto a position-sensitive photodiode. The deflection signal is used in a control system to maintain a constant tip-sample contact force while the tip is scanned laterally.

As the tip comes in contact with the sample its temperature changes due to localized heat transfer between the tip and sample surface (see Figure 8.6b). When the tip reaches a local equilibrium with the sample, one obtains the spatial temperature distribution of sample surface. Based on this principle, by measuring the temperature change in response to a known heat flux, one can obtain the local thermal properties of the sample.

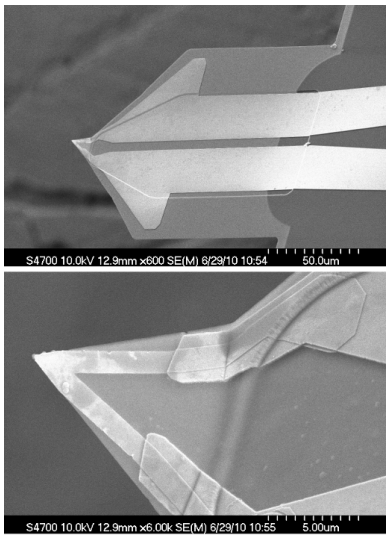
For the characterization of our NCD films Y. Zhang and J. Weaver at the University of Glasgow[1] adopted a *SThM* equipment, which includes a custom-made thermo-sensitive probe consisting of a cantilever carrying a temperature-sensitive tip. The cantilever developed and fabricated by the Glasgow group features a novel, grooved design which reduces its thermal bending at high temperatures (up to 60% less than

1 Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow (UK).

a commercial probe) [218], thus allowing to keep the tip in contact with the sample surface under all bias conditions of the heater. The temperature-sensitive tip is a nano-sized Pt (or Pd) thermo-resistor located at the edge of the cantilever. In Figure 8.7 the layout and SEM pictures of the fabricated cantilever are shown.



(a) cantilever layout



(b) details of the cantilever and tip

Figure 8.7: (a) Schematic layout for the grooved cantilever and (b) SEM images of a fabricated grooved cantilever probe (from [218]).

Prior to every run of measurements, the probe is calibrated using a microfabricated temperature standard based on a measurement of Johnson noise [219]. Figure 8.8 shows the topographic and the temperature map of the surface of a NCD sample measured by SThM[2] in the proximity of the metal heater (the brightest spot).

The spatial resolution of this technique depends mainly on three factors, namely, tip size, tip-sample heat transfer mechanism, and the thermal design of the probe. With the setup of Glasgow, and performing the measurements in air at standard conditions of pressure and temperature (1 atm, 25 °C), a spatial resolution of ~20 nm (i. e. approx. 2 times lower than the *NCD* surface roughness) and a temperature sensitivity of ~1 K can be achieved.

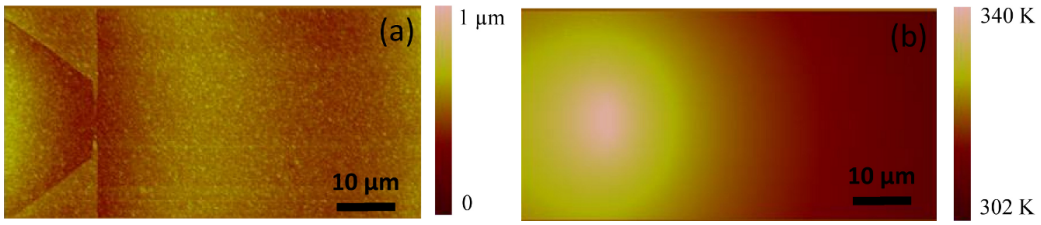


Figure 8.8: (a) AFM topographical map and (b) SThM thermal map[2] of the sample surface in the proximity of the metal heater (reprinted from [38] with permission from Elsevier).

2 measurements performed by Y. Zhang and J. Weaver at the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow (UK).

μ-Raman Thermography (University of Bristol)

Determination of temperature by Raman spectroscopy is based on the temperature dependence of phonon frequency. In fact, as phonons are lattice vibrations, any change in temperature leads to a change in phonon frequency (optical or acoustic) according to the following equation:

$$\Delta\omega = \omega_0 - \frac{A}{\exp\left[\frac{B\hbar\omega_0}{k_B T}\right] - 1} \tag{8.1}$$

where ω_0 is phonon frequency at 0 K, T is the temperature, k_B and $\hbar$ are Boltzmann and Planck constants, respectively, A and B are material-dependent fitting parameters [105]. Usually, one of the strongest modes available in the Raman spectrum of a material is used for temperature determination. Figure 8.9 shows a typical first-order Raman spectrum of a NCD film 1 μm thick grown on a Si substrate.

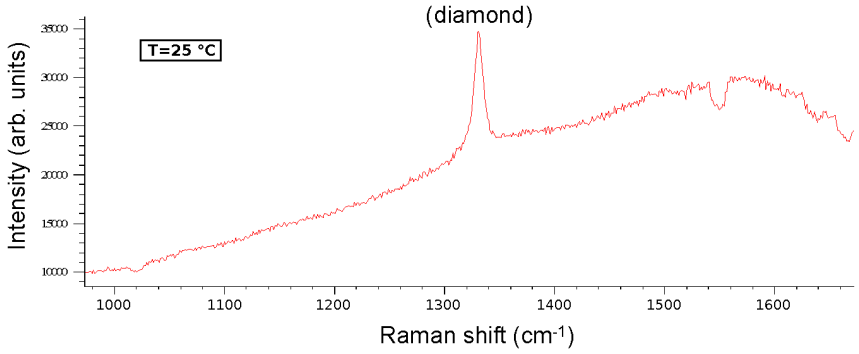


Figure 8.9: Typical Raman spectrum of a *NCD* thin film, indicating the characteristic diamond peak at 1332 cm^{-1}, which is used as temperature marker in the characterization.

The strong phonon mode of diamond at 1332 cm^{-1} can be used to monitor the temperature in the sample by means of a calibration curve like the one shown in Figure 8.10, where the shift in this Raman peak and the one in the peak of the substrate on which the diamond film is deposited (i. e. Si in our case) are plotted in a wide temperature range.

It is worth noticing that for heteroepitaxial layers, the frequency dependence of phonon modes also includes contributions from elastic strain [195], resulting from the difference in lattice thermal expansion coefficients between layers of different materials. Therefore, for improved accuracy in the temperature determination, the calibration dependence for a specific layer structure must be used (in our case the layer stack is NCD/Si).

Once the calibration has been performed, the temperature in the actual test structure can be extracted for the various layers by measuring the difference between the phonon frequency, when the heater stripes are left unbiased and when they are biased at different DC power levels. Usually, the temperature of the unbiased device is known, e. g. room temperature, so this position is then used as a reference for determination of the relative phonon shift due to heating.

The accuracy in the temperature detection by such a method depends on several factors, like for instance the linewidth of the chosen Raman peak and the smallest value of frequency change of a given phonon mode, which can be reliably determined

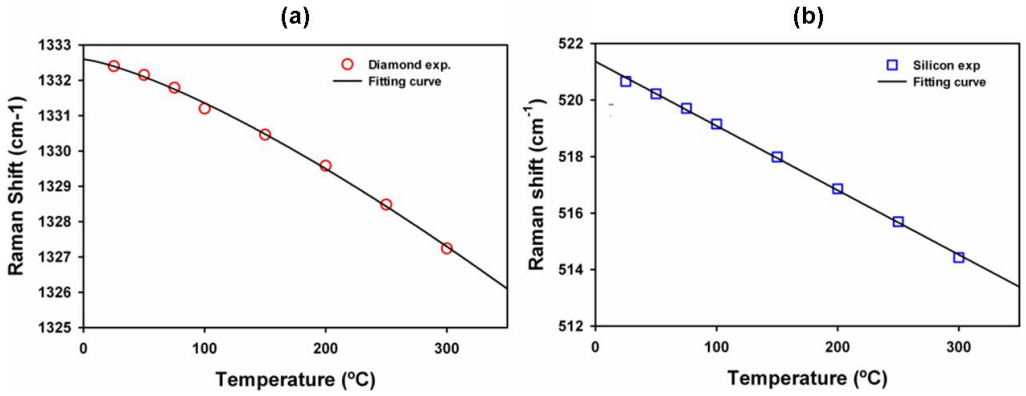


Figure 8.10: Temperature-induced shift[3] in the position of the characteristic Raman peaks of (a) diamond, at 1332 cm^{-1} and (b) Si, for temperatures between 0 and 300 °C.

from the measured Raman spectrum. Furthermore, the accuracy improves as the temperature increases, since the gradient of phonon-frequency versus temperature increases with higher temperatures (Fig. 8.10).

With the system used here, for the diamond peak in nanocrystalline diamond at 1332 cm^{-1}, the temperature sensitivity is of the order of 2–5 °C at 100 °C.

Laterally, the limit of the spatial resolution of such a technique is the one of a microscope measurement, which is defined by the radius D_L of the Airy disk (Rayleigh criterion) or the more rigorous Sparrow criterion [220]:

$$D_L = \frac{1.22(1.00) \cdot \lambda}{2 \cdot NA} \tag{8.2}$$

where 1.22 stands for the Rayleigh criterion (1.00 for the Sparrow criterion), NA is the numerical aperture of the lens and λ the wavelength. For 488 nm and NA = 0.55 used in this work, D_L is on the order of 0.5-0.7 μm.

In depth, the use of different laser excitation wavelengths allows selective probing of phonons, a feature which can be used to retrieve information on the material properties, either averaged over the layer thickness or in a surface layer. For instance in diamond, which has a bandgap of 5.45 eV, only material properties averaged over the film thickness can be probed, both under visible excitation wavelengths (typically in the 400 to 500 nm range), and UV excitation wavelengths (e. g. ~300 nm), whereas surface properties can be studied in the Si substrate due to the absorption of the laser light within the first micron from its surface.

The Raman signal can be collected only from device areas, which are not covered by metallic structures, since metals absorb the laser light. In addition, metals do not exhibit easily accessible lines in their Raman spectrum for temperature measurements.

To obtain the temperature from an area of the device, the scanning mode is often used. The probing laser beam dwells at each spot to acquire the Raman spectrum and is then moved to the next position using a motorized microscope stage.

For the characterization of our NCD films J. Anaya and M. Kuball at the University of Bristol[3] adopted a Renishaw InVia μ-Raman system equipped with a Leica micro-

3 Centre for Device Thermography and Reliability, University of Bristol, Bristol (UK).

scope and two laser sources, namely argon – for visible wavelengths of 488 nm, 514 nm – and HeCd for UV at 325 nm.

A 50X objective lens (NA = 0.55) was used to focus the Ar laser beam (488 nm) onto the sample surface in a spot with diameter less than 1 µm. Measurements were carried out using the confocal mode. Spectral resolution of the InVia system is about 2.0 cm^{-1}, and the minimum shift in Raman line resolvable is 0.02 cm^{-1}.

Both membrane- and MESA-structured NCD/Si test samples were characterized with this method. To increase the spatial resolution of the µ-Raman technique, Si nanowires were placed on the surface of the NCD film/metal heater to be employed as local surface thermometers.

Each sample was then attached to a CuW heat sink, and its temperature was varied between 0 and 300 °C by means of a temperature-controlled stage during the calibration phase, while it was kept at 25 °C using a Peltier thermal stage during the actual measurements.

All temperature measurements[4] were performed in steady-state conditions, by applying a DC bias to the heater stripes, which generated a power between 1 and 10 W. A motorized XY-stage with a lateral resolution of 0.1 µm was used to obtain the temperature distribution along a line perpendicular to the heater line for both membrane and MESA samples (Figure 8.11).

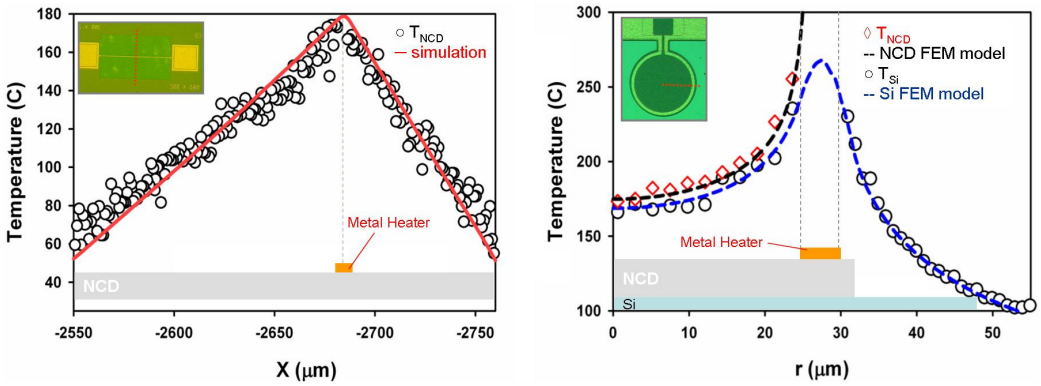


Figure 8.11: Temperature profiles[4] within the NCD film and Si substrate, obtained by scanning the Raman probe along a line (indicated in red) perpendicular to the metal heater in membrane (left) and MESA (right) test structures.

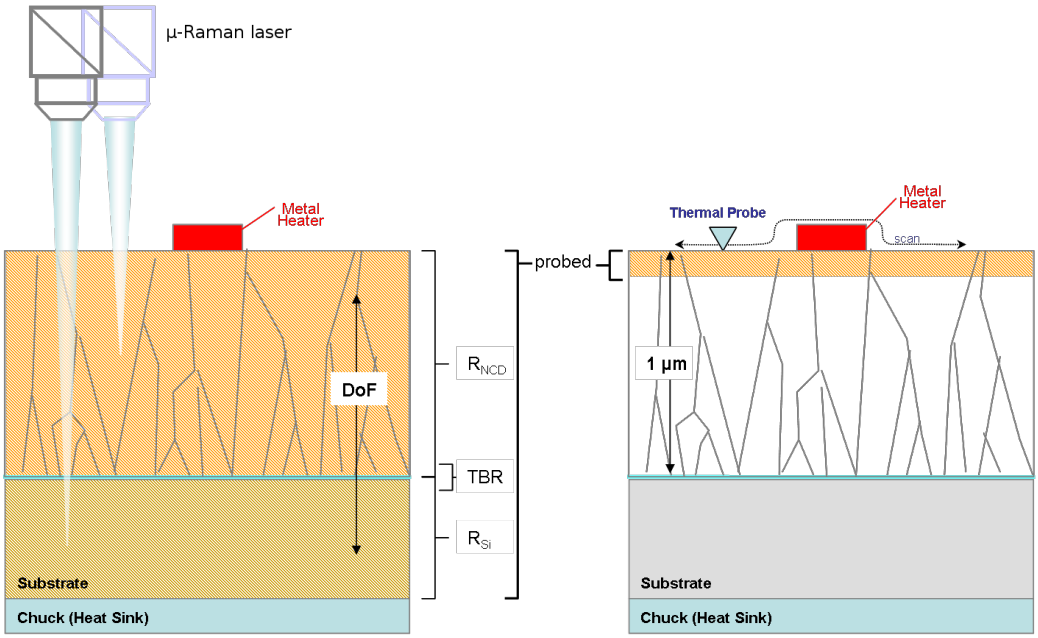
Comparison of the two techniques

At this point it is important to understand the role of the temperature detection method in the extraction of the thermal parameters of the nanodiamond film, and thus the meaning of the thermal conductivity numbers, which will be presented later.

In Figure 8.12 the two techniques *SThM* and µ-Raman thermography are compared side-by-side by highlighting the parts of the NCD film, which are probed by each method.

While *SThM* is highly sensitive to the heat conduction properties of the topmost part of the film, which determine the surface temperature distribution measured by the

4 measurements performed by J. Anaya and M. Kuball at the Centre for Device Thermography and Reliability, University of Bristol, Bristol (UK).



(a) μ-Raman Thermography (b) Scanning Thermal Microscophy

Figure 8.12: Schematic comparing the μ-Raman (a) and *SThM* (b) thermal characterization techniques; the filled area indicates the region of the sample probed with each method (DoF is the depth of focus of the μ-Raman equipment).

temperature-sensitive tip, the μ-Raman beam probes the whole NCD film, nucleation region included, and the top part of the substrate, in which then it is absorbed.

Therefore, a substantial difference in the thermal conductivity k values estimated by the two methods should be expected, as *SThM* analyses the part of the film with the largest grain size, and thus the highest k, while the μ-Raman values are averaged over the film thickness, and ultimately dominated by the fine-grained, and thus the least conductive, part of the film at the interface with the substrate.

On the other hand, this makes the two techniques complementary: *SThM* is particularly suited to study the lateral heat transport in the film, and thus to extract its peak lateral thermal conductivity $k_{lateral}$, while with μ-Raman the vertical transport through the NCD to the substrate can be analyzed, and thus its average vertical thermal conductivity $k_{vertical}$ and the *TBR* at the interface with the substrate can be estimated.

8.2.4 *Data analysis (TU Vienna, University of Bristol)*

The temperature profiles obtained by *SThM* and μ-Raman on the test structures need to be analyzed by means of 3D numerical models reproducing the geometry, material stack and boundary conditions of the real sample. In this work, a pure thermal model (i.e. without electro-thermal interaction) built in COMSOL® or in ANSYS® finite element analysis (*FEA*) software was used.

The *FEA* software solves the steady-state heat diffusion equation [221]:

$$Q(x,y,z) + \nabla \cdot k\nabla T(x,y,z) = 0 \tag{8.3}$$

where Q is the power density applied to the heater, expressed in W/m^3, T is the temperature and k is the NCD thermal conductivity tensor

$$k = \begin{bmatrix} k_x = k_{lateral} & 0 & 0 \\ 0 & k_y = k_{lateral} & 0 \\ 0 & 0 & k_z = k_{vertical} \end{bmatrix}, \tag{8.4}$$

accounting for the spatial anisotropy in the heat conduction properties of nanocrystalline diamond.

To account for the thickness dependence of k and estimate the contribution of different regions of the film to the overall conductivity, the NCD film in the model may be split in H layers, each of thickness t_H, with isotropic, thickness-averaged thermal conductivity k_H. For instance, a set of samples in which the NCD film is grown stepwise to different thicknesses $t_1 < t_2 < t_3$ can be analyzed by a single, multi-layer structure, where the first layer has thickness t_1 and conductivity k_1, the second layer has thickness $t_2 - t_1$ and conductivity k_2 and the topmost layer has thickness $t_3 - t_2$ and conductivity k_3.

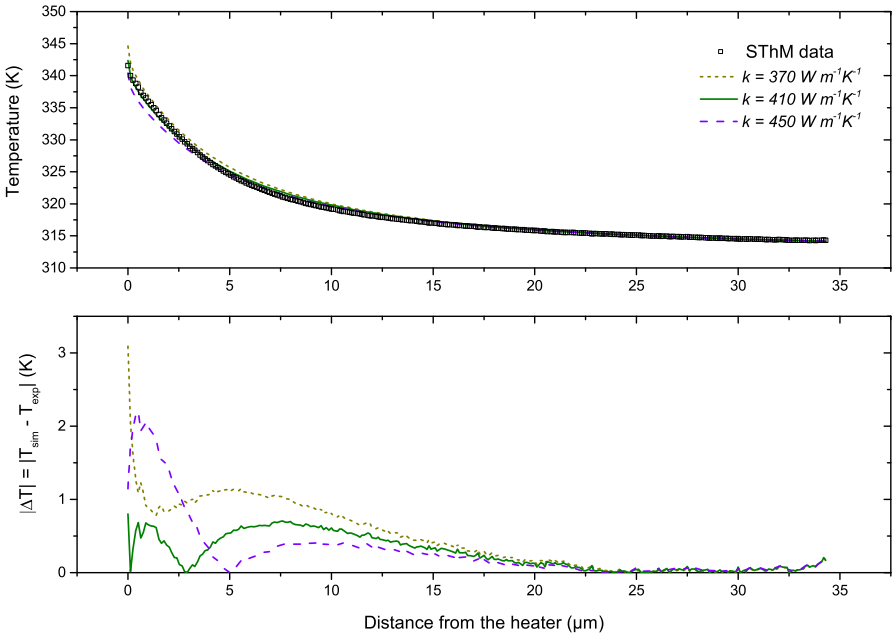
The NCD thermal conductivity k and the *TBR* between NCD/substrate are kept as free parameters in the model. By varying these parameters, a family of simulated temperature curves can be obtained, from which the actual thermal conductivities are estimated as best-fit, i. e. as the set of values $\{k_{lateral}, k_{vertical}, TBR\}$ minimizing the difference $\Delta T = T_{sim} - T_{exp}$ between simulated curve and experimental data.

The experimental temperature profile measured along a line perpendicular to the metal heater and passing through its center, where the highest temperature is reached, is the most suitable for the analysis, since the temperature decay with distance from the heater center has the steepest gradient there (and thus the highest sensitivity to the thermal conductivity of the NCD film).

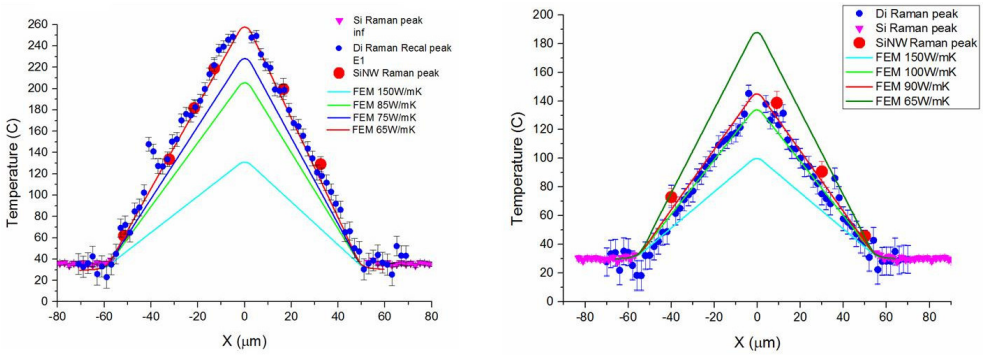
It is worth noting that in this work the temperature dependence of the thermal parameters used in the model was neglected for the analysis of the data collected by *SThM*, since at the low power levels used in the experiments the temperature gradients (ΔT) remain well below 100 K. It was instead taken into account in the model designed for the μ-Raman experiments, which were conducted at higher power levels for the heaters, and thus exhibited higher temperature gradients between 100 and 200 K.

Examples of such a fitting procedure are provided in Figure 8.13 for temperature data obtained by *SThM* (a) and μ-Raman (b) respectively. The temperature trend (a) is the typical outcome of a *SThM* measurement performed at low power levels (i. e. 15-20 mW); the ΔT is small and does not exceed ~ 30 K, besides the decay departing from the heater center is strongly non-linear due to heat-losses to the tip, to the environment and to the substrate (when present). The μ-Raman temperature profiles shown in (b) instead, were obtained at high power dissipation levels (~200 mW) on two membrane-structured samples, in which the NCD film was 680 nm (left-side) and 1 μm (right-side) thick respectively. In this case the maximum ΔT is above 100 K, and since no heat-losses to the substrate and to the tip are present, the decay from the heater center is well approximated by a linear trend.

The accuracy of the fit, and thus the error affecting the thermal conductivity values estimated in such a way, depends mostly on the sensitivity of the temperature detection technique to a specific component of NCD thermal conductivity.



(a) (top) Right hand side of the temperature profile along the heater center, fitted by simulated profiles obtained by varying the thermal conductivity of the NCD film in the model. (bottom) Temperature difference between simulated and experimental data used to identify the best-fit value of k (reprinted from [38] with permission from Elsevier).



(b) Temperature profiles measured by µ-Raman along the heater center for (left) 680 nm and (right) 1 µm membrane-structured samples, fitted by simulated profiles.

Figure 8.13: Examples of the fitting procedure used to extract the values of the thermal parameters for experimental data collected by (a) *SThM* [measurements performed by Y. Zhang and J. Weaver at the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow (UK)] and (b) µ-Raman [measurements performed by J. Anaya and M. Kuball at the Centre for Device Thermography and Reliability, University of Bristol, Bristol (UK)].

For instance the temperature gradients measured in the lateral direction, where the spatial resolution is high (0.02-0.7 μm) and many experimental points are collected, are affected by a small error compared to the gradients measured in the vertical direction, where the spatial resolution is low and only 2-3 experimental points (i. e. above, within and beneath the film) are available. This different sensitivity in the in-plane and out-of-plane directions leads to an error in the order of 10-20% for the the extracted values of the lateral thermal conductivity $k_{lateral}$, and of even 60% for the vertical one $k_{vertical}$.

8.3 RESULTS AND DISCUSSION

For the thermal characterization experiments, NCD films were BEN-nucleated either on Sapphire or on Si substrates, grown by HFCVD to different thicknesses under nominally identical conditions (by varying the total growth time only), and patterned into membranes and MESA structures to be characterized by *SThM* or μ-Raman.

The NCD outgrowth stage was performed at T_{sub} =750 °C and P_{cvd} =1.5 kPa with 0.4% CH_4 diluted in H_2. As detailed in Chapter 6, the NCD films grown in such conditions are columnar-structured, exhibit low concentration of impurities in the grain-boundaries and have grains with in-plane dimensions in the range 100-200 nm within the first micron from the interface with the substrate.

To increase the grain-growth gradient γ, in two samples (labeled E5 and E6), the CH_4 concentration was reduced to 0.3% and 0.2% respectively. These samples have indeed the same total thickness (1 μm), but larger in-plane grain size than that of E4 (173 and 205 nm vs 160 nm), which was grown with 0.4% CH_4.

The values of the thermal parameters extracted by fitting the experimental data collected by *SThM* and μ-Raman on such films are listed in Table 8.1.

By looking at the numbers reported in the table, the first thing worth noticing is the significant difference in the thermal conductivity values extracted for films in the sub-μm range of thicknesses when *SThM* is adopted rather than μ-Raman.

As discussed in the previous sections, this is a consequence of the fact that each technique probes a different part of the film, *SThM* being mostly sensitive to the topmost part of the film, which is the region where the grains reach their largest in-plane size, and thus where the phonons scattering at the grain boundaries is the lowest. Since μ-Raman instead probes the response of the whole film to a temperature gradient, this is reflected in values averaged over the film thickness, which could be even 10 times lower than the *SThM* counterpart for the thinnest films, the heat conduction properties of which are dominated by the near-interfacial, fine-grained – and thus low conductive – nucleation region.

Besides this fundamental difference, a pattern emerges clearly from the data, whose values agree well with the expected anisotropy between lateral and vertical component of k and confirm the expected strong correlation between film thickness (and thus in-plane size of the grains) and heat conduction properties.

When considering the film microstructure, it is reasonable to expect that the anisotropy in the shape of the grains, with an out-of-plane (i.e. vertical) size much larger than the in-plane (i.e. lateral) size, should be reflected in better heat conduction along the columns rather than across adjacent grains, which involve higher scattering

Table 8.1: Thermal conductivity (k) and TBR values (R_{th}) for NCD films in the sub-μm range of thickness.

Method	*Structure*	*Sample*	*t* (nm)	*d* (nm)	Extracted parameter	$k \pm \Delta k$ $(Wm^{-1}K^{-1})$	
SThM	NCD/sapph	A1	370	77	$k_{effective}$	230	20
		A2	600	116		390	20
		A3	650	124		410	20
	membrane	B1	500	110	$k_{lateral}$	270	20
		B2	1100	188		500	20
	MESA	C1	800	146	$k_{vertical}$	700	300
μ-Raman	membrane	E1	320	106	$k_{lateral}$	30	3
		E2	450	115		50	3
		E3	680	133		65	5
		E4	1000	160		90	5
		E5	1000	173		110	5
		E6	1000	205		140	5
	MESA	F1	320	106	$k_{vertical}$	125	75
		F3	680	133		250	125
		F4	1000	160		350	150
						$R_{th} \pm \Delta R$ (m^2K/GW)	
μ-Raman	MESA	F1	320	106	$TBR_{effective}$	5	3
		F2	450	115		13	6
		F3	680	133		20	3
		F4	1000	160		45	1

t: NCD film thickness measured at SEM.
d: NCD in-plane grain size calculated from SEM and AFM micrographs of the top surface.

rates. In addition, based upon the model of phonon scattering at the grain boundaries, a gradient in thermal conductivity with film thickness should be expected as well, since the grains get larger with increasing distance from the substrate, and larger grain dimensions imply a lower concentration of grain boundaries, and thus lower scattering events per unit of material.

Strong anisotropy and thickness-dependence in the thermal conductivity is what have indeed been measured, with $k_{vertical}$ up to 3 times higher than $k_{lateral}$ and thicker (and hence larger grain-sized) films exhibiting larger thermal conductivity *k* compared to the thinner ones.

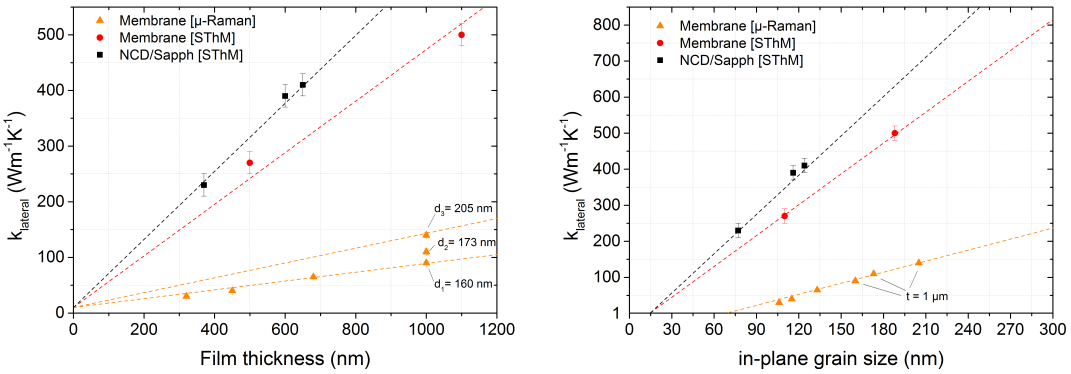
In the following sections, the results of the analysis are further discussed by means of graphs in which each component of the thermal conductivity and the TBR are plotted as a function of either the film thickness or the film in-plane grain size.

8.3.1 *In-plane heat transport: lateral thermal conductivity*

In Figure 8.14 the values of the lateral component of *k* extracted by *SThM* and μ-Raman from NCD-on-sapphire and membrane structures are plotted for each sample against the thickness (on the left side, a) and the in-plane grain size (on the right side, b) calculated from SEM and AFM micrographs of the top surface.

The *SThM* experiments were performed on both NCD-on-sapphire samples (A1, A2, A3 in Table 8.1) and on membrane-structured samples (B1, B2). The idea behind both structures is to limit any heat-loss through the substrate and thus force a pure lateral flux within the NCD film, from which the lateral thermal conductivity could be then extracted. However, in the NCD-on-sapphire design, the poor thermally conductive sapphire and the high thermally resistive SiO2/a-Si interlayers on which the diamond film is deposited are not as effective in limiting the heat losses in the same way like the complete removal of the substrate, and thus the heat transport in this structure is still a mix of lateral and vertical conduction.

For this reason, the thermal conductivity extracted from NCD-on-sapphire samples (labeled $k_{effective}$) appears to be higher than the one extracted from membrane-structured samples of similar thickness.



(a) (b)

Figure 8.14: Lateral thermal conductivity values obtained by *SThM* and μ-Raman on NCD-on-sapphire and membrane structures and plotted against the thickness (a) and the in-plane grain size (b) of the NCD film in each sample.

The plot $k_{lateral}$ vs film thickness (a) shows that the topmost part of the film analyzed by *SThM* has significantly higher thermal conductivity than the film's average, which is represented by the μ-Raman values. For instance, even if the near-surface region of a 0.5 μm thick NCD film has a $k_{lateral}$ of ~ 250 $Wm^{-1}K^{-1}$, k decreases steeply in the inner part of the film approaching the nucleation region, where it reaches the minimum, such that on average its lateral conductivity does not exceed 50-70 $Wm^{-1}K^{-1}$.

The experimental points related to each set of samples (A, B and E in the Table) may be interpolated with good confidence by linear trend lines. Such a trend correlates well with the linear increase in the in-plane dimensions of the grains with thickness z observed in this region of the film, which is expressed by the relation $d(z) = d_0 + \gamma z$, where γ is the grain growth gradient (as described in Chapter 6).

By extrapolating these linear trends for NCD thickness approaching zero, it is possible to estimate that the thermal conductivity of the nucleation region is approx. 1 $Wm^{-1}K^{-1}$, which is comparable to the one of an amorphous material [222]. In the first tens of nanometers, the NCD film has a disordered microstructure consisting of non-diamond, amorphous phases inter-mixed with diamond nanocrystals, similar to *UNCD* films, whose thermal conductivity is indeed rather low and isotropic (<10 $Wm^{-1}K^{-1}$ [185]).

The set of samples characterized by μ-Raman comprised also three test structures (E4, E5, E6) in which the NCD film was overgrown to the same total thickness of 1 μm, but with different γ-gradient, by tuning the growth parameters during the outgrowth phase (technique discussed in Section 6.3.1). As can be seen in the graph, to larger in-plane dimensions of the grains corresponds a higher $k_{lateral}$, whose average value increased of 55% (from 90 to 140 $Wm^{-1}K^{-1}$) when the size of the grains grew by ~30% and passed from 160 to 205 nm for the same thickness.

Side (b) of Figure 8.14, where the same data are plotted this time against the grain size, allows to estimate the corresponding gain at the top part of the film. It is worth noting that the three points lay on the same line interpolating the rest of the μ-Raman data, thus confirming that the linear model is appropriate for fitting the data. By referring to the red line going through the *SThM* points, which carries information on the heat conduction properties of the topmost part of the film, it is possible to predict that an increase in lateral grain size from 160 to 205 nm should lead to a rise in $k_{lateral}$ from 400 to 550 $Wm^{-1}K^{-1}$, which is approx. a 37.5% gain.

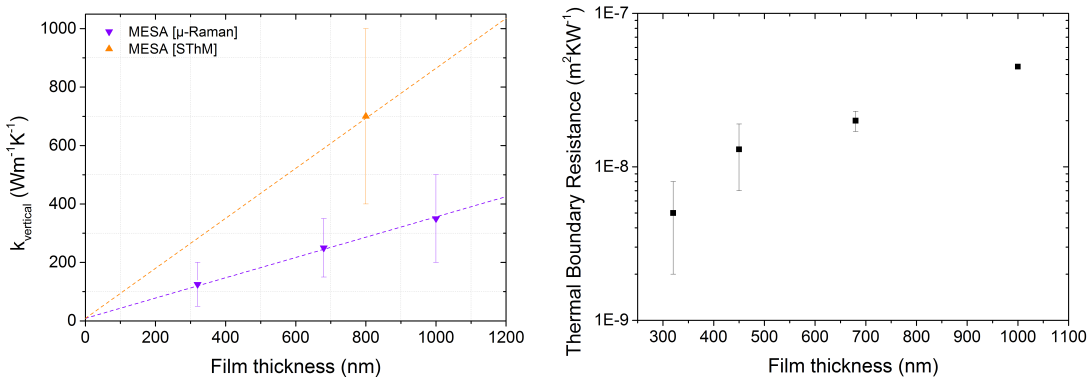
The extrapolation at small grain sizes *d* for the trend lines shows that a columnar film whose grains have a size at the surface smaller than ~70 nm, would have an average $k_{lateral}$ as low as 1 $Wm^{-1}K^{-1}$, while its topmost region would still exhibit 2 orders of magnitude higher lateral conductivity.

These results highlight on the one hand that the growth of highly conductive thin NCD films requires a fine control over the film microstructure in order to reach large in-plane size of the grains as early as possible (i. e. as close as possible to the interface with the substrate). On the other hand they point out how crucial it is to improve the thermal properties of the nucleation region of the film, which would otherwise severely limits the performance of the whole film, even when the upper regions could achieve 1/4 of the ideal diamond *k* in less than 1 μm distance from the interface.

8.3.2 *Out-of-plane heat transport: vertical thermal conductivity and TBR*

In Figure 8.15 the values of the vertical component of *k* (on the left side, a) and TBR (on the right side, b) extracted from MESA-structured samples are plotted against the NCD film thickness. The data were collected by analyzing the vertical heat transport in five samples: one sample was studied by *SThM*, while for the other four the μ-Raman technique was adopted, hence for these films information on the thermal boundary resistance (R_{th}) at the interface NCD/substrate is also available.

The plot of the vertical thermal conductivity (a) clearly indicates that the vertical heat transport, in a similar manner to the lateral one, is very sensitive to the film's microstructure, both in terms of thickness and in-plane dimensions of the grains, with values gradually increasing as the film gets thicker, from 125 $Wm^{-1}K^{-1}$ for the thinnest film (320 nm thick) up to 350 $Wm^{-1}K^{-1}$ for the 1μm thick film. The *SThM* data point suggests that in this range of thicknesses the topmost part of the film may even reach 1000 $Wm^{-1}K^{-1}$, which is nearly half of the single crystal thermal conductivity. Also in this case, the linear extrapolation of the data predicts that the thermal properties of the nucleation region are isotropic, with $k_{vertical} = k_{lateral} = k$ of approx. 1 $Wm^{-1}K^{-1}$.



(a) (b)

Figure 8.15: (a) Vertical thermal conductivity (a) and *effective* thermal boundary resistance (R_{th}) values (b) obtained by *SThM* and μ-Raman on MESA structures and plotted against the thickness of the NCD film in each sample.

At a first glance, the TBR plot (b) seems to suggest a correlation exists between film thickness and interfacial thermal resistance, in which the TBR increases as the NCD film gets thicker, even of one order of magnitude, passing from $\sim 5 \times 10^{-9}$ at 320 nm to $\sim 4.5 \times 10^{-8}$ m^2K/W at 1 μm.

Although differences may exist between each sample, being the nucleation technique the same for all of them, the most likely explanation of this trend is that it is due to the model adopted to analyze the data and extract the thermal parameters.

What differentiates a layer of a certain thickness from a thicker one is the contribution of the volume resistance, which becomes increasingly higher as the film gets thicker and adds to the actual TBR at the diamond/Si boundary.

In the model instead, it is convenient to consider the volume resistance of each layer as a boundary resistance lumped at the interface, plus a term which is thickness independent [173, 176]. On the one hand, this approach allows to estimate the vertical component of NCD thermal conductivity even for small layers hundreds of nm thick, which would otherwise require nm-spatial resolution in depth to be detected. But on the other hand it overestimates the TBR between the film and the substrate, which would therefore be more appropriate to call *effective* TBR.

The value of $5 \pm 3 \times 10^{-9}$ m^2K/W extracted from the 320 nm thick film seems to be a realistic upper limit for the actual TBR between diamond/Si in our samples. This value was cross-checked by the team at the University of Bristol[5] by means of *TDTR* and was found in agreement with the results obtained by Verhoeven *et al.* in [29] for BEN-nucleated films on Si (see also Section 5.2.2).

Despite the temperature detection method adopted, the uncertainty in the estimation of $k_{vertical}$ ranges between 40 and 60%. This is due to the scarce spatial resolution in the depth direction of both techniques, which prevents to pinpoint the temperature drop within the film with nm precision, as it would be necessary for a strongly anisotropic material like NCD. In fact, the *SThM* tip does not have access to the inner part of the film and can only monitor the surface temperature, while the

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μ-Raman signal carries information only about the average temperature within the whole NCD layer, thus making it very challenging to separate the contribution of the film itself from the one of the nucleation region, which is the most resistive part of the film.

A very simple, but effective way of describing the challenges involved in the accurate determination of $k_{vertical}$ is by means of the thermal resistance model of the MESA-structure which is depicted in Figure 8.16.

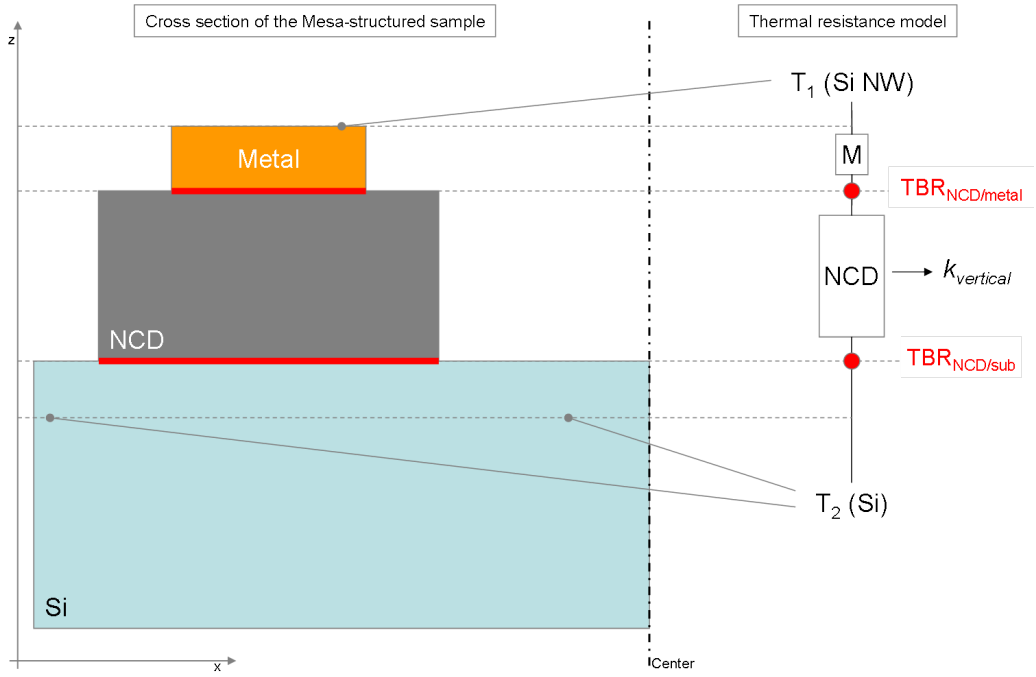


Figure 8.16: Schematic representing the cross section of a MESA-structured sample (left side) and its equivalent thermal resistance model (right side), in which the different contributions to the vertical heat transport are indicated by resistors in series.

According to this model, the vertical heat flux due to the temperature gradient $\Delta T = T_1 - T_2$ faces a thermal resistance $R_{th,vertical}$ on its way from the metal heater to the substrate, which is the series of three components:

$$R_{th,vertical} = TBR_{metal/NCD} + R_{NCD} + TBR_{NCD/sub} \tag{8.5}$$

where $TBR_{metal/NCD}$ and $TBR_{NCD/sub}$ are the thermal resistances at the interfaces between the metal heater and the NCD, and between the NCD and the Si substrate respectively, and $R_{NCD} = t_{NCD}/k_{vertical}$ is the volume resistance due to the film.

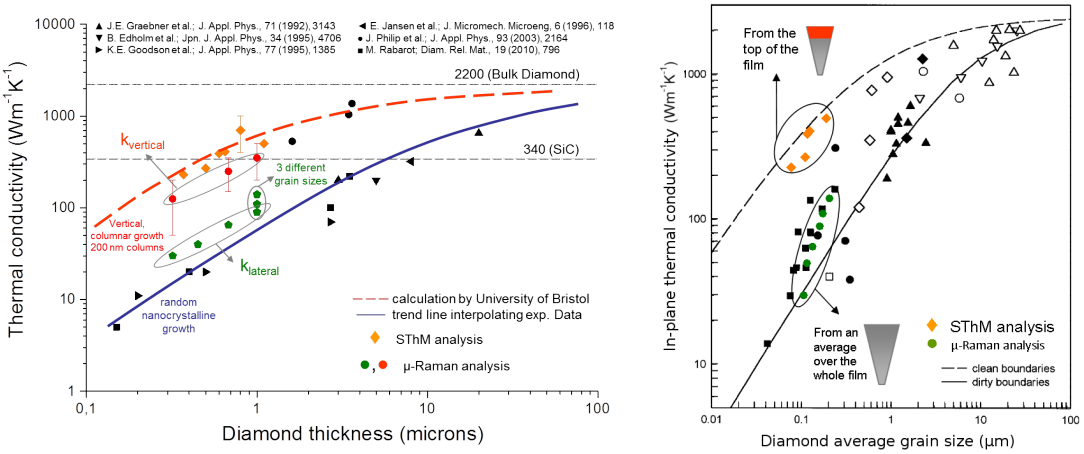
Since the thermal resistance of a 1 μm thick NCD film with $200 < k_{vertical} < 1000$ $Wm^{-1}K^{-1}$ lays in the range $0.1 - 0.5 \times 10^{-8}$ m^2K/W, it may be easily screened by the $TBR_{metal/NCD}$, which is of approx. 1×10^{-8} m^2K/W for Ti/NCD from [215, 216], and by the $TBR_{NCD/sub}$, which is of $\sim 0.5 \times 10^{-8}$ for our films.

To further improve the sensitivity of the μ-Raman technique to $k_{vertical}$ in thin, highly conductive diamond films would therefore be necessary to reduce the TBR at the interface metal/NCD, for instance by using heaters made of doped-NCD instead of the metal ones, or by adopting optical rather than electrical heat generation methods.

Summary and conclusions

At this point of the analysis, it is useful to put the numbers we obtained for our submicron films in a wider context comprising also the data collected in the past years by several groups investigating similar, as well as thicker, larger grain-sized CVD diamond films. Such a comparison would allow to verify and, whenever possible, extend the validity of our conclusions.

In Figure 8.17, the thermal parameters extracted on our films are compared with literature data [212, 167] collected on diamond films with thicknesses between 0.1 and 100 microns (a) and average grain-sizes between 0.01 and 100 microns (b).



(a) (b)

Figure 8.17: Thermal conductivity data found in literature [212, 167] for CVD diamond films spanning a wide range of thicknesses (a) and grain sizes (b), comprising the results of the analysis on our submicron NCD films.

Trend lines in plot (a) represent the predicted values of thermal conductivity according to theoretical calculations performed by the team at the University of Bristol[6], which consider the heat transport in different microstructures, namely one in which the diamond nanocrystals are randomly oriented and slowly growing with thickness, and one in which the columnar texture develops in a short distance from the interface with the substrate (i. e. with high γ-parameter) and the average column size is 200 nm.

Our data for the top part of the film agrees well with the columnar model and with the results of Phillip *et al.* [30] obtained on similar, columnar-structured NCD films. The average values are instead inherently influenced by the bottom region of the film, which has small in-plane grain-size and higher content of grain-boundaries, and hence they lay in an intermediate area between the two curves.

These conclusions are supported by plot (b), in which the continuous and dotted trend lines represent the expected thermal conductivities, when scattering within the diamond layer takes place at dirty and clean grain-boundaries respectively (see Section 5.2).

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Scattering rate is low, and thus $k_{lateral}$ is very close to the theoretical maximum, in the upper region of the film, which is made of large grains connected through clean grain-boundaries. The scattering taking place in the first hundreds of nanometers, where the grains have dimension of 10-20 nm, is instead strong and lowers significantly the average conductivity, the effect being more significant for thinner films, which are indeed closer to the dirty grain-boundary trend line.

CONCLUSIONS. In this chapter, the thermal properties of NCD films outgrown in a columnar way up to 1 μm and heated by resistive top heaters were characterized by means of scanning thermal microscopy and μ-Raman temperature detection techniques, with the aid of numerical simulations for the analysis.

Test structures were specifically designed and fabricated in order to extract relevant information on the thermal conductivity anisotropy of the films and correlate it with their microstructure. However, the correct interpretation of the temperature profiles obtained with each technique requires to take into account the boundary conditions in which each measurement is performed and in particular, the part of the film which is probed by each method (and thus its relative sensitivity).

The results of the characterization show that such NCD films are indeed heterogeneous, with a clear dependence of the thermal conductivity k on the film's thickness and in-plane grain size. With a lateral thermal conductivity above 300 $Wm^{-1}K^{-1}$ reached in the top part of the film, columnar NCD films approach the bulk thermal conductivity of high thermally conductive materials like SiC (300 $Wm^{-1}K^{-1}$ at RT [223, 161]) or AlN (270 $Wm^{-1}K^{-1}$ at RT [24]) already in the sub-μm range, and are therefore promising for the thermal management and self-heating mitigation of GaN-based HEMTs when they are used as top heat-spreaders.

They also indicate that these films can spread the heat more efficiently by vertical conduction along the columns (with $k_{vertical}$ up to 1000 $Wm^{-1}K^{-1}$), rather than laterally across them (with an anisotropy ratio of ~ 3).

Furthermore, the evaluation of the thermal properties of the highly-resistive nucleation region in proximity of the substrate on our BEN-nucleated films, whose thermal boundary resistance (R_{th})s (*TBR*s) may be as low as 5×10^{-9} m^2K/W, prove that the BEN pre-treatment allows to achieve perhaps the best possible thermal contact between the diamond film and the material on which it is deposited.

Finally, the results of the thermal characterization strongly suggest that in order to grow thin NCD films with high thermal conductivity, it is crucial to use growth parameters promoting the earliest development of large grains in the shortest distance from the substrate. For instance, a gain of approx. 50% in lateral thermal conductivity was measured for films outgrown to the same total thickness, but with higher grain growth gradient γ.

9

SUMMARY AND CONCLUSIONS

Among all the unique properties diamond possesses, its exceptional thermal conductivity is perhaps the most appealing for GaN-based power electronics, which currently faces the challenge of managing the huge thermal load due to the high power densities enabled by GaN HEMT power devices.

For thermal management purposes, diamond can be integrated either on the substrate side or on the device side of the GaN HEMT structure. In both cases, it should act as an ideal heat-spreader able to efficiently remove the heat from the channel and to transfer it to the ultimate heat-sink, thus mitigating the self-heating effect. However, seamlessly integrating a diamond heat-spreader with a GaN HEMT proved to be a technical challenge both on the substrate-side (i. e. GaN-on-diamond), in which GaN needs to be glued or grown on a diamond substrate, and on the device-side (i. e. diamond-on-GaN), in which the HEMT needs to be coated with a thin, high thermally conductive diamond overlayer.

In this work, the latter approach has been thoroughly investigated, firstly by exploring the correlation between growth parameters and film microstructure in BEN-nucleated, thin nanocrystalline diamond (*NCD*) films in the submicron range of thicknesses, with the scope of identifying the growth conditions leading to high thermally conductive films, at the lowest thermal budget.

Subsequently, by performing overgrowth experiments of gate-less and fully-processed InAlN/GaN HEMTs with NCD to identify and to gradually improve (or even replace) the HEMT components detrimental for the device stability at high temperature, eventually leading to fully-functional, NCD-coated HEMTs.

And finally, by characterizing the anisotropic thermal properties of the NCD overlay by means of scanning thermal microscopy (*SThM*) and μ-Raman thermography, applied to test structures specifically designed and fabricated to study independently the heat transport in the lateral and vertical directions.

The results of the structural characterization performed by SEM, AFM and TEM at each stage of the deposition for NCD films prepared with different growth recipes, allowed to identify the most suitable conditions to be used during the nucleation phase and clearly showed the influence the growth parameters have on the development of film's microstructure.

Concerning the nucleation stage, the results of TEM analysis showed that when bias enhanced nucleation (*BEN*) is performed on a Si-based substrate (either crystalline or amorphous), the topmost part of the substrate reacts with the carbon radicals, thus forming cubic SiC particles of 2-3 nm size in direct contact with the surface and a 5-20 nm thick, amorphous-C transition layer on top of which the diamond phase starts to nucleate. They also indicated that structure, composition, and spatial extension of this disordered region at the interface with the substrate depend on the BEN process parameters. For our HFCVD reactor, the quality of the interface seemed indeed to be extremely sensitive to both filaments and substrate temperatures

during the BEN. NCD films with the thinnest (<10 nm) disordered region between Si substrate/diamond overlayer and high nucleation densities above 10^{10} cm^{-2} were obtained by keeping the filaments temperatures above 2150 °C and the substrate temperature above 730 °C for the 2 hours of the BEN process.

Structural characterization after the outgrowth stage indicated methane concentration and substrate temperature as the parameters with the greatest impact on the film microstructure, both in terms of controlling the α-parameter (i. e. shape and size of the crystals), as well as in terms of non-diamond components embedded in the layer (i. e. graphite content and grain boundary density).

At methane concentrations of a few percent (>1.2% in our HFCVD) and low substrate temperatures (<650 °C), a strong diamond re-nucleation takes place, which combined with a high α value leads to a 3D structure with cauliflower-like crystals and a "small-grained" diamond film with extended grain boundaries network. Instead, a gas mixture with methane highly diluted in hydrogen (<0.5%) and substrate temperatures above 700 °C, drastically reduce the re-nucleation rate and the α value, thus resulting in a 2D-/columnar-structure whose grains have in-plane size of tens/hundreds of nanometers, linearly increasing with thickness in the first few microns, whereas their vertical extension can reach several micrometers.

The columnar-structured NCD films used in the HEMTs overgrowth experiments were grown using a methane concentration of 0.4% in hydrogen at substrate temperatures of 750 °C. With such a recipe, the NCD film is made of grains with high crystalline purity – indicated by the strong diamond peak and almost-absent graphite peak in the Raman spectrum – and average in-plane size of ~150–200 nm at 1 µm thickness. However, in such conditions the growth rate did not exceed 0.1-0.12 µm/h, and therefore required to fabricate GaN-based HEMTs able to withstand a plasma of hydrogen and methane radicals at 750 °C for several hours (approx. 5 and 10 hours for 0.5 and 1 µm layers respectively).

The overgrowth experiments clearly showed that the components used routinely to fabricate HEMTs in GaN technology are not stable at high-temperatures above 600 °C in the aggressive hydrogen plasma atmosphere in which the deposition of the diamond overlay is carried out. In particular, device passivation and contact metallization were identified as weak points for the thermal stability in extreme environments.

Surface passivation encapsulates both the barrier (AlGaN or InAlN) and GaN buffer layers and should prevent them to be decomposed by the H-plasma. However, we found out that most ex-situ dielectric films used as device passivation have a hydrogen content which may reach 30% of their volume and may cause explosive outgasing during the outgrowth process. Significant effort was spent to develop PECVD-deposited SiO_2, silicon nitride and Si oxy-nitride thin films, as well as ALD-deposited Al_2O_3 and in-situ silicon nitride layers, which are stable after prolonged thermal stress in the diamond reactor.

By studying the failure mechanisms of the contact metallization after diamond overgrowth of gate-less HEMTs, it became clear that the gold component used in the ohmics stack was prone to electromigrate under the effect of high thermal budgets and bias applied to the device. Therefore, new metal stacks were adopted for the ohmics and the gate, in which gold was replaced by copper or by refractory metals

molybdenum and tantalum: Ti/Al/Ni/Cu (or Ti/Al/Ni/Ta) for the ohmics, and Cu/Pt or Mo for the gate Schottky contact.

This improved processing routine allowed indeed to coat fully-fabricated InAlN/-GaN HEMT devices with 0.5, 1.0 and 2.8 μm NCD films, deposited at a temperature of 750 °C, while largely preserving their DC and RF electrical characteristics. The maximum drain current density of about 1.3 A/mm and cut-off frequency f_t of 16.8 GHz of the devices with 0.5 μm gate length and 1 μm NCD cap are the highest ever achieved for diamond-coated HEMTs.

Although thicker NCD overlays were also demonstrated in this work (2.8 μm being the thickest diamond overcoat realized on a GaN-based HEMT to date), it may not be necessary to grow such thick layers, which require 3 times the thermal budget needed for the 1 μm coating.

In fact, as the the results of the thermal characterization show, columnar NCD films may reach high thermal conductivities already in the submicron range of thickness, with peak values measured by *SThM* of 300 $Wm^{-1}K^{-1}$, when the heat spreads mostly laterally in the film, and up to 1000 $Wm^{-1}K^{-1}$ when the heat is extracted from the top of the layer through vertical conduction.

However, they also show that their average thermal conductivity (measured by μ-Raman) is approximately three times lower, due to the influence of the highly thermally-resistive region located in the first hundreds of nanometers from the substrate, comprising the nucleation layer, which is the most defective part of the film, and the coalescence layer, where the in-plane dimensions of the grains does not exceed 70–80 nm. Although the evaluation of the thermal properties of the nucleation region on our BEN-nucleated films showed that *TBR* as low as 5×10^{-9} m^2K/W may be reached, further effort has to be devoted to improve the thermal properties of the coalescence region, before the higher thermal conductivities achieved in the upper part of the film in layers thicker than 1 μm could be exploited.

A way to improve the heat transport properties of the coalescence region has been suggested in this work, which consists in using growth parameters promoting the earliest development of large grains in the shortest distance from the substrate (i. e. maximizing the grain growth gradient γ). Initial results on the thermal characterization of thin films outgrown to the same total thickness of 1 μm, but with different γ-parameter, showed that the film with the highest γ had approx. 50% higher average lateral thermal conductivity than the film used as a reference (140 vs 90 $Wm^{-1}K^{-1}$).

Besides the thermal properties of the NCD film itself, the effectiveness of the top heat extraction approach depends also on the thermal properties of the passivation layer and of the Si-based nucleation interlayer, since the heat from the GaN channel has to cross them before reaching the diamond heat-spreader.

It was suggested in this work that if the nucleation interlayer is thin enough, it could initially supply the bias necessary to nucleate diamond on the HEMT passivation, but be completely consumed during the process, thus not adding any additional thermal resistance to the stack. The ideal case would therefore be to use such a thin nucleation interlayer for nucleating diamond on HEMT devices passivated in-situ with nm-thick dielectric layers. Although requiring further optimization, the overgrowth experiment performed on InAlN/GaN HEMTs passivated with in-situ SiN reported in this work represents the first successful step in this direction.

Finally, the work of this thesis has laid the basis for the growth and characterization of thin nanocrystalline diamond films to be used in the fabrication of diamond-coated GaN-based HEMTs, whose concept is one of the most promising for the thermal management of high power GaN-based devices, but whose realization has proven technologically very challenging.

Taking into account that equally important efforts have been spent in recent years on the substrate-side approach, i. e. growing a GaN heterostructure directly onto a diamond substrate, and that the first HEMT devices have been demonstrated, which could handle nearly three times the power of GaN-on-SiC counterparts at the same channel temperature, it is not difficult to envision a GaN-based HEMT structure sandwiched in between a (polycrystalline) diamond substrate and a (nanocrystalline) diamond overlayer. Not only such a structure would allow to remove and spread the heat generated in the channel at a fast pace, but by encapsulating the device in a highly corrosion-resistant diamond packaging, it would also be possible to use aggressive heat extraction methods, which are beyond the reach of any other material and far superior to a passive heat-sink, as for instance liquid and explosive evaporation cooling.

In light of the work here presented and of proof-of-concept experiments currently available, it seems the building blocks needed to realize such a concept are already in place.

A

APPENDIX

A.1 THEORY OF LATTICE THERMAL CONDUCTIVITY

At temperatures higher than 0 K, atoms in solids are not at rest, but vibrate about their equilibrium positions and the displacement of each atom is strongly coupled with neighboring atoms.

Considering the atoms of a crystal lattice as a chain of harmonic oscillators with mass M and spring constant K, set at a distance a apart from each other, it is possible to calculate the normal modes of vibration of the lattice [224].

In case of a 1D lattice, the solution to the wave equation, which describes the motion of each atom can be expressed by the following:

$$\omega(q) = 2\sqrt{\frac{K}{M}}\left|\sin(qa/2)\right|. \tag{A.1}$$

Such a relation $\omega(q)$ between frequency ω and wavenumber q of the waves propagating along the crystal is called *dispersion relation*. If the linear chain comprises two different atoms with masses M_1 and M_2, the solution to the wave equation results in two branches of the dispersion relation, labeled acoustic (ω_-) and optical (ω_+) branch respectively:

$$\omega_\pm^2 = K\left(\frac{1}{M_1}+\frac{1}{M_2}\right) \pm K\sqrt{\left(\frac{1}{M_1}+\frac{1}{M_2}\right)^2 - \frac{4\sin^2(qa/2)}{M_1 M_2}}. \tag{A.2}$$

In the low-frequency acoustic branch the atoms in a unit cell move in phase, while in the high-frequency optical branch the atoms move out of phase. If the masses M_1 and M_2 are equal there is no gap between acoustic and optical branches.

In a 3D lattice with N types of atoms per unit cell, there will be three acoustic branches and $3(N-1)$ optical branches. Examples of the dispersion curves for monatomic and diatomic lattices are shown in Figure A.1.

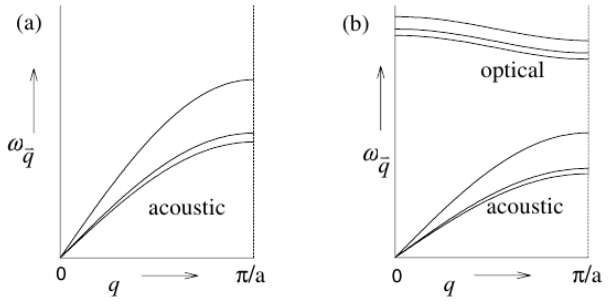


Figure A.1: Schematic phonon dispersion curves for a given direction of q of (a) monatomic lattice and (b) diatomic lattice. The lattice parameter is denoted a.

The quanta of the lattice vibrational field are called *phonons* [225]. The average number of phonons with wave vector q present in the crystal follows a phonon distribution function N_q, that in equilibrium can be written as:

$$N_q^0 = \frac{1}{exp(\hbar w_q / k_B T) - 1}. \tag{A.3}$$

In the presence of a temperature gradient the phonon distribution is driven out of equilibrium (i. e. $N_q^0 \to N_q$) and thermal energy propagates in the crystal by means of wave packets consisting of various normal modes [226]. Since at low frequencies the optical branch is characterized by a vanishing group velocity $v_g = d\omega/dq$, most of the heat transport occurs in the lattice via the acoustic branch. Even if the optical phonons are not effective in transporting heat directly, they may influence the heat conduction by interacting with the acoustic phonons (especially in the high temperature range).

According to the Boltzmann equation, scattering processes restore the phonon distribution N_q to N_q^0 at a rate proportional to the departure from equilibrium:

$$\frac{N_q - N_q^0}{\tau_q} = -(v_g \cdot \nabla T)\frac{\partial N_q^0}{\partial T}, \tag{A.4}$$

where v_g is the group velocity and τ_q is the phonon scattering relaxation time.

The total heat flux carried by all phonon modes can be written as

$$Q = \sum_q N_q \hbar w_q v_g \tag{A.5}$$

$$= -\sum_q \hbar w_q v_g^2 \langle \cos^2\theta \rangle \tau_q \frac{\partial N_q^0}{\partial T} \nabla T \tag{A.6}$$

$$= -\frac{1}{3}\sum_q \hbar w_q v_g^2 \tau_q \frac{\partial N_q^0}{\partial T} \nabla T, \tag{A.7}$$

where θ is the angle between v_g and ∇T.

According to Fourier's law of heat conduction, the lattice thermal conductivity k is defined as the ratio between heat flux Q and temperature gradient ∇T in Eq. A.7:

$$k = -\frac{Q}{\nabla T} = \frac{1}{3}\sum_q \hbar w_q v_g^2 \tau_q \frac{\partial N_q^0}{\partial T} \tag{A.8}$$

$$= \frac{1}{3}\int \hbar w_q v_g^2 \tau_q \frac{\partial N_q^0}{\partial T} f(w) dw, \tag{A.9}$$

where k has the units of $W m^{-1} K^{-1}$ and the summation over q have been replaced by the integral in $f(\omega)d\omega$, with $f(\omega)$ phonon density of states.

Physically, *k* expresses the response of a material to a temperature gradient, whereas materials with high *k* are able to carry a larger heat flux compared to the ones with low *k*.

On the other hand, *k* describes the temperature gradient established in a material in response to an inward (or outward) heat flux, the higher the *k*, the lower the ∇T.

From Eq. A.9 it is clear that the evaluation of k for a material requires knowledge of its phonon-dispersion relation ω_q, phonon density of states $f(\omega)$ and phonon relaxation-time τ_q [227, 228, 229, 230, 231].

For a proper calculation of the density of states $f(\omega)$ it is essential to obtain numerical values of the phonon-dispersion relation ω_q for a large number of wave vectors q within the irreducible part of the Brillouin zone of the solid under consideration.

Figure A.2 shows the the phonon-dispersion relation and the density of states calculated for diamond, as reported in [232]. It can be seen that due to the presence of two carbon atoms per primitive unit cell, there are six phonon branches. With increasing energy near the Brillouin zone center Γ these branches are labeled: T1A (slow transverse acoustic), T2A (fast transverse acoustic), LA (longitudinal acoustic), T2O (fast transverse optical), T1O (slow transverse optical) and LO (longitudinal optical).

The density of states shows a few characteristic peaks, corresponding to the flatness of the dispersion curves for the various polarization branches.

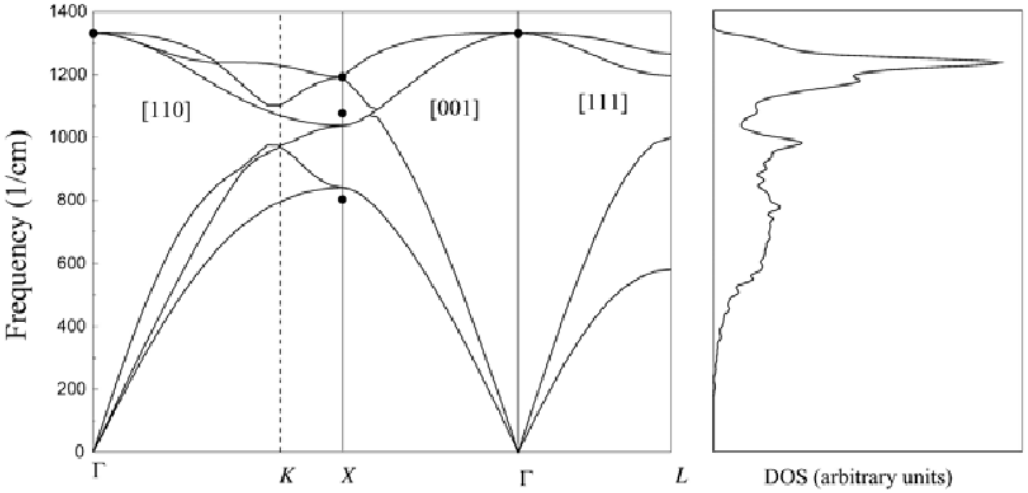


Figure A.2: Phonon-dispersion curves and density of states for diamond. The results are obtained from the application of a bond charge model [232]. Experimental measurements are indicated by filled circles.

Since the thermal conductivity calculation according to Eq. A.9 becomes complex and time consuming when considering the actual phonon-dispersion relation and density of states, most calculations are usually carried out by using simplified forms of ω_q and $f(\omega)$.

One particularly simple scheme is provided by the so-called *isotropic continuum model* in the Debye cutoff scheme [227]. In this scheme the realistic Brillouin zone for a three-dimensional cubic system is replaced by a Debye sphere of radius q_D and the phonon-dispersion relation is simplified to the linear form $\omega_q = q \cdot v$ for all directions of q with v sound velocity in solids. This relation is certainly true in the long wavelength (i. e. small q) limit.

The size of the Debye sphere is large enough to contain the correct number of acoustic phonon modes (3N modes for a crystal with N atoms):

$$3N = \int_0^{w_D} f(w)\,dw \tag{A.10}$$

where w_D is the Debye frequency, which is defined here as the maximum vibrational frequency of a given mode in a crystal. For acoustic modes, this corresponds to the frequency at the zone boundary.

The density of states within the isotropic continuum model is given by the following simple expression:

$$f(w)dw = \frac{3w^2}{2\pi^2 v^3}dw \tag{A.11}$$

Figure A.3 shows the phonon-dispersion curve and the density of states within the Debye model for a single polarization branch. The density of states increases quadratically with increasing phonon frequency, but in contrast to the real situation (cfr. Fig. A.2) there are no characteristic peaks.

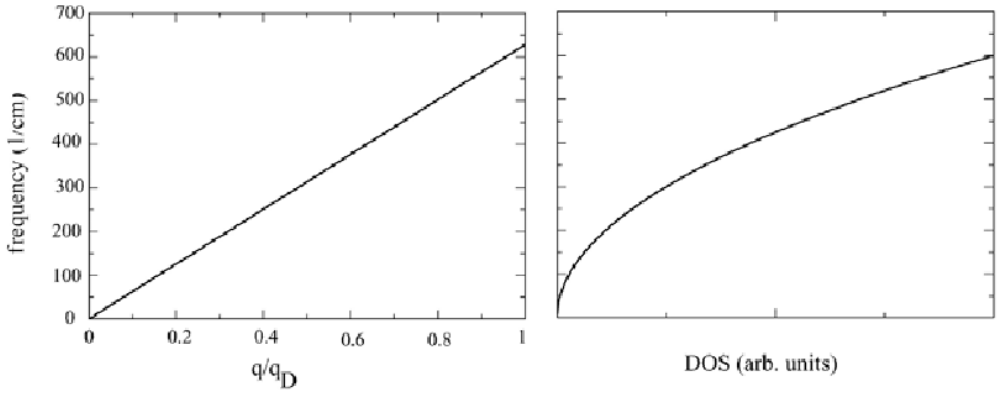


Figure A.3: (left) Phonon-dispersion curve and (right) density of states (DOS) for a single polarization branch within the Debye model of a three-dimensional isotropic continuum.

Using the Debye assumptions and the expression of N_q^0 from Eq. A.3, Eq. A.9 yields

$$k = \frac{1}{2\pi^2 v}\int_0^{wD} \hbar w^3 \tau_q(w) \frac{(\hbar w/k_B T^2)exp(\hbar w/k_B T)}{[exp(\hbar w/k_B T)-1]^2}dw. \tag{A.12}$$

Making the substitution $x = \hbar w/k_B T$ and defining the Debye temperature $\theta_D = \hbar w_D/k_B$ as the temperature above which all vibrational modes in a crystal are excited, Eq. A.12 becomes

$$k_{Debye} = \frac{k_B}{2\pi^2 v}\left(\frac{k_B}{\hbar}\right)^3 T^3 \int_0^{\theta_D/T} \tau_q(x)\frac{x^4 e^x}{(e^x-1)^2}dx, \tag{A.13}$$

which is usually called the *Debye approximation* for the lattice thermal conductivity.

This expression can be viewed as the result of the kinetic theory by introducing the lattice specific heat $C(x)$:

$$C(x) = \frac{3k_B}{2\pi^2 v^3}\left(\frac{k_B}{\hbar}\right)^3 T^3 \frac{x^4 e^x}{(e^x-1)^2} \tag{A.14}$$

such that

$$k_{Debye} = \frac{1}{3}\int_0^{\theta_D/T} v^2 \tau_q(x) C(x)dx = \frac{1}{3}\int_0^{\theta_D/T} C(x) v l(x)dx, \tag{A.15}$$

where $l(x) = v\,\tau_q(x)$ is the mean free path of the phonons.

Once the formula for the lattice thermal conductivity has been derived the problem is to calculate the phonon relaxation times $\tau_q(x)$.

Finite sample size, static imperfections, alloying and inhomogeneity, and anharmonicity in crystal potential provide the main phonon-scattering sources in nonmetallic solids. Each mechanism acts in limiting the lifetime of phonons.

Although anharmonicity gives rise to an *intrinsic relaxation time*, other mechanisms produce *extrinsic relaxation times*. Thus the actual relaxation time $\tau_q(x)$ will be calculated as follows:

$$\tau_q^{-1}(x) = \tau_{intrinsic}^{-1}(x) + \sum_i \tau_{extrinsic,i}^{-1}(x) \tag{A.16}$$

A list of the main extrinsic mechanisms $\tau_{extrinsic,i}$ follows.

BOUNDARY SCATTERING. It is the dominant scattering mechanism at low temperatures, where the phonons acquire long wavelengths and the main source of scattering is the sample size. The phonon relaxation rate due to boundary scattering is independent of the phonon frequency and temperature and can be written as:

$$\tau_B^{-1} = \frac{v}{d} \tag{A.17}$$

where d represents an effective boundary mean free path, i.e. the sample size for a single crystalline material or the grain size for a polycrystalline sample.

SCATTERING FROM POINT-DEFECTS. Static point imperfections in solids, such as isotopes, substitutional impurities with different masses, impurities causing changes in atomic force constants, and single and aggregate vacancy defects, can strongly scatter phonons. For phonons with longer wave-lengths compared with the imperfection size, the scattering rate will follow a Rayleigh law, that is, it increases as the fourth power of phonon frequency ω [225]:

$$\tau_{PD}^{-1} \approx \omega^4 \tag{A.18}$$

SCATTERING FROM EXTENDED-DEFECTS (E.G. IMPERFECTION AGGREGATES, STACKING FAULTS). According to the size s of the extended defect, the relaxation rate may assume the Rayleigh ω^4 form for phonons with long-wavelength λ, or change to ω^2 for the ones with short wavelengths [233, 234, 225],

$$\tau_{ED}^{-1} \approx \omega^4, \quad \lambda > s \tag{A.19}$$

$$\tau_{ED}^{-1} \approx \omega^2, \quad \lambda < s \tag{A.20}$$

SCATTERING FROM DISLOCATIONS. The phonon scattering rate for scattering from the strain field surrounding a dislocation has the form [235]:

$$\tau_D^{-1} \approx \omega \tag{A.21}$$

The intrinsic phonon scattering processes $\tau_{intrinsic}$ included in the Debye model are phonon-phonon interactions that do not conserve the total crystal momentum,

giving rise to thermal resistance. Such processes are called *Umklapp processes*, or U-processes (flip-over in German), with phonon scattering rate τ_U^{-1} given by:

$$\tau_U^{-1} \propto T \exp\left(\frac{\theta_D}{T}\right) \approx \frac{\hbar\gamma^2}{Mv^2\theta_D}\omega^2 T \exp\left(-\frac{\theta_D}{3T}\right), \tag{A.22}$$

with the Grüneisen constant γ and an average atomic mass in the crystal M.

There exist, however, other non-resistive and crystal-momentum-conserving processes which do not contribute to the thermal resistance, but may still have a profound influence on the lattice thermal conductivity and are called *Normal processes*, or N-processes. A modified expression of the lattice thermal conductivity taking into account such processes has been elaborated by Callaway [229] replacing the relaxation time τ_q by τ_C such that:

$$\tau_C^{-1} = \tau_q^{-1} + \tau_N^{-1} \tag{A.23}$$

with

$$\tau_N^{-1} = B w^a T^b \tag{A.24}$$

where B is a constant independent of w and T; the values (1,3) for the parameters (a, b) have been indicated for diamond in [236], while (1, 4) and (2, 3) were used for group IV and III-V semiconductors in [237].

The resulting lattice conductivity is expressed by the sum of k_{Debye} given in Eq. A.13 and an additional term k_N for the N-processes contribution:

$$k = k_{Debye} + k_N \tag{A.25}$$

Whereas the Callaway model is necessary to interpret experimental data on pure materials, the thermal conductivity behavior in solids with a large concentration of lattice defects or appreciable amount of isotopes can be well predicted by Debye's simplified model.

A.1.1 *Temperature dependence of the thermal conductivity*

According to Equations A.13 and A.15, the temperature variation of the lattice conductivity k is governed by the joint temperature variation of the lattice specific heat C and phonon relaxation time τ_q.

The lattice specific heat rises as T^3 at very low temperatures and saturates to a constant at high temperatures, as described in Debye's theory of specific heat [238]. The phonon relaxation time τ_q is dominated by boundary scattering, and hence has no temperature dependence, at very low temperatures, and by an-harmonic interactions (i.e. three-/four-phonon processes) with T^{-1} behavior at high temperatures.

Therefore the thermal conductivity of a bulk material (see Figure A.4) will rise steeply as T^3 at very low temperatures and decrease with temperature as T^{-1} in the high-temperature limit. It will reach a maximum in the intermediate temperature region, whose location will be determined mostly by phonons scattering from defects and impurities.

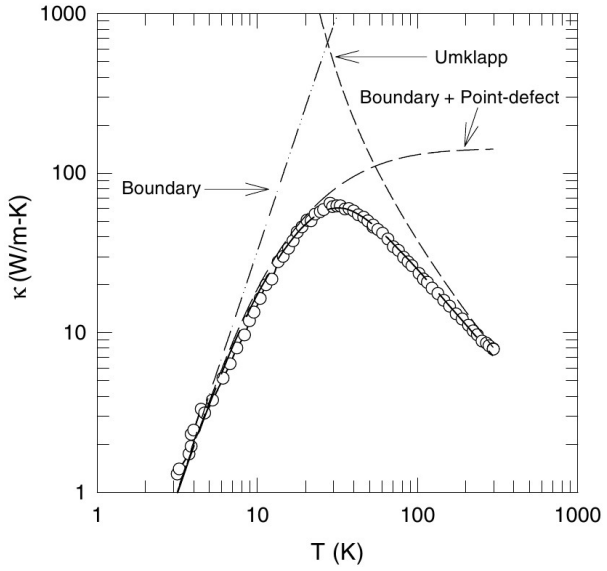
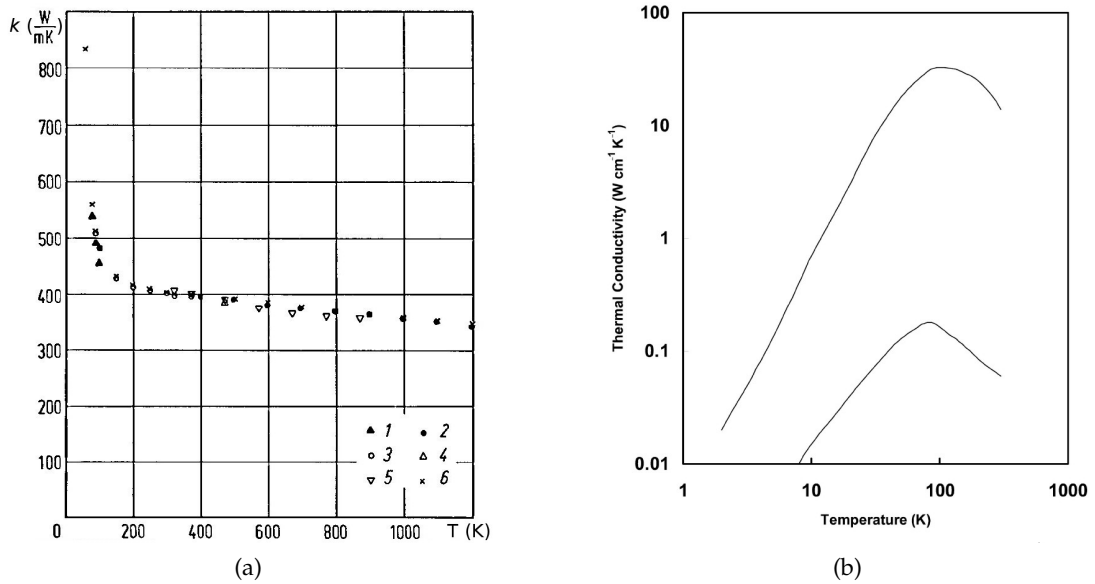


Figure A.4: General trend of the lattice thermal conductivity versus temperature for a solid. The dashed curves are the theoretical limits imposed on the phonon heat transport by boundary scatterings, by a combination of boundary plus point-defect scatterings, and by umklapp scatterings.

A.1.2 *Thermal conductivity of various materials*

COPPER. Figure A.5a shows the thermal conductivity of Cu as a function of temperature as found in [239]. The curve conform to the predictions for the thermal conductivity of metals, in which heat is carried by both electrons and phonons (see [240] for the theory). An essentially constant thermal conductivity at high-temperatures, in the range 340–400 $Wm^{-1}K^{-1}$, gives way to a rapidly rising thermal conductivity at lower temperatures, with a peak of ~900 $Wm^{-1}K^{-1}$ at $T \sim \theta_D/15 \simeq 70\,K$, which results from the competing influence of electron-phonon and electron-impurity scattering. Below that temperature an approximately linear decrease of thermal conductivity is expected, as impurity scattering dominates the transport.

GRAPHITE. In Figure A.5b the thermal conductivity of (highly oriented polycrystalline pyrolytic) graphite is plotted against temperature (from [214], p. 56). In graphite the highly anisotropic nature of bonding (covalent sp^2 within a plane and weak Van der Waals between planes) manifests itself as an enormous anisotropy in the conduction of heat. Because of the crystal symmetry there are only two principle conductivities: the in-plane k, and that perpendicular to the plane (along the so-called c-axis), with a peak of ~4000 and 20 $Wm^{-1}K^{-1}$ respectively for a temperature of ~100 K. The curves in Fig. A.5b for in-plane and c-axis thermal conductivity represent an average of many measurements (see [214] and references within).

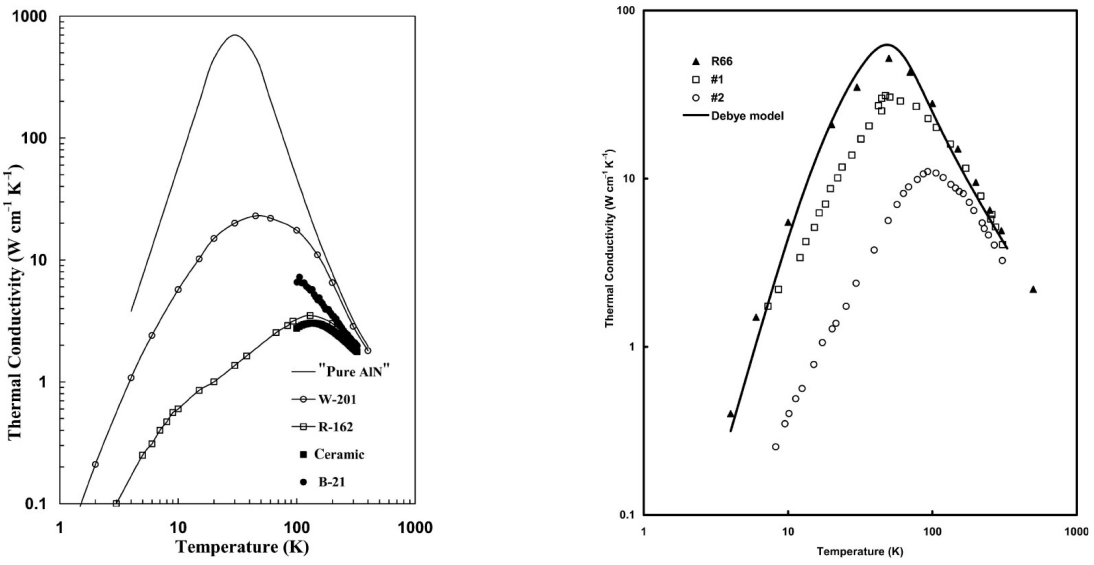


(a) (b)

Figure A.5: Thermal conductivity of Cu (a, from [239]), measured on 6 different samples (number 1 to 6 in the inset) and highly oriented graphite (b, from [214]): in-plane [upper line] and out-of-plane [lower line] components.

ALUMINUM NITRIDE. Figure A.6a shows the thermal conductivity of single-crystal AlN as a function of temperature for samples with different amount of oxygen impurities (340 ppm for W-201, 1000 ppm for R-162) (from [214], p. 61). The oxygen content determines large differences in the thermal conductivity, where the purest sample has a RT thermal conductivity of ~350 $Wm^{-1}K^{-1}$, while those containing higher quantities of oxygen impurity have a lower conductivity, characterized by a depression in the curve as a function of temperature.

SILICON CARBIDE. In Figure A.6b the thermal conductivity of single crystalline SiC is plotted against temperature, for a crystal with no impurities and for crystals with different electron concentrations (from [214], p. 58). Samples with higher electron concentrations (#1 and #2 in the Figure) have lower thermal conductivity than the one predicted by the Debye model, an effect ascribed to scattering of phonons by electrons in an impurity band.



(a) (b)

Figure A.6: (a) Thermal conductivity of single-crystal AlN. "Pure AlN" is the calculated result for a crystal containing no impurities; samples W-201, R-162, and B-21 are single crystals with varying amounts of oxygen concentrations. A ceramic sample is shown for comparison. (b) Thermal conductivity of various single crystals of SiC: R66, pure crystal; #1 and #2, crystals with electron concentrations of 3.5×10^{16} and 2.9×10^{18} cm^{-3} respectively (from [214]).

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