



Thin Body InAlN/GaN HEMT Technology on Sapphire:
Special Focus on High-Temperature and Electrochemical
Applications

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Abstract

This thesis is dedicated to the investigation of lattice-matched InAlN/GaN high electron-mobility transistors (HEMTs) for their application in high-temperature electronics and in electrochemical sensor systems. In this work, this refers to ambient temperatures as high as 600 °C or to the application in corrosive liquid media, like strong acidic (pH = 1) or alkaline (pH = 13) solutions. These two environments cannot be addressed with conventional silicon (Si) or gallium arsenide (GaAs) devices, but can be accessed using a more robust, more thermally stable material like the lattice-matched InAlN/GaN heterostructure. However, to further enhance performance and stability the proposed electrochemical sensor comprises an InAlN/GaN HEMT and, as the actual chemical sensor, an inert boron-doped diamond (BDD) electrode applicable for pH measurements or redox signal detection.

The integration with diamond and, apparently, the operation at elevated temperatures require a thermally stable HEMT. Additionally, both applications also require HEMTs exhibiting low overall device leakage characteristics. Therefore, in this work a new GaN-on-Sapphire (GOS) HEMT technology comparable to the Silicon-on-Insulator (SOI) technology was developed, capable of reducing parasitic leakage currents through the gate diode, through the buffer, and between separate contact pads (also between separate devices). Here, GOS implies the oxidation of the InAlN barrier, employment of a thin body (as thin as 50 nm GaN buffer + 50 nm AlN nucleation layer) material stack on sapphire, and the confinement of the active device mesa by dry-etching to small islands on the sapphire substrate.

At room temperature, 0.25 μm gate length devices prepared in this GOS technology exhibit an output current density of $I_{\text{DS}} = 0.4 \text{ A/mm}$ and a threshold voltage of $V_{\text{th}} = -1.4 \text{ V}$. The residual off-state current is 1 pA nearly independent of the gate width and the subthreshold swing is 73 mV/dec. The resulting current on/off ratio is larger than 10^{10} , increased by 3 orders of magnitude compared to HEMTs prepared in a conventional device technology. Up to 600 °C such GOS HEMTs allow operation exploiting the full modulation range, i.e. from below threshold ($V_{\text{GS}} = -2 \text{ V}$) to fully open channel ($V_{\text{GS}} = +2 \text{ V}$). The corresponding device characteristics, e.g the maximum drain current, the transconductance, and the 1 MHz large signal output power, change only within less than 10 %. The residual off-current at 600 °C is approximately $I_{\text{off}} = 10 \text{ nA}$ ($W_{\text{G}} = 50 \mu\text{m}$) resulting in an, at this temperature, high current on/off ratio larger than 10^6 .

The electrochemical sensor system is analyzed with respect to two different measurement techniques yielding two essential combinations of the BDD electrode and the InAlN/GaN

HEMT. Measurements of the pH are conducted in an extended gate ion-sensitive field-effect transistor (ISFET) configuration, where the electrode is connected to the HEMT gate. In the second measurement configuration the electrode is connected to the drain and the HEMT is used as switch to turn on or off redox reactions at the BDD electrode. To achieve optimal performance the two individual elements have to meet certain requirements, although in this case such requirements are mainly established by the electrode. Such boundary conditions are derived from individual BDD electrodes and are, e.g. the potential window of approximately 2.8 V, the background current of 0.1 nA, the resulting redox current, and the equivalent circuit of the BDD/electrolyte interface. Cyclic voltammetry, capacitance voltage measurements as well as electrochemical impedance spectroscopy were used to extract the relevant parameters and helped to derive design recommendations for the HEMT, in turn allowing a full exploitation of the HEMT saturation or subthreshold regime in the corresponding measurements. As ISFET the sensor system exhibits a high linearity over the whole pH scale with a pH sensitivity of 5 mA/mm per ΔpH or 3.1 pH/dec in the subthreshold regime. As switch the HEMT is capable to completely turn on and off the redox reactions (in the nA regime), where the transfer region between on and off is less than 200 mV.

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List of Abbreviations and Symbols

List of Acronyms

| | |
|--------------|--|
| 2DEG | Two-Dimensional Electron Gas |
| 2DHG | Two-Dimensional Hole Gas |
| Al | Aluminum |
| AlGaN | Aluminum Gallium Nitride |
| AlN | Aluminum Nitride |
| BDD | Boron-Doped Diamond |
| BEN | Bias-Enhanced Nucleation |
| CV | Capacitance-Voltage |
| CVD | Chemical Vapor Deposition |
| DHFET | Double Heterostructure Field-Effect Transistor |
| ϵ | Permittivity |
| E_C | Conduction Band Energy |
| E_F | Fermi Energy |
| E_G | Band Gap |
| E_{SD} | Surface Donor Energy |
| E_V | Valence Band Energy |
| ΔE_C | Conduction Band Offset |
| F_{pol} | Polarization Field |
| FET | Field-Effect Transistor |
| g_m | Transconductance |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| GOS | GaN-On-Sapphire |
| HEMT | High Electron-Mobility Transistor |
| HFCVD | Hot-Filament Chemical Vapor Deposition |
| HTMC | High-Temperature Measurement Chamber |
| InAlN | Indium Aluminum Nitride |
| InGaN | Indium Gallium Nitride |
| InN | Indium Nitride |
| ISFET | Ion-Sensitive Field-Effect Transistor |
| μ | Electrochemical Potential |
| μ_C | Chemical Potential |
| μ_{el} | Electron Mobility |

| | |
|----------------|---|
| MEA | MicroElectrode Array |
| MEMS | Micro Electro-Mechanical System |
| MISHEMT | Metal-Insulator-Semiconductor High Electron-Mobility Transistor |
| MOCVD | Metal-Organic Chemical Vapor Deposition |
| MOSFET | Metal-Oxide-Semiconductor High Electron-Mobility Transistor |
| n_S | 2DEG Sheet Charge Carrier Concentration |
| Φ_{SB} | Schottky Barrier Height |
| Φ_{SP} | Surface Potential |
| P_{SP} | Spontaneous Polarization |
| P_{tot} | Total Polarization |
| PECVD | Plasma-Enhanced Chemical Vapor Deposition |
| Pt | Platinum |
| ρ_C | Specific Contact Resistance |
| R_{sh} | Sheet Resistance |
| RF | Radio Frequency |
| RIE | Reactive Ion Etching |
| RT | Room Temperature |
| RTA | Rapid Thermal Annealing |
| σ_{int} | Bound Interface density |
| SCE | Saturated Calomel Electrode |
| SEM | Scanning Electron Microscope |
| SHE | Standard Hydrogen Electrode |
| Si | Silicon |
| SiC | Silicon-Carbide |
| SiN | Silicon-Nitride |
| SOI | Silicon-On-Insulator |
| SS | Subthreshold Swing |
| TEM | Tunneling Electron Microscope |

List of Constants

| | | |
|-------|---------------------------------|------------------------|
| F | = 96485 C/mol | Faraday Constant |
| k_b | = 1.380×10^{-23} J/K | Boltzmann Constant |
| q | = 1.6022×10^{-19} C | Elementary Charge |
| R_g | = $8.314 \frac{J}{mol \cdot K}$ | Universal Gas Constant |

1 Introduction and Motivation

In terms of speed, efficiency, heat and power handling capability, wide band gap semiconductor devices are predicted to exhibit device performances beyond that of conventional silicon (Si) or gallium arsenide (GaAs) electronics. Such predications are based on the existence of the large band gap and on certain materials properties of the wide band gap materials. Some important material parameters of Si, GaAs, and the wide band gap materials silicon carbide (SiC), gallium nitride (GaN), and diamond are compared in table 1.1. A large band gap essentially means an increased distance between electrons in the conduction band and holes in the valence band, which makes devices less susceptible to impact ionization and is associated with a large breakdown field F_{br} . This allows for higher driving voltages at smaller device dimensions, thus potentially increasing speed and power density. The intrinsic carrier concentration n_i is also linked to the band gap E_G and, in case of Si, it is in the range of 10^{10} cm^{-3} at room temperature. In contrast, the intrinsic carrier concentration of wide band gap materials at room temperature is well below 1 cm^{-3} [1] leading to reduced noise and leakage, thus leading to a reduced overall power consumption. While their electron mobility μ_{el} is comparable to that of Si (except μ_{el} of SiC), the saturation velocity v_{sat} of the wide band gap materials is above that of Si, thus enabling high-power microwave devices based on wide band gap semiconductors.

Furthermore, III-Nitride semiconductors are robust materials exhibiting an exceptionally high thermal and chemical stability. This means that electronic devices compatible with harsh environments, that cannot be tolerated by conventional Si or GaAs devices, may be feasible using wide band gap materials. This, i.e. the development of electronic

| | Si | GaAs | GaN | SiC | Diamond ¹ |
|--|------|------|------|-----|----------------------|
| Band gap E_g [eV] | 1.1 | 1.4 | 3.4 | 2.9 | 5.45 |
| Electron mobility μ_{el} [cm^2/Vs] | 1500 | 8500 | 1500 | 900 | 2200 |
| Saturation velocity v_{sat} [10^7 cm/s] | 1.0 | 1.0 | 1.3 | 2.0 | 2.7 |
| Breakdown field F_{br} [MV/cm] | 0.3 | 0.6 | 5 | 3 | 100 |

Table 1.1: Selected material properties of Si, GaAs and the wide band gap materials SiC, GaN, and diamond at room temperature after [1, 2, 3, 4]. ¹ Values of limited technological use.

devices for harsh environments, is one aim of this work. Subject of chapter 4 will be high-temperature electronics, in this work up to 600 °C. Chapter 5 and chapter 6 will discuss chemical sensor applications also for the use in strong acidic ($\text{pH} = 1$) or alkaline ($\text{pH} = 13$) liquid media. Chemical sensor applications take advantage of the high corrosion resistivity and high-temperature electronics take advantage of the high thermal stability and the initially low intrinsic carrier concentration, where an extrapolation of n_i towards higher temperatures yields, that the room temperature carrier concentration of Si is reached at temperatures as high as 500 °C, 700 °C and 1250 °C for SiC, GaN, and diamond, respectively.

In this work, the materials chosen to address such applications were GaN and diamond. Diamond was chosen as chemical sensor, because of its superior chemical stability and inertness. Combined with its biocompatibility, high transparency, and especially the possibility to use it for potentiometric as well as for amperometric measurements, i.e. for pH tracking and the detection of redox reactions, diamond is the state-of-the-art material for chemical sensors applicable in aggressive media and in biomedical applications [5, 6, 7, 8]. Considering the material parameters, it would also present the ideal choice for the development of high-performance field-effect transistors (FETs). However, up to now diamond faces some severe technological challenges limiting the development of diamond electronic devices. Some of these hurdles, but also achievements in diamond technology are subject of chapter 5. Currently, the material superseding all others for the fabrication of high-grade electronic devices is GaN. Therefore, GaN was chosen for the development of high electron-mobility transistors (HEMTs) compatible with high temperatures and the integration with diamond electrodes for the fabrication of an electrochemical sensor system. Thus, such prepared sensor systems can take advantage of both, the superior chemical properties of diamond and the excellent electronic properties of GaN HEMTs. To accomplish a possible dual mode operation, i.e. pH tracking and detection of redox reactions, two different combinations of these two elements will be discussed in chapter 6, introducing the HEMT as transducer in an ion-sensitive field-effect transistor (ISFET) and as electronic switch to turn on and off redox reactions. Since they present the core elements, a large part of this work is dedicated to the description and analysis of GaN FETs (chapter 3) and diamond electrodes (chapter 5) in light of the two envisaged applications.

The term GaN HEMT usually refers to a material system comprising at least two of the group-III nitrides or nitride semiconductors. This material group is constituted of the binary compounds indium nitride (InN), aluminum nitride (AlN), and gallium nitride (GaN), their ternary alloys aluminum-gallium nitride (AlGaIn), indium-gallium nitride (InGaIn), indium-aluminum nitride (InAlIn) or even quaternary alloys thereof. In contrast to conventional HEMTs, a two-dimensional electron gas (2DEG) can be created without the need of intentional doping, but results from the high polarity of the nitride semiconductors. More precisely, the 2DEG is generated due to the polarization discontinuity at the heterointerface of two nitrides. The first GaN-based HEMT exploiting the high resulting polarization discontinuity, was established using an AlGaIn

barrier/GaN buffer heterostructure. However, today the InAlN/GaN heterostructure system is gaining increasing interest for the development of GaN-based HEMTs. The advantage of InAlN as barrier layer material is that it can be grown lattice-matched onto GaN when the Al-content is around 83 %. Thus, the material system experiences no strain, which potentially increases stability. As will be explained in chapter 3, a further advantage of such Al-rich alloys is a larger polarization discontinuity to GaN, thus leading to a high carrier concentration in the 2DEG, in case of the lattice-matched InAlN/GaN material system up to $2.6 \times 10^{13} \text{ cm}^{-2}$ [9]. Additionally, these high carrier densities can be achieved at thin barrier layer thicknesses, which would allow for further device scaling, while maintaining a rather high aspect ratio [2, 10, 11]. Hence, compared to more conventional AlGaIn/GaN HEMTs lattice-matched InAlN/GaN HEMTs can be faster with even higher power densities. Indeed, rather impressive results were obtained with this lattice-matched InAlN/GaN material system. A high output current density of 2.3 A/mm [12] and device operation at 1000 °C [13, 14] were already demonstrated, indicating a high capability in power applications and an extremely high, ceramic-like thermal stability. Its high-speed capability was recently demonstrated with a high transit frequency of $f_T = 370 \text{ GHz}$ at a gate length of 30 nm [15]. Output power densities of $P_{\text{out}} = 10 \text{ W/mm}$ at a frequency of 10 GHz were obtained with a rather conventional device technology [16]. Furthermore, normally-off, enhancement mode devices with a high output current density of 1.9 A/mm and a very high extrinsic transconductance of $g_m = 800 \text{ mS/mm}$ were obtained employing a gate-recess technology [17]. All these numbers express the high degree of maturity this material system already reached and are convincing arguments for the use of lattice-matched InAlN/GaN HEMTs in the two targeted applications. Additionally, because of its exceptional, ceramic-like stability, the lattice matched InAlN/GaN heterostructure is the only material system known presently, which allows the overgrowth of fully fabricated HEMTs with high quality polycrystalline diamond [18]. Therefore, this material system currently is the only material system allowing the realization of the envisaged electrochemical sensor system.

This previous statement can be made because the deposition of diamond films is linked to an extremely harsh growth process, especially if the film is prepared for electrochemical applications. Prepared for electrochemistry means that the amount of sp^2 -bonded carbon (graphitic phases) in the polycrystalline diamond film is low, which is necessary to exploit the full potential of diamond electrodes. This means a high chemical stability, a large potential window, i.e. the potential difference between hydrogen and oxygen evolution (electrolysis), and a low background current within the potential window [5, 19]. However, to this day diamond films of high electrochemical grade are obtained at growth temperatures above 750 °C [20]. Another prerequisite to allow electrochemical applications in terms of both, amperometric and potentiometric measurements, is a diamond layer exhibiting metal-like conductivity on the electrode surface. This is mostly realized by the deposition of a heavily boron-doped diamond (BDD) film, with a surface which is sensitive to the pH value, i.e. the concentration of hydronium ions (H_3O^+) in an electrolyte, but also allows for charge transfer across the BDD/electrolyte phase boundary. Compared to conventional noble metal electrodes such BDD electrodes can

then exhibit extraordinary device properties, like the large potential window of approximately $\Delta V = 3 \text{ V}$ ($\Delta V \approx 1.5 \text{ V}$ for metal electrodes) and a background current in the range of $\mu\text{A}/\text{cm}^2$ (compared to approximately mA/cm^2 of metal electrodes). This enables the detection of redox reactions, which usually occur at potentials outside the stability window of water and allows the detection of lower signal currents, i.e. lower concentrations with higher resolution. This already lead to the realization of individually addressable BDD micro- and nanoelectrodes, e.g. arranged in a 3 by 3 matrix with $2 \mu\text{m}$ pitch, for the spatial and time resolved detection of single cell activities [21, 22]. In these experiments, the resulting ion currents were in the range of 15 pA to 25 pA and were observed for a few milliseconds.

Obviously both elements, the lattice-matched InAlN/GaN HEMT and the BDD electrode, have successfully demonstrated their capabilities within their respective applications, however so far mainly as individual components. The challenge for the development of the sensor system, where these two elements are combined, is to engineer the lattice-matched InAlN/GaN HEMT in a way that it is compliant with specific requirements established by the BDD electrode, especially for the perspective of array integration possibly with high integration density, thus high spatial resolution, of individual addressable microelectrodes. Among others, one specific and important requirement is the need of a low overall FET leakage. Considering for example the above mentioned ion current of 15 pA means, in case of individual addressable electrodes, that the InAlN/GaN HEMT (as switch) must be able to block this low current. In case of ISFET measurements gate leakage can cause an unbalanced bias distribution, in turn causing a drop of the extrinsic transconductance, thereby limiting the achievable pH resolution. Additionally, leakage currents between separate devices of an integrated system may lead to noise and cross-talk [21, 23], thus limiting the spatial resolution. Similar thoughts also apply to high-temperature electronics. Here, an initially low leakage current is desired, since leakage may be further activated, when rising the ambient temperature. Excessive gate leakage, for instance, can limit the applicable input voltage drive, thus limiting the resulting output current swing. A residual drain-source leakage can prevent complete pinch-off. In consequence the resulting output voltage swing, hence the output power in RF applications is decreased. Both phenomena were already observed in previous high-temperature experiments [13, 24].

Thus, in order to accomplish good performances in high-temperature electronics and in electrochemical sensor applications, the elimination of parasitic leakage currents, here especially of the InAlN/GaN HEMT, is of high priority. However, device leakage in GaN-based HEMTs is still one of the main hurdles preventing optimum performance, especially under extreme operations [13, 25, 26, 27, 28]. The dominating leakage current in GaN-based devices seems gate leakage, which is commonly ascribed to tunneling across the Schottky gate [29, 30]. Thus, in a number of experiments it was tried to increase the tunneling barrier by e.g. the deposition of an additional gate oxide [31, 32, 33], or by other surface modification techniques like post processing annealing [34], oxygen plasma treatment [35, 36] and thermal oxidation [37, 38], where the Schottky diode is then

essentially replaced by a metal insulator semiconductor (MIS) diode. All these methods are capable to reduce the gate leakage currents by several orders of magnitude. Gate leakage currents in the lower nA/mm regime are typically reported. However, with an efficient reduction of gate leakage other leakage mechanisms, e.g. buffer leakage (drain to source) or, more general, off-state leakage, may become equally important. Buffer leakage is usually considered a matter of materials quality, which is why strategies to cope with buffer leakage usually focus on improvements in the heterostructure growth technology [39].

In this work, the limit of "acceptable" device leakage certainly is established by the 15 pA ion current, which is seen using individual BDD microelectrodes. Nevertheless, a residual off-current I_{off} of the lattice-matched InAlN/GaN HEMT, significantly lower than these 15 pA, would be needed to achieve a reliable detection of such a signal. Therefore, in this work a new InAlN/GaN HEMT technology on sapphire substrates was developed, which is capable to reduce the overall device leakage of a 50 μm wide HEMT to approximately 1 pA. This technology is inspired by the Silicon-on-Insulator (SOI) technology (essentially Si on sapphire) and employs a deep isolation process leaving small, confined mesa islands on the substrate, thin buffers (here as thin as 50 nm) heterostructures, and thermal oxidation of the InAlN barrier. Thus, in reference to SOI this technology may be referred to as GaN-on-Sapphire (GOS) technology leading to lattice-matched InAlN/GaN MISHEMTs. Although it seems already outdated as substrate material, especially for the fabrication of high power, high frequency GaN HEMTs, here sapphire presents one of the key features of this technology, which is linked to its high insulation properties. The capabilities of such lattice-matched InAlN/GaN MISHEMTs prepared in this way, were then tested at high ambient temperatures and in combination with BDD electrodes for electrochemical applications.

Thus, the outline of this thesis follows the route from the development of low leakage lattice-matched InAlN/GaN HEMTs to their applications in high-temperature electronics and in electrochemical applications, here as extended-gate ISFET or as switch for individual electrode pixels. The initial chapter ***Lattice-Matched InAlN/GaN HEMT Device Basics*** introduces the material system of the group-III nitrides and the basic operation principles of GaN-based HEMTs, however, clearly focusing on the lattice-matched InAlN/GaN material system, also giving an insight into three important contributions to the leakage currents of GaN HEMTs. Then, the chapter ***Low-Leakage Lattice-Matched InAlN/GaN HEMTs on Sapphire*** introduces the GOS technology, which was developed to eliminate the leakage current. The corresponding device characterization compares the GOS MISHEMT technology to a conventional GaN HEMT technology, here especially with respect to the leakage or subthreshold behavior. Afterwards, the chapter ***Thin Body InAlN/GaN MISHEMT: Device Operation up to 600 °C*** discusses the change of device characteristics at elevated temperatures. First long-term stability experiments by means of high-temperature storage and high-temperature large-signal class A measurements at radio frequency (RF) are presented for this new, thin material configuration. After the discussion of high-

temperature electronics, the focus of the thesis is moved to the field of electrochemical sensors. This starts in chapter 5 ***Diamond Electrodes for the Integration with InAlN/GaN HEMTs*** with the introduction of the BDD electrode as chemical sensor. All relevant parameters, which establish the specific electrochemical requirements for the InAlN/GaN HEMT in a combined measurement system are extracted in this chapter. This is linked to a discussion of the BDD/electrolyte phase boundary, which is used to explain the pH sensitivity. Since it is of particular interest for the design of ISFETs, an equivalent circuit model of this interface is derived mainly relying on electrochemical impedance spectroscopy. Additionally, microelectrode arrays (MEAs) are introduced as electrode structures for advanced amperometric measurements. The actual combination of BDD electrodes and InAlN/GaN MISHEMTs is then discussed in chapter 6 ***Combining InAlN/GaN HEMTs and BDD Electrodes for Electrochemical Sensing Applications***, where initially two different technologies to achieve the monolithic integration of diamond and GaN HEMTs are presented. During this work, a new "diamond first" integration technique was investigated, which could eliminate concerns about the compatibility of electronic materials with the harsh diamond growth conditions. Subsequently, the two different measurement configurations, i.e. the ISFET configuration for pH tracking and the switch configuration to switch on/off redox currents, are discussed with respect to the boundary conditions given through the BDD electrode. In other words, this means a deduction of certain design criteria for the FET to be compliant with the electrochemical requirements, hence stressing the importance of a low FET leakage characteristic. The chapter closes with the presentation of the achieved results in both measurement configurations. Finally, the chapter ***Closing Remarks*** provides a summary of the main ideas and results obtained during this work and presents an perspective for the development of a miniaturized electrochemical sensor system.

2 Lattice-Matched InAlN/GaN HEMT Device Basics

High-temperature electronics and the integration with diamond for the development of electrochemical sensor systems are two applications, which supplement the application range of InAlN/GaN electronic devices, which, so far, is mainly centered around high-power operation at high-frequencies. All these applications benefit from the excellent materials properties, where the key enabling parameter for the two applications being discussed in this work, namely high-temperature electronics beyond the limit of silicon devices (chapter 4) and the integration with diamond for electrochemistry (chapter 6), is the extremely high, ceramic-like thermal stability, especially of the lattice-matched InAlN/GaN heterostructure. Indeed, HEMT operation at temperatures up to 1000 °C [13] and the integration with diamond [18] (of high electrochemical grade ¹) had already been demonstrated using lattice-matched InAlN/GaN HEMTs. One parameter limiting the performance of GaN-based devices under high-temperature operation, but also in power applications, is parasitic leakage. Thus, a technological implementation to address leakage phenomena is welcome to further enhance the device performance in the different applications. A precise control of leakage currents, however, is of particular interest for high-temperature electronics, since leakage currents may be further activated with temperature. In case of electrochemical sensor systems, where in this work a diamond electrode is connected either to the gate or the drain of the transistor, leakage currents may cause an unbalanced bias distribution, thus limiting the sensor output range. Additionally, leakage currents present a hurdle for the realization of sensor systems with high integration density, especially with respect to biomedical applications, where measurements of single cells with high spatial resolution are targeted and signals in the range of 15 pA are expected [22].

The term leakage, however, is used for a rather wide spectrum of different phenomena depending on the application being discussed, thus also referring to different sources of leakage currents with a possibly predefined evaluation technique. In digital applications, for instance, leakage may refer to the dynamic losses when switching from high (low) to low (high) state, but also to the residual drain-source current due to a insuffi-

¹high electrochemical grade shall refer to a low amount of sp²-bonded carbon (graphitic phases) in the diamond lattice, which is only achieved at diamond growth temperatures above $T > 750$ °C (see chapter 5)

ciently depleted channel in the low state ($V_{GS} = 0$ V [40]). Under radio-frequency (RF) operation leakage may be linked to dis-/charging of (parasitic) capacitances or traps [41, 42, 43]. However, the two applications being presented later in this work are mainly discussed within the frame of DC-operation. Therefore, the discussion and investigation of leakage currents, that will be given in this chapter, shall also be limited to DC device characteristics.

Since the group-III nitride semiconductors are already well established materials, there do exist a number of textbooks explaining the origin of polarization or the device physics of heterostructure systems comprised of these materials [2, 10, 11]. Therefore, a detailed discussion of the complete set of group-III nitrides and their ternary alloys will be omitted. Instead, this part shall briefly summarize the properties of the InAlN/GaN heterostructure system, especially in its lattice-matched configuration, explain the formation of the two-dimensional electron gas (2DEG) at the heterointerface, and give an insight into the InAlN/GaN HEMT operation technology. Since they are of high relevance for this work, also a first description of parasitic conduction paths shall be provided.

2.1 Crystal Structure of Nitride Semiconductors

The group-III nitrides are polar materials and crystallize in the noncentrosymmetric hexagonal close-packed (hcp) wurtzite structure exhibiting both, piezoelectric polarization P_{pz} and spontaneous polarization P_{sp} . Figure 2.1(a) schematically shows the wurtzite structure for the example of a GaN crystal, but is generally valid for InN, AlN or the ternary alloys InAlN, AlGa_{1-x}N and InGa_{1-x}N by replacing the Ga-atoms with the corresponding metal atom of the binary or ternary alloy. The crystal is described by the lattice constant a_0 for the length of the basal hexagon and c_0 for the height of the hexagonal prism (the subscript 0 indicates relaxed conditions), where, like in this work, a_0 is generally perpendicular to and c_0 parallel to the growth direction. Among the ternary alloys the In_xAl_{1-x}N system is special, because it can be grown lattice-matched to GaN. Since growth is carried out along the c-axis, lattice-matched refers to the lattice constant a_0 . The change of this lattice constant with the alloy composition x is predicted by Vegard's law and is shown for the different ternary alloys Al_xGa_{1-x}N, In_xAl_{1-x}N, and In_xGa_{1-x}N in figure 2.1(b). At an In-content of approximately 17 % the InAlN alloy is grown lattice-matched to GaN. Thus, a heterostructure comprised of a lattice-matched InAlN barrier and a GaN buffer does not bear internal strain, which might be the reason for its extremely high thermal stability even allowing the HEMT operation at temperatures as high as 1000 °C [13, 14].

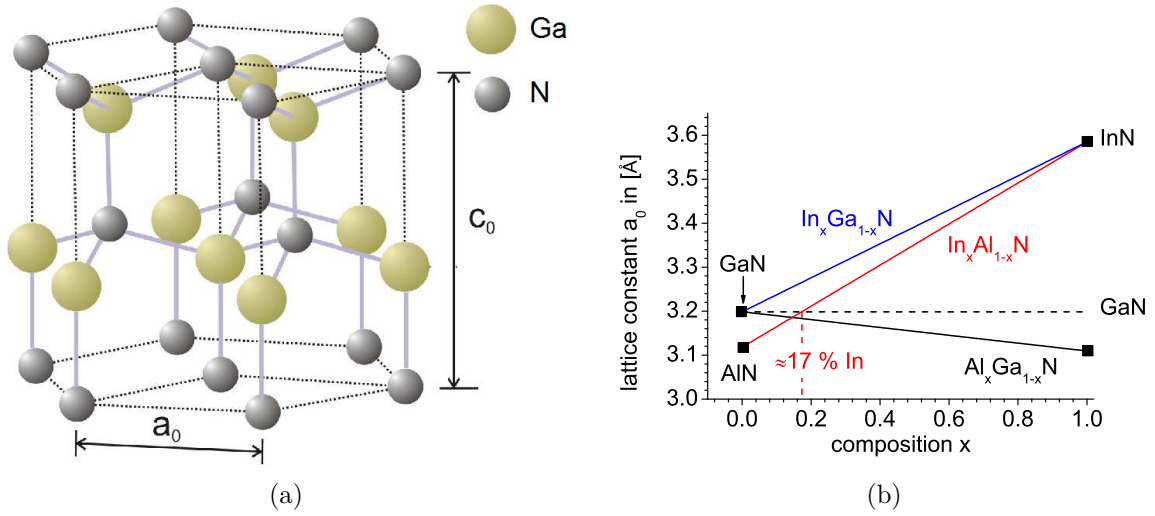


Figure 2.1: (a) Hexagonal structure of the GaN crystal. Figure redrawn after [44]. (b) Change of lattice constant a_0 with alloy composition x . The InAlN alloy can be grown lattice-matched to GaN when its In-content is approximately 17 %.

2.2 Formation of 2DEG in InAlN/GaN Heterostructures

In contrast to Si or GaAs devices, where the formation of a conductive channel relies on doping, the formation of the 2DEG at the heterointerface of two nitride materials relies on the discontinuity of the total polarization P_{tot} between the two materials, where P_{tot} is the sum of P_{sp} and P_{pz} . The formation of the 2DEG shall be illustrated with the help of figure 2.2, where InAlN is considered as the barrier and GaN as the buffer material. A gradient of the total polarization P_{tot} is associated with a fixed polarization charge density σ given by

$$\sigma = -\nabla P_{\text{tot}}. \quad (2.1)$$

The fixed polarization sheet charges cause an accumulation of mobile charges of the same magnitude, but of opposite sign labeled as polarization-induced sheet charges. Assuming an abrupt interface of an InAlN/GaN heterostructure, where the two nitrides possess a different total polarization, the bound polarization charge at the interface will partially compensate leaving a net fixed polarization interface density equal to

$$\sigma_{\text{int}} = P_{\text{tot,GaN}} - P_{\text{tot,InAlN}}. \quad (2.2)$$

A positive σ_{int} causes an accumulation of free mobile electrons (the 2DEG) at the heterointerface in the material with lower band gap (here, GaN). Thus, the sheet carrier concentration n_s of the 2DEG should be given by the difference of the total polarization between these two materials. However, as will be explained below, this presents a maximum n_s , which neglects the influence of the pinned surface potential (see below) resulting in a dependency on the InAlN barrier thickness.

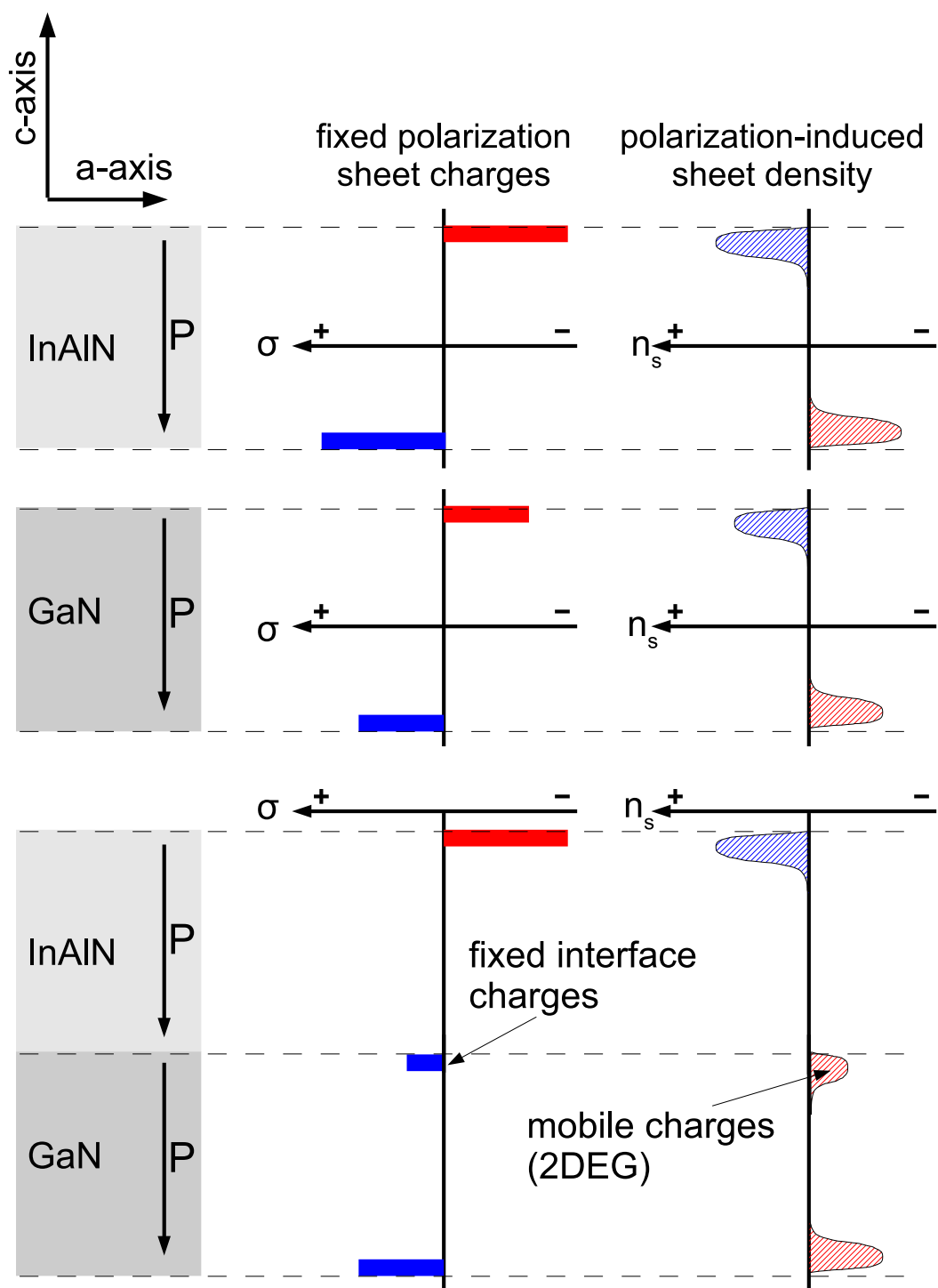


Figure 2.2: Illustration of polarization-induced charges at an InAlN/GaN heterointerface.

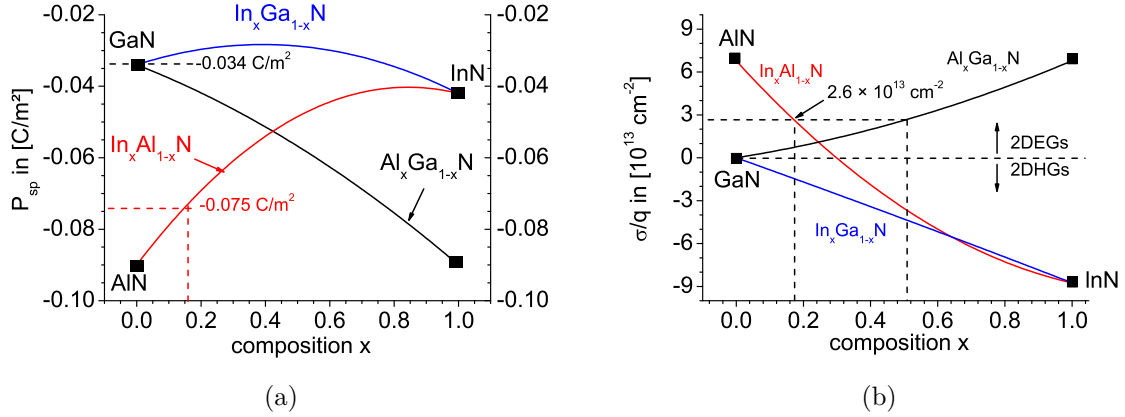


Figure 2.3: (a) Change of the spontaneous polarization P_{sp} dependent on the material composition of random ternary alloys. (b) Fixed interface carrier density σ_{int}/q . The interface density of the lattice-matched InAlN/GaN system is $\sigma/q = 2.6 \times 10^{13} \text{ cm}^{-2}$. Calculated after [9].

In case of the lattice-matched InAlN/GaN configuration, where no strain is present in the material system, the total polarization is equal to the spontaneous polarization ($P_{tot} = P_{sp}$). Thus, the fixed interface density σ_{int} solely arises from the difference in spontaneous polarization. Figure 2.3(a) shows the change of the spontaneous polarization of random ternary alloys with the alloy composition x . The corresponding calculations follow the routine described in [45]. The spontaneous polarization of GaN is $P_{sp} = -0.034 \text{ C/m}^2$ and that of lattice-matched $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is $P_{sp} = -0.075 \text{ C/m}^2$. According to equation (2.2) this results in a fixed interface density of $\sigma_{int} = 0.041 \text{ C/m}^2$. Thus, the maximum 2DEG carrier concentration, which could be obtained from a lattice-matched InAlN/GaN heterostructure, is as high as $n_s = 2.6 \times 10^{13} \text{ cm}^{-2}$. For comparisons figure 2.3(b) shows the maximum n_s , which could be obtained by any other GaN-based heterostructure also taking into account piezoelectric polarization (the corresponding calculations again follow [45]). In the more conventional AlGaIn/GaN material system a similar high carrier concentration can only be achieved for an Al-content of approximately 50 %, which then inherits a significant lattice mismatch, thus internal strain in the barrier.

As mentioned above, the bound interface density σ_{int} can be considered as an upper limit for the 2DEG carrier concentration, which can be obtained in a heterostructure neglecting the effect of the surface potential, thus the influence of the barrier layer thickness. In GaN heterostructures this surface potential Φ_{sp} (of the free surface) is given by a donor-like trap density (equal to σ_{int} , also referred to as surface states) on the barrier surface, which represents the induced counter charges of the electrons in the channel [46], causing a dependency of the 2DEG concentration on the barrier layer thickness. This effect shall be explained with the help of figure 2.4(a), which compares the schematic band diagrams of three InAlN/GaN heterostructures with different barrier

layer thicknesses. The circle indicates the energy level of the surface donors E_{SD} , where their states can be occupied (filled circle) or partially occupied (partially filled circle). The energy level of the surface donors is constant with respect to the conduction band E_C and here assumed as a single trap level. Considering initially the band diagram of the thin InAlN barrier (dashed blue) means that the level of the surface donors is located below the Fermi energy. Thus, their states are completely filled with electrons. Hence, the source of electrons (the surface donor) is not ionized meaning that no electrons accumulate in the 2DEG ($n_S = 0$). In this case the surface potential increases linearly with the barrier layer thickness and the electrical field across the barrier is equal to

$$F = \frac{q\sigma_{int}}{\varepsilon_{InAlN}}. \quad (2.3)$$

With increasing barrier layer thickness the energy level of the surface donor approaches the Fermi energy enabling electron transfer from the surface donor to unoccupied states (of lower energy) in the GaN 2DEG channel. This barrier thickness is the critical thickness t_{crit} (red band diagram in figure 2.4(a)). As the InAlN thickness increases further more electrons transfer from the donor to the channel until the surface state is empty (maximum n_S). As long as the surface donor is partially filled, the Fermi energy will remain at the donor level meaning that the surface potential is equal to the surface donor level ($\Phi_{SP} = E_{SD}$) and independent of the barrier thickness. Since the polarization is then partially screened by the accumulated electrons, the electrical field across the barrier decreases with increasing n_S (increasing t_{InAlN}) and is given by

$$F = \frac{q(\sigma_{int} - n_S)}{\varepsilon_{InAlN}}. \quad (2.4)$$

The 2DEG concentration n_S of the InAlN/GaN heterostructure is calculated by [9]

$$n_S = \frac{\sigma_{int}}{q} - \frac{\varepsilon_{InAlN}}{t_{InAlN} \cdot q} \left(\Phi_{SP} + \frac{E_F(n_S)}{q} - \frac{\Delta E_{C, InAlN/GaN}}{q} \right), \quad (2.5)$$

where $\varepsilon_{InAlN} = 12.3$ is the permittivity of the barrier (see appendix E), t_{InAlN} is the barrier layer thickness, $E_F(n_S)$ is the position of the Fermi-level with respect to the conduction band edge at the heterointerface, and $\Delta E_{C, InAlN/GaN} = 0.65$ eV (see appendix E) is the conduction band discontinuity between GaN and InAlN (compare figure 2.4).

The resulting 2DEG concentrations of lattice-matched InAlN/GaN heterostructures for different barrier layer thicknesses (determined by Hall measurements) are shown in figure 2.4(b). For barrier layer thicknesses larger than 10 nm the carrier concentration in the channel is equal to the bound interface density ($2.6 \times 10^{13} \text{ cm}^{-2}$). In case of thinner barriers the 2DEG is partially depleted due to the pinned surface potential and vanishes completely at the critical barrier layer thickness $t_{crit} = 2$ nm. The surface donor energy level of the lattice-matched InAlN/GaN heterostructure was identified by numerical fitting of experimental data (using Atlas Silvaco) to approximately $E_{SD} = 0.6 \text{ eV} \dots 0.8 \text{ eV}$ below the conduction band edge (assuming a single trap level [47, 48]).

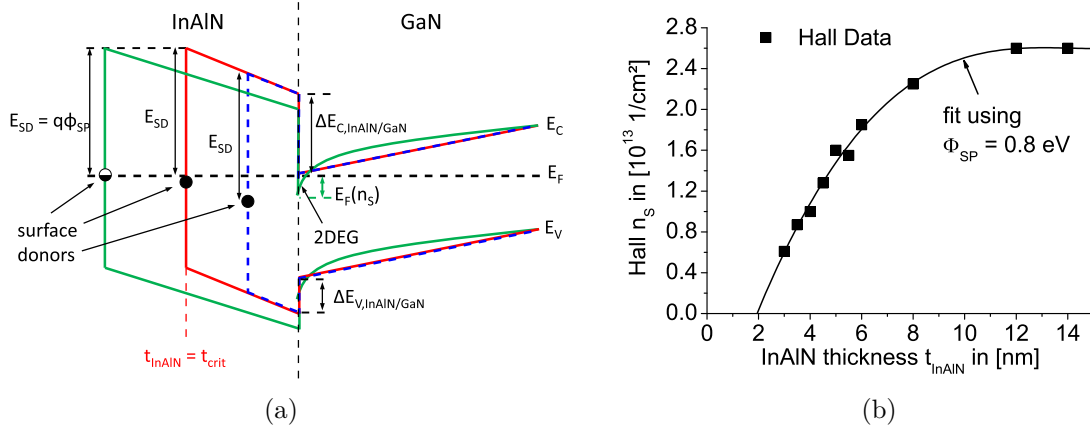


Figure 2.4: (a) Schematic representation of diagrams corresponding to three different InAlN barrier thicknesses. Green: $t_{\text{InAlN}} > t_{\text{crit}}$; red: $t_{\text{InAlN}} = t_{\text{crit}}$; dashed blue: $t_{\text{InAlN}} \leq t_{\text{crit}}$. (b) Change of the 2DEG carrier concentration of lattice-matched InAlN/GaN heterostructures with barrier layer thickness. Squares correspond values of n_s obtained through Hall measurements (in part from [47]). The black curve presents a fit based on equation (2.5) with $\Phi_{SP} = 0.8 \text{ eV}$.

It is worth mentioning again that the ionized surface donors correspond to positive surface charges, which consequently represent the surface counter charges to the electrons in the 2DEG. Thus, the 2DEG charge carriers can be depleted by discharging these positive surface counter charges. For instance, this phenomenon is observed in the virtual gate effect, where electrons are injected from the gate to the surface states of the neighboring free barrier partially compensating the counter charges, thus depleting the 2DEG [44]. This phenomenon is coped with by a proper surface passivation scheme, like e.g. SiN passivation on top of the barrier or thermal oxidation of the InAlN surface, which is capable of stabilizing the surface counter charge [37]. Moreover, an ideal surface passivation scheme can reduce the influence of the surface potential by moving the surface states from the InAlN surface to the surface of the passivation layer [49]. Hence, a carrier concentration as high as the bound interface density ($n_s \approx \sigma_{\text{int}}/q$) can be obtained even in combination with thin barrier layers provided that an efficient surface passivation is applied [17].

In GaN-based HEMTs the dependency of n_s on the barrier layer thickness can be used to achieve normally-off devices. Typically, the barrier layer is then recessed underneath the gate down to the critical thickness, thereby eliminating the 2DEG in the gate region [17]. However, of special interest for the electrochemical application proposed in this work are lattice-matched InAlN barrier layers with a thickness of approximately 5 nm to 6 nm, because the resulting threshold voltage should be in the range of $V_{\text{th}} = -2 \text{ V}$ (see chapter 6). In turn, the resulting n_s in that region is very sensitive to small variations of the barrier thickness. Using a linearized relation for that thickness range results in a variation of the carrier concentration of $\frac{\Delta n_s}{\Delta t_{\text{InAlN}}} \approx \frac{0.4 \text{ cm}^{-2}}{\text{nm}}$.

2.3 Principles of InAlN/GaN HEMT Operation

In an InAlN/GaN HEMT the current modulation is based on the modulation of the carrier concentration n_s in the 2DEG channel and therefore is closely related to the discussion above. Here, the modulation of charges is done by varying the potential of the gate contact. Depicted in figure 2.5(a) is a typical cross section of an InAlN/GaN HEMT. The current path in such a HEMT device is from source through the 2DEG channel to the drain terminal. Source and drain present ohmic contacts to the 2DEG. The gate contact in between is a rectifying contact used to accumulate or deplete electrons of the 2DEG underneath the gate metal, thereby modulating the conductivity of the channel. A striking difference between the above discussed heterostructures and the presented device structure is the insertion of the AlN spacer between the InAlN barrier and the GaN buffer. The AlN spacer leads to a reduced roughness at the heterointerface and prevents a deep penetration of the electron wave function into the InAlN barrier layer. This leads to a reduction of alloy scattering, thus to an enhanced electron mobility in the channel [50]. It was shown through experiments and calculations that a 1 nm thin AlN layer is sufficient to efficiently suppress the penetration of the electron wave function into the barrier, while its influence on the bound interface density remains negligible [50]. Therefore, all calculations concerning the exact device structure (as depicted in figure 2.5(a)) can be carried out using the simplified model of the InAlN/GaN heterostructure.

The effect of carrier modulation by different gate potentials is illustrated in figure 2.5(b), which shows the corresponding band diagrams in case of three different gate potentials. For the sake of simplification only the conduction band is depicted, which is sufficient for n-channel InAlN/GaN devices. At the gate contact the surface potential Φ_{SP} is then replaced by the Schottky barrier height Φ_{SB} . Due to Fermi level pinning Φ_{SB} is independent of the chosen gate metal [51, 52]. Initially, the black band diagram under equilibrium ($V_{GS} = 0$ V) shall be considered. The fact that at 0 V gate bias the 2DEG channel is (partially) occupied implicitly states that the corresponding InAlN barrier thickness is larger than the critical barrier thickness (in reference to Φ_{SB}). Negative gate voltages will start depleting the 2DEG, which is completely depleted if the threshold voltage $V_{GS} = V_{th}$ is applied (red band diagram). In that case the electrical field across the barrier is again equal to the polarization field given by equation (2.3). Through a positive gate voltage more electrons can accumulate in the 2DEG channel until the maximum n_s is reached at $V_{GS} = V_{max}$, where the polarization field is completely screened (flat band in the barrier, blue band diagram).

With the help of charge balance equations and the band diagrams of figure 2.5(b), the two voltages V_{th} and V_{max} can be calculated provided that the corresponding material parameters are known (here, $\Delta E_{C,InAlN/GaN}$, Φ_{SB} , ϵ_{InAlN} , $E_F(n_s)$, and σ_{int}). The charge balance equation is written as

$$qV_{GS} + q\Phi_{SB} = F \times t_{InAlN} + \Delta E_{C,InAlN/GaN} + E_F(n_s). \quad (2.6)$$

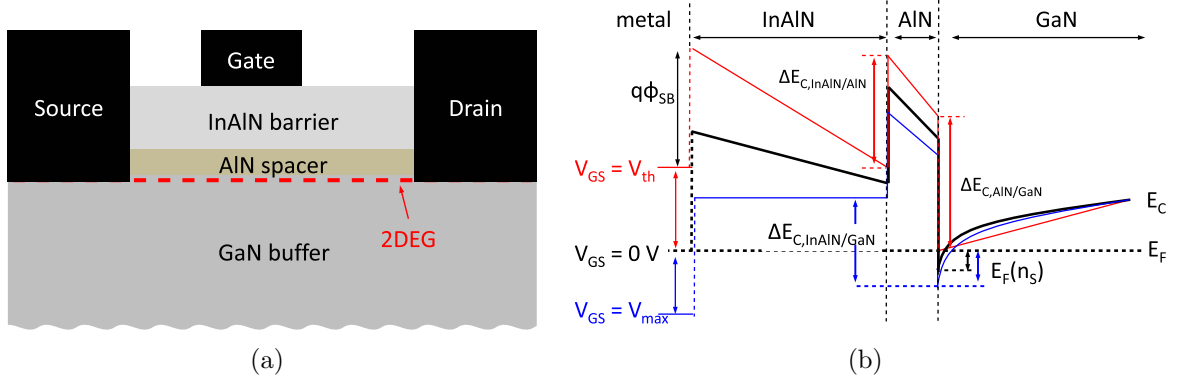


Figure 2.5: (a) Schematic cross section of an InAlN/GaN HEMT with the AlN spacer between the InAlN barrier and the GaN buffer layer. The 2DEG forms at the AlN/GaN interface inside the GaN. (b) Sketch of a corresponding band diagrams of the HEMT of (a) at three different gate potentials.

To calculate V_{th} equation (2.3) is used for the polarization field F and $E_F(n_S)$ is set to 0. The threshold voltage is then given by

$$V_{th} = \frac{\sigma_{int}}{q\epsilon_{InAlN}} \times t_{InAlN} + \frac{\Delta E_{C,InAlN/GaN}}{q} - \Phi_{SB}. \quad (2.7)$$

This means, that the threshold voltage of an InAlN/GaN HEMT is determined by the Schottky barrier height and depends linearly on the barrier layer thickness. Different behavior is observed for the calculation of V_{max} , which corresponds to flat band in the barrier. Thus, V_{max} is the voltage needed to compensate for the remaining polarization field expressed by equation (2.4). Hence, the gate voltage, where the maximum n_S is obtained is calculated to

$$V_{max} = \Phi_{SB} - \Delta E_{C,InAlN/GaN} - E_F(n_S) \quad (2.8)$$

In that case the penetration of the conduction band below the Fermi level $E_F(n_S)$ is constant meaning that also V_{max} is constant and independent of the barrier layer thickness. The flat band potential V_{max} was determined to slightly below 2 V for different gate contact metals [52].

2.4 Leakage Currents in InAlN/GaN HEMTs

As mentioned earlier, leakage currents are one parasitic effect limiting the performance of GaN-based HEMTs. One source of leakage in an InAlN/GaN HEMT is gate leakage, which can be observed under forward and reverse gate bias conditions. In general, there may be several mechanisms like e.g. thermionic emission, thermionic field emission or

(trap-assisted or defect-related) tunneling, contributing to the overall gate leakage current of a GaN HEMT [29, 30, 41, 42], where the dominating mechanism seems tunneling from the gate metal through the barrier. Nevertheless, surface or interface leakage currents cannot be neglected [53]. Figure 2.6(a) illustrates different gate leakage paths, one vertical component across the InAlN barrier to and then through the 2DEG channel and lateral components on the InAlN surface or through the InAlN barrier. Figure 2.6(b) shows a typical current-voltage characteristics of such a gate diode. Three regions can be identified in this graph, whose boundaries are given by the two voltages V_{th} and V_{max} , thus can be linked to the state of the electrical field in the barrier. Region II corresponds to the normal HEMT operation regime meaning that the 2DEG carrier concentration is modulated by the gate potential. The gate leakage current in this regime is low, because the InAlN barrier presents a rather efficient tunneling barrier and the leakage current is often ascribed to trap-assisted tunneling [29, 30]. Increasing the gate potential beyond the flat band potential V_{max} causes, as expected, a rapid increase of gate leakage, which is then dominated by thermionic emission or Fowler-Nordheim tunneling [29]. In reference to figure 2.6(a) the dominating leakage path of region II and III is vertical tunneling across the InAlN barrier to the 2DEG. However, region I corresponds to the subthreshold regime, where the channel underneath the gate is depleted. Thus, there are no free states in the channel, which could be occupied. In this case the lateral field component becomes dominating causing lateral conduction through the InAlN barrier or on its surface, which could be explained by variable range hopping along a network of surface states or defects [53]. However, it may also be noted that surface leakage can, generally, be observed on any surface of an insulator and often reflects the ability to adsorb (water) molecules from the ambient. Since the dominating leakage mechanism is tunneling, strategies to reduce or eliminate gate leakage usually focus on increasing the tunneling barrier, e.g. through the deposition of a gate dielectric or surface oxidation (thermally or plasma-based) leading to a Metal-Insulator-Semiconductor HEMT (MISHEMT) device technology [31, 32, 33, 35, 38].

Another important leakage current is the drain-source leakage current, which can be associated to any conductive path in parallel to the 2DEG channel (see figure 2.7(a)). Usually, such conductive paths are located in the GaN buffer, which is why this current is also referred to as buffer leakage, and are commonly ascribed to the materials quality i.e. to impurities or defects in the buffer volume [27, 29, 43]. Under open-channel conditions ($V_{GS} > V_{th}$) this leakage current is screened by the much larger output current. Thus, buffer leakage is mainly observed, if the device is biased into the pinch-off regime ($V_{GS} \leq V_{off}$). The residual drain-source current in the pinch-off regime is the off-state current I_{off} and is commonly extracted from the semilogarithmic transfer characteristics. This shall be further illustrated by figure 2.7(b), which compares two transfer characteristics with different I_{off} to a typical gate leakage characteristic. In one case I_{off} is nearly identical to the gate leakage. Consequently, it may be concluded that the buffer leakage is lower or of the same magnitude. Thus, the off-current is rather dominated by gate leakage than by buffer leakage. On the other hand, if I_{off} is larger than I_{GS} the off-current can clearly be ascribed to drain-source leakage.

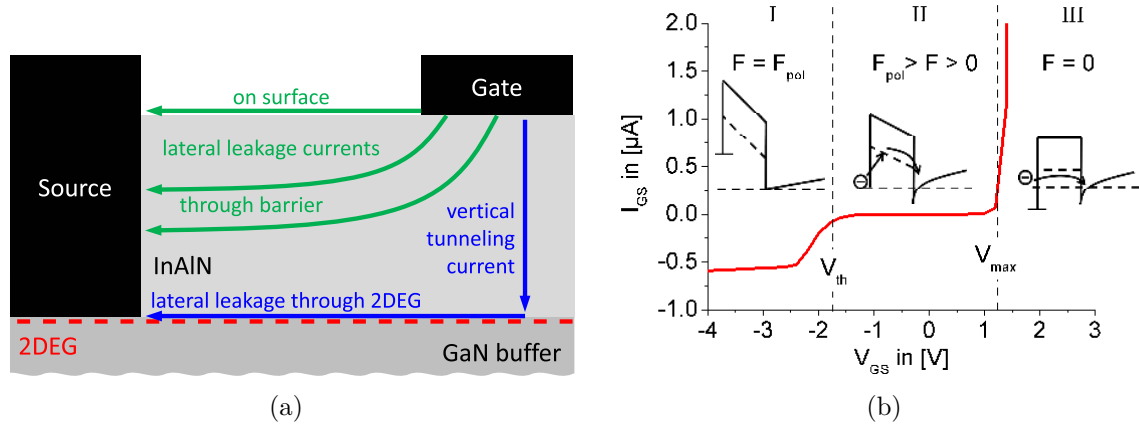


Figure 2.6: (a) Sketch of gate diode with possible vertical tunneling leakage and lateral leakage paths through the barrier or on the surface. (b) Typical current voltage characteristics of a gate diode with sketches of band diagrams at the gate corresponding to different gate potentials.

As mentioned, buffer leakage is usually ascribed to defects and impurities (unintentional doping) in the GaN lattice. Thus, materials growers have investigated strategies to improve the materials quality. One such strategy was the insertion of a low-temperature nucleation layer between the substrate and the GaN buffer, which accommodates the mismatch between GaN and substrate leading to a remarkably improved material quality [54]. In case of sapphire substrates this nucleation layer usually is an AlN layer. Another possibility to improve the materials quality, which relies on the fact that materials quality improves with growth thickness, is defect outgrowth. Thus, commonly rather thick GaN buffer layers ($t_{GaN} \geq 1 \mu m$) are grown on top of the nucleation layer resulting in low a defect density close to the 2DEG channel and the barrier surface [39]. However, this technique is mainly employed to enhance the electron mobility in the channel, which then rises due to reduced defect scattering. On the other hand, impurities like carbon, oxygen or hydrogen can be incorporated during growth and may act as shallow dopants leading to a residual conductivity of the buffer [55, 56]. Therefore, compensation-doped buffer layers were introduced enhancing the buffer isolation properties. The choice of the compensation dopant species depends on the resulting type of conductivity (n- or p-type) without compensation. Often, a residual n-type conductivity is reported. Thus, suitable compensation dopants are Fe or Mg [57, 58].

A further improvement of the heterostructure design is possible by implementing a double heterostructure system as illustrated in figure 2.8(a). In such a case one speaks of an InAlN/GaN/AlN double heterostructure, where the GaN (now called channel layer) is sandwiched in between the InAlN barrier and the AlN layer (now called buffer, not including the low-temperature nucleation layer). It is worth mentioning that buffer materials other than AlN and even buffer systems comprising different materials may be chosen as well, which may be useful to avoid strain in the GaN channel layer. Such

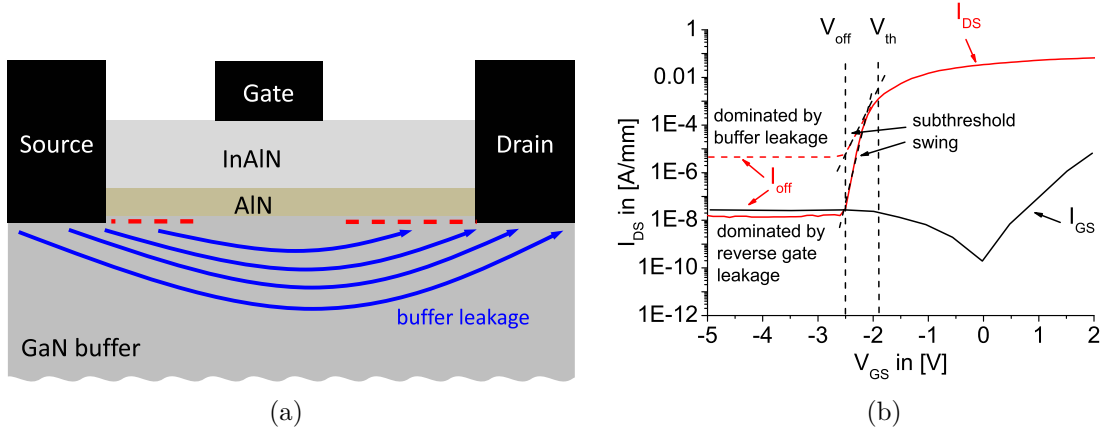


Figure 2.7: (a) Cross section of an InAlN/GaN HEMT illustrating leakage through the buffer volume. (b) Semilogarithmic transfer characteristics (red lines) compared to gate leakage current (black line). Red dashed line: I_{off} dominated by buffer leakage; solid red line: I_{off} dominated by gate leakage.

double heterostructure FETs (DHFETs) comprise a rather thick buffer and a relatively thin (less than 150 nm; typical: 20 nm to 50 nm) channel [59, 60, 61, 62]. These device structures benefit from stronger carrier confinement in the channel, where the confinement increases with decreasing channel thickness (compare figure 2.8(b)), and are less susceptible to leakage, but may inherit a parasitic two-dimensional hole gas (2DHG) at the GaN/AlN back barrier. However, more aggressive scaling of the channel layer thickness will eventually lead to carrier depletion in the channel (compensation by back barrier), which could be an alternative way to achieve normally-off operation [60]. As depicted in figure 2.8(b) a strong carrier confinement pushes the electron wave closer to the InAlN/GaN heterointerface, thus increasing the quantum capacitance, i.e. the capacitance given by the distance between the heterointerface and the peak of the electron wave. This also reflects in a significantly improved (steeper) subthreshold swing SS (sometimes also referred to as subthreshold slope) in the subthreshold regime and is a measure how sharp an electronic device can be biased from on to off state (for the depiction of SS see again the transfer characteristics of 2.7(b)). The quantity SS is calculated by [63]

$$SS = \frac{k_b T}{q} \cdot \ln(10) \cdot \left(1 + \frac{C_{depl}}{C_{GS}}\right), \quad (2.9)$$

where $k_b = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T the absolute temperature in K, and q the elementary charge. The quantities C_{depl} and C_{GS} present the depletion layer capacitance and the gate capacitance, respectively. The gate capacitance itself is presented by the series connection of the capacitance of the barrier layer and the quantum capacitance. Hence follows a steeper SS for stronger carrier confinement. At room temperature the lower limit of SS corresponds to approximately 59 mV/dec. Empirically, a steep SS can be associated with low buffer leakage currents [36, 64, 65, 66, 67]. An explanation for the reduction of the drain-source leakage in DHFET structures may be

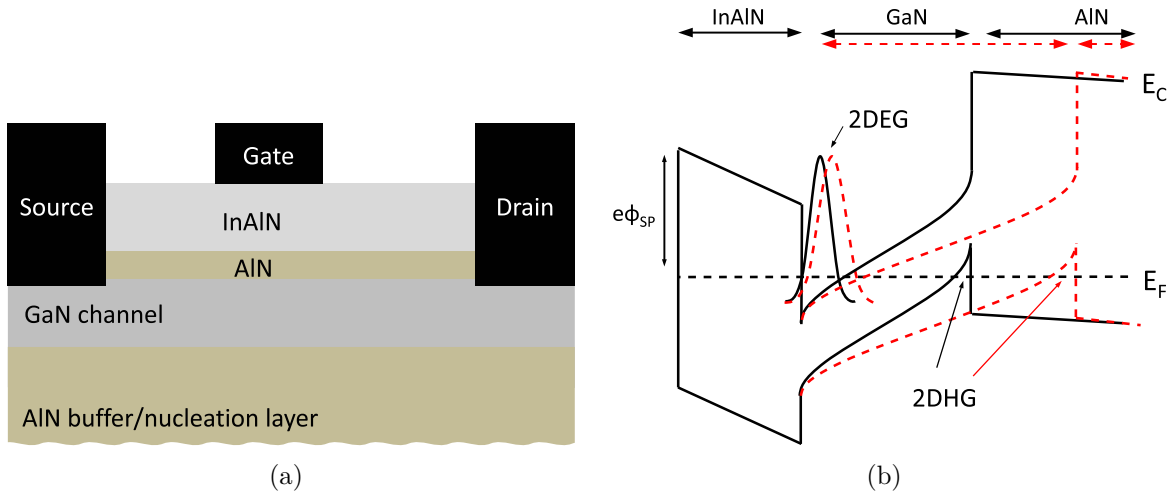


Figure 2.8: (a) Schematic cross-section of a InAlN/GaN/AlN DHFET. (b) Schematic band diagram of two DHFETs with different GaN channel thickness. The carrier confinement in the channel increases, when the GaN channel thickness decreases.

given by following Ohm's law, which relates the shape of a volume to its resistivity. However, this statement neglects the relatively thick buffer layers onto which the GaN channel is grown.

The last part of the leakage current, which shall be considered in this work is leakage current that occurs outside the active device area, but may also have influence on the device performance. As illustrated in figure 2.9 such leakage currents are mainly thought to occur between the contact pads. Thus, those leakage currents can be observed as part of the drain-source or gate-source current, even though an exact distinction between pad leakage and the above discussed leakage mechanisms is difficult in a single HEMT device. Also of interest, especially in an integrated system, is the consideration of the isolation between two different HEMT devices, since inter-device leakage can distort the signal of neighboring devices and may lead to cross-talk [23, 21]. Both, pad and inter-device leakage, are strongly dependent on the isolation properties of the material, onto which the contact pads are positioned and similar to the above discussed leakage mechanisms, these leakage currents may occur through the volume or on the surface. Thus, the positioning of contact pads onto a highly resistive material is preferred to suppress such leakage currents.

In this work, all these above discussed leakage currents are addressed by means of technological implementations resulting in an InAlN/GaN HEMT technology with low overall device leakage. In the following, the corresponding HEMT fabrication technology is introduced also pointing out the differences to the standard GaN technology (standard at the Institute of Electron Device and Circuits EBS, Ulm University and as described for example in [47, 14]).

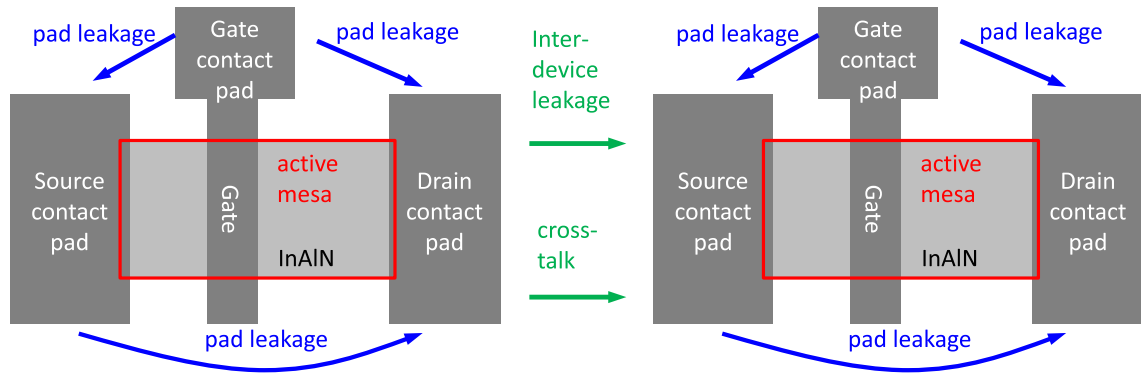


Figure 2.9: Top view of a HEMT illustration leakage paths outside the active device area, mainly between the contact pads. Also of interest is the isolation between two different HEMT devices.

3 Low-Leakage Lattice-Matched InAlN/GaN HEMTs on Sapphire

The physical basis of InAlN/GaN HEMTs was established in the previous chapter. This chapter shall now describe the way chosen (by means of technological implementations) to reduce or eliminate parasitic conduction paths, thus reducing the overall leakage of lattice-matched InAlN/GaN HEMTs. As will be shown, one key to reduce leakage is to exploit the high insulating properties of the sapphire substrate by introducing a deep mesa etch process. The implementation of this deep mesa process was facilitated by the development of ultrathin InAlN/GaN heterostructures on sapphire, in combination leading to a new GaN-on-Sapphire (GOS) technology (in reference to Silicon-on-Insulator SOI technology). The last part of this chapter shall then show the effects of the new GOS technology in comparison to a conventional GaN technology (compare technology reported in [14, 47]).

Before going into details it is worth mentioning that all InAlN/GaN heterostructures used in this work were grown by metal-organic vapor-phase epitaxy (MOVPE) and were provided by Prof. N. Grandjeans group, especially to mention L. Lugani and J.-F. Carlin, from the Laboratory of Advanced Semiconductors for Photonics and Electronics (LASPE) at the Ecole Polytechnique Federale De Lausanne (EPFL) in Switzerland. Thus, a large portion of the success of this work is owed to these people, who continuously refined their material growth technology, were always open to discussions, and were willing to pursue new ways to achieve common goals.

3.1 Sapphire as Substrate Material

One drawback of GaN technology is the lack of a large area GaN substrate. Luckily, GaN growth onto different foreign substrates has matured and one may chose the proper substrate material, depending on the targeted application and the material properties. The three most commonly used substrates for GaN heteroepitaxy are sapphire, silicon carbide (6H-SiC), and (111) silicon. Some criteria, which may be considered for the choice of the substrate material, are mentioned in table 3.1. Si substrates are attractive because of their low prize combined with the large available size, but also involve the

| | Si (111) | 6H-SiC | Sapphire |
|-----------------------------------|-----------------|-----------------|------------|
| available size | 12" | 6" | 6" |
| band gap [eV] | 1.1 | 2.9 | ≥ 8 |
| insulation | semi-conducting | semi-insulating | insulating |
| thermal conductivity [W/(cm · K)] | 1.3 | 4.9 | 0.42 |
| breakdown field [MV/cm] | 0.3 | 3 | 4 - 5 |
| lattice mismatch [%] | -16.9 | 3.3 | 16.1 |
| thermal mismatch [%] | 60 | 25 | -34.4 |

Table 3.1: Material properties of standard substrates for GaN heteroepitaxy at room temperature [1, 2, 3, 68, 69].

largest mismatch to GaN leading to a rather complex epitaxial structure to accommodate this mismatch. The best suited substrate for GaN growth, in terms of lattice mismatch, is SiC also offering a large thermal conductivity, which might be beneficial for high-power applications. However, its high prize may limit its application to research or niche products. A good compromise between cost and lattice mismatch is given by sapphire as substrate material. Moreover, as the only real insulator with a high transparency even in the deep ultra-violet (DUV) range, sapphire may even be considered as the ideal substrate for the development of low-leakage InAlN/GaN HEMTs for high-temperature electronics or electro-/biochemical applications. At temperatures as high as 500 °C its volume resistivity is approximately $10^{10} \Omega\text{cm}$ [68]. Simultaneously, its rather low thermal conductivity (self-heating) may play a minor role at such high temperatures, but may be advantageous in biochemical applications, where heat transport from the read-out circuitry to an investigated cell must be avoided. With respect to the targeted applications, these rationales clearly suggest sapphire as the substrate material.

3.2 GaN-On-Sapphire HEMT Technology

As will be described below, the implemented fabrication process to reduce the previously discussed leakage currents leads to a technology similar to the Silicon-on-Insulator (SOI) technology. With sapphire being the substrate material in this work, this new developed technology shall therefore, from here on, be referred to as GaN-on-Sapphire (GOS) technology. Since the GOS fabrication scheme also involves the formation of a gate oxide (by oxidation), the fabricated FETs will be referred to as MISHEMTs. In the following, some general remarks on the GaN FET fabrication process will be provided, which will be followed by a brief summary of the GOS fabrication technology. Details about the fabrication process itself are provided in appendix A.

Generally, the FET fabrication process starts with mesa isolation and is followed by the Ohmic contact and gate deposition. Mesa isolation can be achieved either by ion implantation or dry etching. While mesa etching physically removes the heterostructure outside the active area, ion implantation is associated with the destruction of the heterostructure stoichiometry and therefore eliminates the two-dimensional electron gas. Ion implantation of e.g. H, He, O, or N ions [70, 71, 72, 73, 74], has demonstrated to be a powerful tool to achieve resistivities up to the $G\Omega$ and even the $T\Omega$ regime while, simultaneously, maintaining a planar device technology, which might be favorable to increase the wafer yield. Furthermore, due to the planar device technology the possibility of short circuiting the gate with the 2DEG from the mesa sidewall is omitted, which can lead to a significant reduction of the gate leakage. However, ion implantation does not necessarily lead to permanent inter device isolation. High-temperature post annealing at temperatures larger than 700°C may slowly lead to a recovery of the heterostructure stoichiometry and reduced isolation properties [72]. Therefore, ion implantation does not seem to be compatible with the fabrication of InAlN/GaN HEMTs operating at very high temperatures, which is one goal of this work, and mesa dry etching had been chosen.

Considering wafer yield it seems beneficial to etch away only the barrier layer, thereby eliminating the 2DEG and maintaining a nearly planar device technology. However, it has been shown that deep mesa isolation down to the sapphire substrate greatly enhances the inter-device isolation [75]. As a consequence, in this work the InAlN/GaN heterostructure including the AlN nucleation layer had been scaled down to a total layer thickness of 100 nm enabling both, easy deep mesa isolation to the sapphire substrate and maintaining a nearly planar device technology. As will be seen in the next section employing an ultrathin GaN/AlN buffer layer also reduces significantly the residual drain-source leakage current. Another modification of the conventional or standard GaN technology is the use of Au-free contact metalization schemes. Au-based metalizations were found to be less stable during operation at very high temperatures [24] and were found to be incompatible with the harsh diamond overgrowth process [48], which is also of interest for this work. Thus, previously a Au-free HEMT device metalization was developed by M. Alomari [48] and refined by D. Maier [24] (colleagues in the EBS), which serves as the basis for the GOS MISHEMT technology employed in this work. Nevertheless, usually associated with the use of the Au-free metalization scheme is an increased access resistance. The main differences between the HEMT and the GOS MISHEMT technology are summarized in table 3.2. It is worth mentioning again that in case of thin barrier layers the carrier concentration is a function of the barrier thickness. Only if a proper surface passivation scheme is applied, the full carrier concentration of $n_s \approx 2.6 \times 10^{13} \text{ cm}^{-2}$ can be achieved. However, the addition of a passivation layer on top of the barrier layer may also influence the leakage behavior of the device. Therefore, in this work additional device passivation was omitted. As a consequence reduced carrier concentrations in the range of $n_s \approx 1.5 \times 10^{13} \text{ cm}^{-2}$ (compare figure 2.4(b)) are obtained leading also to reduced output current densities.

| | HEMT | GOS MISHEMT |
|------------------|----------------------------------|--|
| Mesa isolation | shallow through InAlN barrier | deep through entire heterostructure |
| Ohmic contacts | Ti/Al/Ni/Au 15/100/40/45 nm | Ti/Al/Ni 15/100/40 nm |
| Contact alloying | 30 s at 800 °C | 30 s at 800 °C |
| Oxidation | none | 2 min at 800 °C |
| Gate metals | Ni/Au 40/160 nm | Cu/Pt 200/20 nm |
| Remetallization | Ti/Au 20/200 nm | Cu/Ti/Pt 200/10/20 nm |

Table 3.2: Comparison of the standard HEMT and the GOS MISHEMT fabrication scheme.

The heterostructures used in this work were grown by MOCVD on two-inch sapphire substrates and were provided by Prof. Grandjeans group at the EPFL. The layer structure comprised a 50 nm low-temperature AlN nucleation layer, a GaN buffer of varying thickness (1000 nm, 450 nm, 200 nm, 50 nm), an 1 nm AlN smoothing layer and a 5 nm lattice-matched InAlN barrier layer (compare figure 3.1(a)). The actual fabrication process was initiated by mesa dry etching using reactive ion etching (RIE) in an Ar/BCl₃/Cl₂ plasma. The resulting etch rate was approx. 35 nm/min with nearly vertical mesa sidewalls. Slanted mesa profiles (approx. 50° angle) as seen in figure 3.1(b) were obtained using the reflow technique. The heterostructure was etched down to the sapphire substrate, which also served as a natural etch stop layer, where slight over-etching resulted in a clean and smooth sapphire surface. However, strong over-etching might lead to a significant narrowing of the device geometry.

Ohmic contacts were adapted for high-temperature electronics and were Ti/Al/Ni (15/100/40 nm) without Au overlay, which, as mentioned, was found to be not suitable for high-temperature operation [24]. The metal stack was deposited by e-beam evaporation and afterwards alloyed by rapid thermal annealing (RTA) in nitrogen atmosphere for 30 seconds at 800 °C. Alloyed ohmic contacts on InAlN/GaN structures typically produce quite large specific contact resistances above $\rho_C > 0.5 \Omega\text{mm}$ (see later). Therefore, new methods were developed to reduce access resistances. One such method is to recess the barrier in the contact region [76]. However, this technique requires precise control of the recess etch process. A new, promising method to reduce contact resistances is the use of regrown ohmic contacts [77], i.e. to regrow (by MBE) the drain and source contact areas with a heavily n⁺ doped GaN film. Using this technique also self-aligned InAlN/GaN HEMTs can be obtained [15].

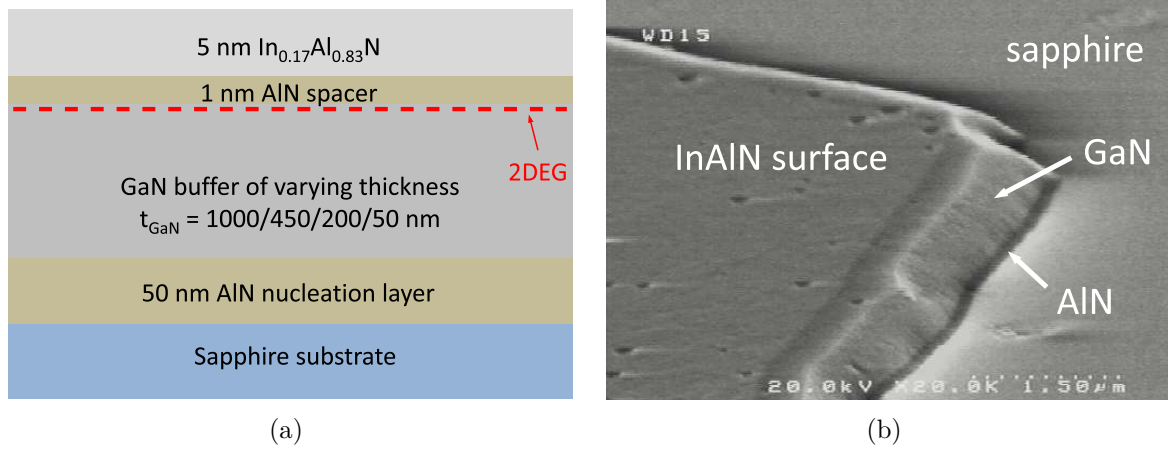


Figure 3.1: (a) Schematic presentation of the investigated lattice-matched InAlN/GaN heterostructure system. (b) SEM picture of mesa etched down to sapphire substrate with slanted profile. The different epi-layers (450 nm GaN buffer and 50 nm AlN nucleation layer) can clearly be distinguished. First published in [75].

The preparation of the gate contact was initiated by thermal oxidation of the InAlN surface, which drastically reduces gate leakage currents [37]. However, the process window of this thermal oxidation process is rather narrow in terms of oxidation time and temperature [38]. With short oxidations (less than 4 minutes) a crystalline native oxide forms on the InAlN surface, where the output current densities change according to the reduction of the InAlN barrier thickness [38]. Longer processes distort the crystalline order and cause an increased surface potential and consequently a severely reduced effective sheet charge density (compare figure 2.4). In this work, oxidation was done in pure oxygen atmosphere for 2 minutes at 800 °C in a tube oven forming an approximately 1.5 nm to 2.0 nm thin native oxide. In reference to the dielectric free passivation (DFP) formed by O_2 plasma pretreatment [78] the native oxide corresponds to a DFP formed by oxidation. After oxidation the Cu/Pt (200/20 nm) gates were patterned by e-beam lithography and deposited by e-beam and thermal evaporation. HEMT device processing was finalized by the deposition of an additional Cu/Ti/Pt (200/10/20 nm) metal stack onto the ohmic and gate contact pads allowing better device probing by needles. A schematic cross-section and an SEM picture of a fully fabricated InAlN/GaN GOS MISHEMT are presented in figure 3.2. In a fabricated device (figure 3.2(b)) the device mesa is confined to a relatively small area (active device geometry: gate-width $W_G = 50 \mu\text{m}$, drain-source distance $L_{\text{DS}} = 4 \mu\text{m}$; mesa geometry: $A \approx 40 \times 55 \mu\text{m}^2$). Thus, the major part of the much larger contact pads is positioned on the highly insulating sapphire substrate.

It was mentioned above, that for this work the heterostructure material stack (including barrier, buffer and nucleation layers) was scaled down to a total thickness of approximately 100 nm, mainly to facilitate the deep mesa isolation process. The next

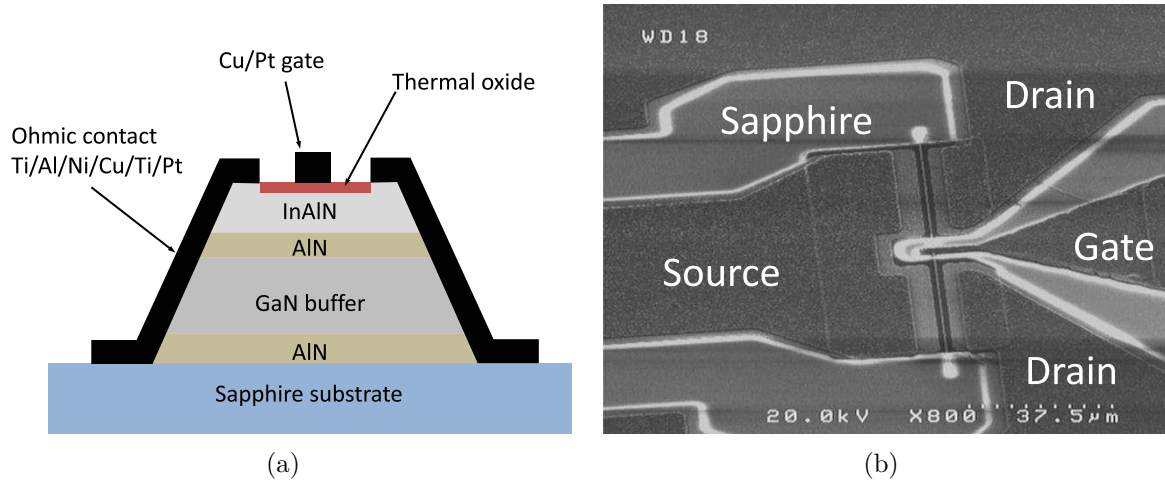


Figure 3.2: (a) Schematic cross-section of a final MISHEMT. (b) SEM graph of fully fabricated GOS MISHEMT ($W_G = 2 \times 50 \mu\text{m}$), where the major part of the contact pads is positioned on sapphire.

section shall discuss both, the influence of the technology and the effect of GaN buffer downscaling on the FET device characteristics.

3.3 Standard HEMT vs. GOS MISHEMT Device Characteristics

One key to facilitate the GOS MISHEMT device technology was the downscaling of the total heterostructure thickness, in this case to a thickness as thin as $0.1 \mu\text{m}$. Such thin heterostructures allow for an easy, deep isolation process and simultaneously maintain a nearly planar device technology. However, it was also mentioned before that, due to defect outgrowth, the materials quality increases with the materials thickness, which is the reason why GaN heterostructures grown onto foreign substrates are usually grown with buffer or nucleation layers thicker than $1 \mu\text{m}$. Thus, the choice to employ thin heterostructures for a simplified, reliable GOS technology may be accompanied by degraded transport properties of the 2DEG. Therefore, this section shall show both, the influence the applied technology (GOS vs. standard) and also the effect of a scaled GaN buffer on the device characteristics.

In order to evaluate the effect of GaN buffer layer scaling on the FET characteristics a set of four samples with different GaN thicknesses ($t_{\text{GaN}} = 1000 \text{ nm}$, $t_{\text{GaN}} = 450 \text{ nm}$, $t_{\text{GaN}} = 200 \text{ nm}$, $t_{\text{GaN}} = 50 \text{ nm}$) had been prepared on sapphire substrate and processed following the two above described routines. As mentioned previously, the four heterostructure systems have in common a 50 nm AlN nucleation layer, a 1 nm AlN

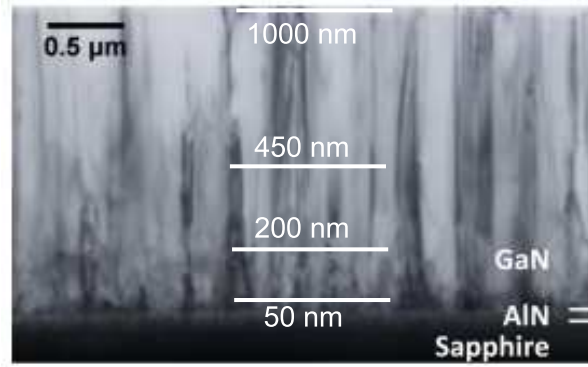


Figure 3.3: TEM cross-section of an InAlN/GaN heterostructure with $t_{\text{GaN}} = 2 \mu\text{m}$ grown on sapphire substrate. Picture taken from [79]. The four investigated GaN thicknesses are indicated by the white horizontal lines.

spacer, and a 5 nm lattice matched InAlN barrier and are grown by MOCVD on two inch sapphire substrates (see again 3.1(a)). In order to give an impression about the change of materials quality with the GaN buffer thickness, figure 3.3 shows a TEM cross-section of a lattice-matched InAlN/GaN heterostructure grown on sapphire with a $2 \mu\text{m}$ GaN buffer (picture taken from reference [79]). The crystalline quality (in terms of defect density) of the GaN layer can be estimated by the brightness. In close vicinity to the AlN nucleation layer the GaN buffer appears dark indicating a rather high defect density. With increasing thickness the GaN material appears brighter speaking for higher crystalline quality. For comparisons, the four in this work investigated layer thicknesses are indicated by white lines, which in turn would present the position of the 2DEG channel. Thus, an increased GaN buffer thickness may lead to a reduced lateral conductivity (through the barrier or on its surface; see again section 2.4) and an improved electron mobility μ_{el} due to reduced defect scattering. However, it was already suggested in 2005 [80] and confirmed recently [79] that the dominating limitation for high electron mobilities in InAlN/GaN heterostructures is the roughness at the barrier/buffer interface. As in this case, high, nearly state-of-the-art 2DEG mobilities can be achieved even for extremely thin InAlN/GaN heterostructure systems ($\mu_{\text{el}} = 1100 \text{ cm}^2/\text{Vs}$ for a 50 nm AlN nucleation and 50 nm GaN buffer layer [79]). It is worth mentioning that the samples discussed in the following and in reference [79] are identical. Therefore, details on the growth optimization process can also be found in this reference.

Prior to the FET processing the 2DEG carrier concentration n_s and mobility μ_{el} of the four heterostructure systems had been determined by Hall measurements. The thickness dependent Hall data are depicted in figure 3.4. Since the carrier concentration is a matter of polarization discontinuity and barrier layer thickness the resulting n_s is, as expected for a 5 nm lattice-matched InAlN barrier, $1.5 (\pm 0.1) \times 10^{13} \text{ cm}^{-2}$ and nearly constant with the buffer layer thickness. The small variations are probably caused by an inaccuracy of the InAlN barrier thickness together with the high sensitivity of n_s vs. t_{InAlN} for thin barriers (compare figure 2.4(b)). Another possible explanation in

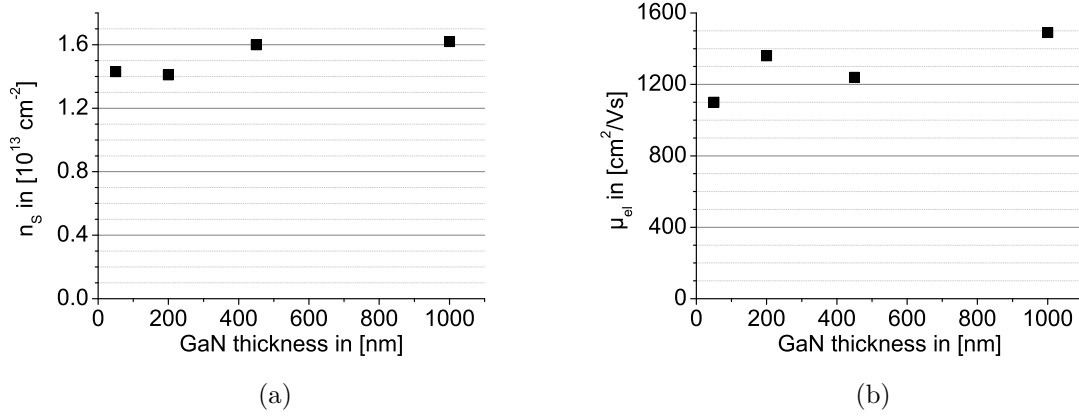


Figure 3.4: Hall n_s (a) and μ_{el} (b) vs. GaN buffer layer thickness. While n_s remains nearly constant μ_{el} degrades towards thin buffer layers.

case of the 50 nm GaN sample could be depletion caused by the charges at the GaN buffer/AlN nucleation layer heterointerface (compare figure 2.8 or [60]). In contrast, as a consequence of increasing surface roughness the mobility tends to degrade with reduced buffer thickness [79]. An electron mobility of $\mu_{el} = 1490 \text{ cm}^2/\text{Vs}$ is obtained for a 1000 nm thick GaN buffer. The mobility reduces to $\mu_{el} = 1240 \text{ cm}^2/\text{Vs}$, $\mu_{el} = 1360 \text{ cm}^2/\text{Vs}$, and $\mu_{el} = 1100 \text{ cm}^2/\text{Vs}$ for the 450 nm, the 200 nm, and the 50 nm GaN sample, respectively.

3.3.1 Ohmic Contacts and Inter Device Isolation

The trends of carrier concentration n_s and electron mobility μ_{el} are also reflected in the sheet resistance R_{sh} extracted by TLM measurements after complete device processing (see figure 3.5(a)). Due to the thermal oxidation, which transforms the upper 1 nm to 2 nm into a native oxide [38], the GOS MISHEMTs have lower n_s and consequently a larger sheet resistance (compare also figure 2.4(b)). In both cases the lowest sheet resistances are obtained for the 1000 nm GaN buffer sample with $R_{sh} = 611 \Omega$ and $R_{sh} = 259 \Omega$ for the HEMT and the MISHEMT, respectively. The sheet resistances of the other samples are (from thin to thick GaN layers): $R_{sh} = 710 \Omega$, 769Ω , and 723Ω for GOS technology and $R_{sh} = 396 \Omega$, 325Ω , and 314Ω for the conventional technology. However, in all cases (apart from the 50 nm GaN sample) the increase of the sheet resistance due to oxidation is more than 100 %, or, in other words, the reduction of the sheet conductivity σ_{sh} is around 50 % being in line with a reduction of the barrier layer thickness of approximately 1.5 nm. On the contrary, ohmic contacts in GaN-based HEMTs are expected to follow tunneling emission theory [81]. Therefore, the specific contact resistance ρ_C should mainly depend on the InAlN barrier layer thickness and the individual surface preparation. This is clearly confirmed by the samples processed

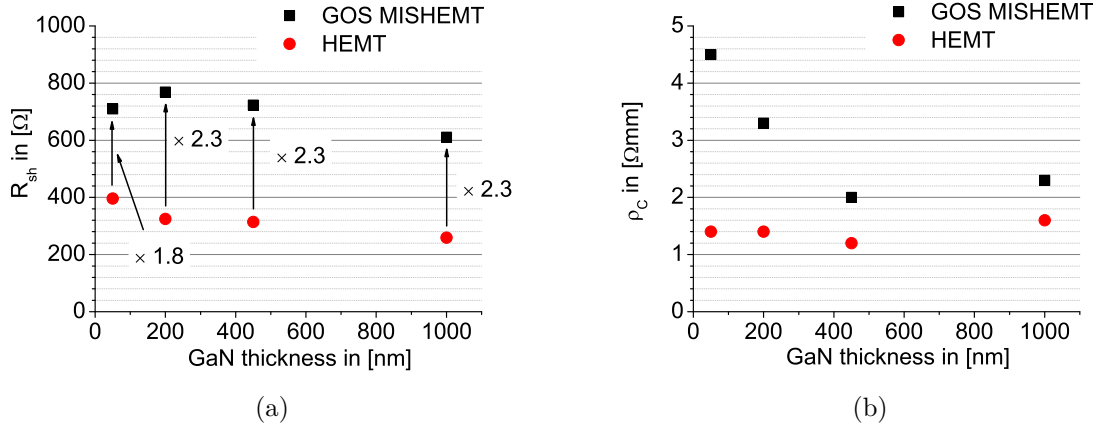


Figure 3.5: Comparison of (a) R_{sh} and (b) ρ_C vs. GaN buffer layer thickness of the two different technologies determined by TLM measurements.

according to the conventional HEMT technology (see figure 3.5(b)), where the specific contact resistance varies slightly around $\rho_C \approx 1.4 \Omega\text{mm}$. However, in the case of the Au-free GOS technology the contact resistance is $\rho_C \approx 2.1 \Omega\text{mm}$ for the two thick samples and is drastically increased to $\rho_C = 3.3 \Omega\text{mm}$ and even $\rho_C = 4.5 \Omega\text{mm}$ for the 200 nm and the 50 nm GaN buffer sample, respectively. As already mentioned, this increase is probably linked to the individual sample processing and, taking also into account results of conventional processing, cannot be linked to the GaN thickness.

The inter device isolation or the leakage between two contact pads of the same device was estimated by measurements using two ohmic contact pads positioned directly on the etched surface. This means that the contact pads are positioned either on the residual GaN buffer layer or, in the case of the GOS MISHEMT technology with deep mesa etching, directly on the sapphire substrate (see figure 3.6(a)). The two contact pads are 100 μm wide and separated by a 5 μm distance. The resulting leakage currents of the individual samples at an applied voltage of 10 V are summarized in figure 3.6(b). The corresponding IV characteristics exhibit a largely Ohmic behavior and are provided in appendix B. Sapphire is an extremely good insulator with a volume resistivity larger $10^{14} \Omega\cdot\text{cm}$ and is available with a high crystalline quality [68]. Thus, the leakage currents between two pads on sapphire can be expected to be surface currents, here in the range of 2 pA to 5 pA, which is already close to the measurement precision of the used setup. This means that due to the excellent isolation properties of sapphire both leakage currents (around the active device area and between two different devices) can be neglected using the GOS technology. The 50 nm and 200 nm GaN buffer samples also exhibit leakage currents in the lower pA regime when processed according to the standard technology, which is linked to an (in this case) unintentional deep mesa isolation. In contrast, the leakage currents of the 450 nm and 1000 nm samples are 1.6 nA and 6.2 nA, respectively, therefore increasing with increasing (residual) GaN buffer thickness. This suggests that leakage currents are linked to the residual cross-section of the GaN layers and leakage

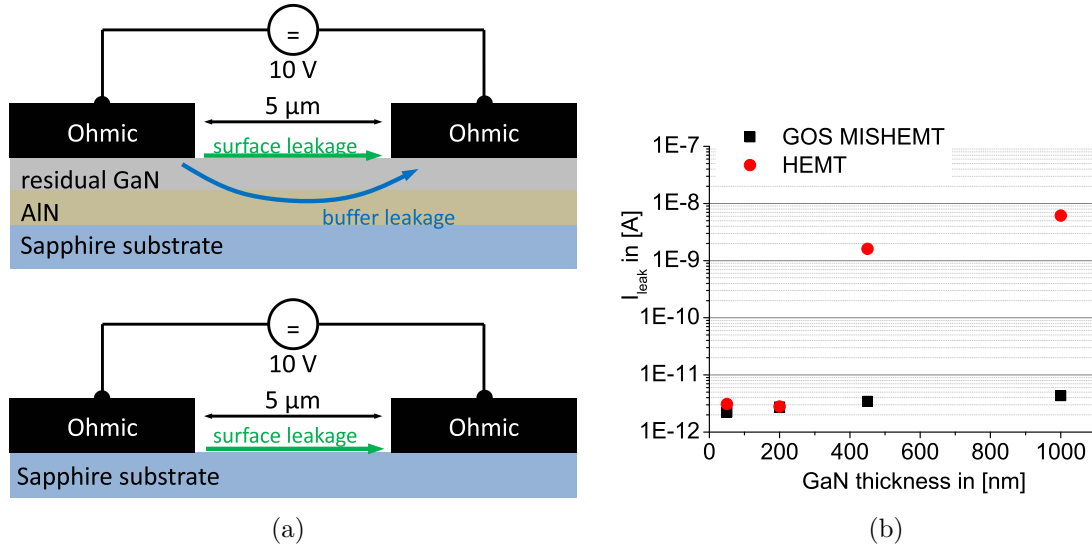


Figure 3.6: (a) Schematic representation of the test structures of the device isolation measurements. The Ohmic contact pads are positioned on the etched surface, which is the residual GaN buffer layer (top, standard HEMT) or the sapphire substrate (bottom, GOS MISHEMT). (b) corresponding leakage currents at 10 V for 100 μm wide contact pads. Black squares and red circles represent values of the MISHEMT and the HEMT, respectively.

is rather through the volume and not (only) on the free GaN surface. However, an exact evaluation of the leakage behavior with GaN layer thickness is difficult, because the existences of currents on the surface cannot be excluded. Another hurdle preventing a detailed analysis is the crystalline morphology, which, especially in the case of rather thin GaN buffers, strongly depends on the layer thickness [79] (see again figure 3.3). Therefore, the role of the back barrier, the defect network or impurities remain uncertain at this point.

3.3.2 On-State Characteristics

Figure 3.7 compares the FET output characteristics of HEMTs and MISHEMTs with the example of the 50 nm GaN buffer system. The complete set of output characteristics is provided in appendix B. The device dimensions for all characteristics presented in the following are (exceptions are labeled accordingly): gate-width $W_G = 50 \mu\text{m}$, gate-length $L_G = 0.25 \mu\text{m}$, source-to-drain distance $L_{SD} = 3 \mu\text{m}$, and source-to-gate distance $L_{SG} = 1 \mu\text{m}$. The gate-source voltage swing was from slightly above flat-band conditions in the barrier $V_{GS} = +2 \text{ V} > V_{\text{max}}$ to below pinch-off $V_{GS} = -2 \text{ V} < V_{\text{th}}$ in steps of $\Delta V_{GS} = -1 \text{ V}$. Although, the shape of both characteristics is comparable, the two major differences between the HEMT and the MISHEMT being observed are a significant reduction of the output current density and a shift of the threshold voltage V_{th} . Both

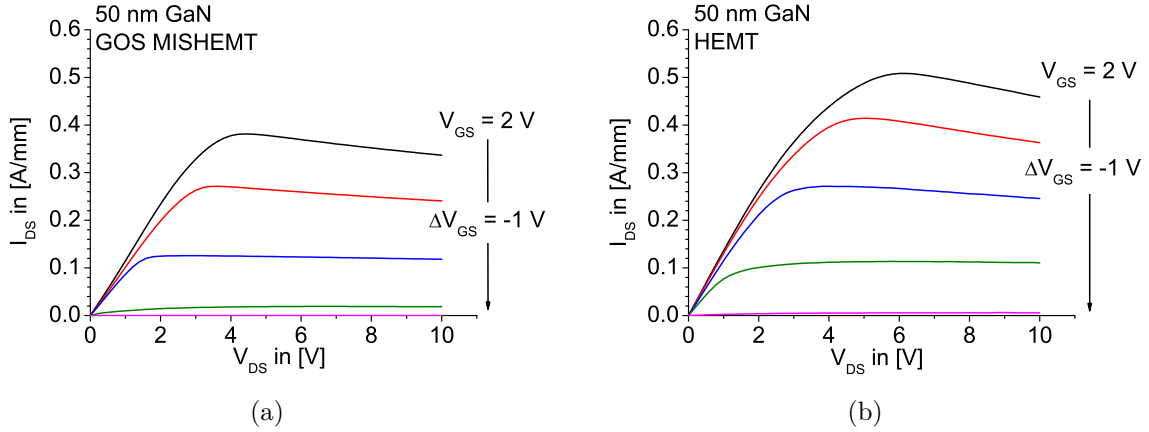


Figure 3.7: DC output characteristics of the 50 nm GaN buffer system for a GOS MISHEMT (a) and a standard HEMT (b). The device geometries are: $W_G = 50 \mu\text{m}$, $L_G = 0.25 \mu\text{m}$, $L_{SD} = 3 \mu\text{m}$, and $L_{SG} = 1 \mu\text{m}$.

observations are linked to the oxidation process leading to a reduction of the InAlN thickness, thus to a reduction of the undepleted 2DEG carrier concentration.

The peak current densities I_{\max} of all samples extracted at $V_{GS} = +2 \text{ V}$ are summarized in figure 3.8(a). Generally, oxidized samples exhibit a lower peak current density I_{\max} and a larger on-resistance R_{on} . For each set of samples the highest current density is obtained for the 1000 nm GaN sample with $I_{\max} = 0.93 \text{ A/mm}$ and $I_{\max} = 0.56 \text{ A/mm}$ for the HEMT and the MISHEMT, respectively. For both technologies, I_{\max} decreases with decreasing GaN layer thickness to $I_{\max} = 0.56 \text{ A/mm}$ and $I_{\max} = 0.38 \text{ A/mm}$ for the 50 nm samples. Apart from the 50 nm GaN sample the reduction of I_{\max} due to oxidation is in the range of approximately 40 % (30 % for the 50 nm sample) again being in good agreement with results of TLM measurements. Especially in case of the GOS technology I_{\max} follows rather the trend of n_s and not that of μ_{el} or R_{sh} , which strongly suggests that, independent of the GaN buffer thickness, the devices can exhibit saturation velocity dominated behavior. However, this cannot be confirmed for the standard technology, where I_{\max} decreases with increasing R_{sh} . Because this relation is not linear it is ascribed to other parasitic effects. A possible explanation for this might be that the applied gate voltage of $V_{GS} = +2 \text{ V}$ is slightly above the determined flat band voltage V_{max} allowing for a significant current conduction through the gate diode (compare figure 2.6). Depicted in figure 3.8(b) are the on-resistances R_{on} of the individual devices linearly extracted at $V_{GS} = +2 \text{ V}$ and $V_{DS} = 1 \text{ V}$. With the given device dimensions the main contribution to R_{on} should be given by the specific contact resistance ρ_C and not by the free source-gate region, thus the sheet resistance R_{sh} . Indeed, the on-resistances extracted for the HEMTs vary slightly around $R_{\text{on}} \approx 4 \Omega\text{mm}$, but is significantly higher for the 50 nm sample ($R_{\text{on}} = 7.0 \Omega\text{mm}$). Similar behavior, but with significantly larger values, is observed for the MISHEMTs, where the on resistances are $R_{\text{on}} = 7.3 \Omega\text{mm}$ for

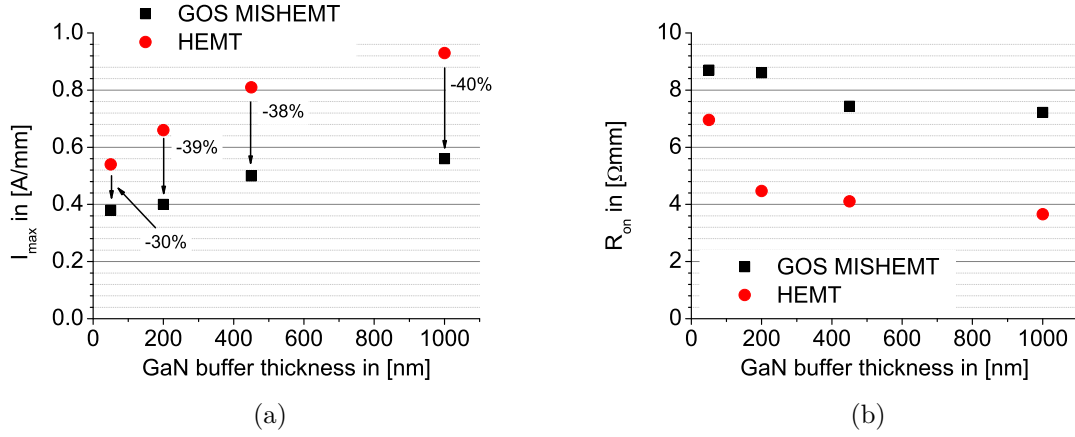


Figure 3.8: Peak current density I_{\max} (@ $V_{\text{GS}} = +2$ V) vs. GaN buffer thickness (a). On-resistance R_{on} (@ $V_{\text{GS}} = +2$ V, $V_{\text{DS}} = 1$ V) vs. GaN thickness (b). Black squares depict values of MISHEMTs and red circles those of HEMTs.

the two thick GaN buffer samples and $R_{\text{on}} \approx 8.4 \Omega\text{mm}$ for the two thin samples, again confirming the trend of TLM measurements.

The corresponding linear transfer characteristics were recorded in saturation at $V_{\text{DS}} = 6$ V being close to the V_{DS} , where the peak current density was obtained. The gate-source voltage swing was from $V_{\text{GS}} = -4$ V to $V_{\text{GS}} = +2$ V. Figure 3.9(a) shows the transfer characteristics of the GOS MISHEMTs and figure 3.9(b) those of standard HEMTs. The above mentioned trend of I_{\max} and the shift of the threshold voltages V_{th} are confirmed.

The threshold voltages V_{th} extracted through linear extrapolation are depicted in figure 3.10(a). Within one set of samples two different threshold voltages can be extracted. One for the two thick buffer samples and another for the two thin samples. For both sets the threshold voltage shift from thick to thin samples is $\Delta V_{\text{th}} = 0.5$ V, thereby confirming results from Hall measurements, where a lower 2DEG carrier concentration was determined for the two thin buffer samples. Comparing the two technologies, it is obvious that the threshold voltage is shifted towards more positive V_{th} . Due to the oxidation process, hence the reduced n_{S} , the threshold voltages are shifted by $\Delta V_{\text{th}} = 0.7$ V independent of the GaN buffer layer thickness.

Another important parameter which usually is extracted from transfer characteristics is the transconductance g_{m} and is shown for all samples in figure 3.10(b). Similar to the case of I_{\max} the highest g_{m} are obtained for the 1000 nm at $g_{\text{m}} = 237$ mS/mm (HEMT) and $g_{\text{m}} = 176$ mS/mm (MISHEMT) and the lowest for the 50 nm sample at $g_{\text{m}} = 154$ mS/mm (HEMT) and $g_{\text{m}} = 136$ mS/mm (MISHEMT). Since the distance between the 2DEG channel and gate metal does neither change due to oxidation nor due to the growth of different GaN buffers, the reduction of g_{m} must be related to the

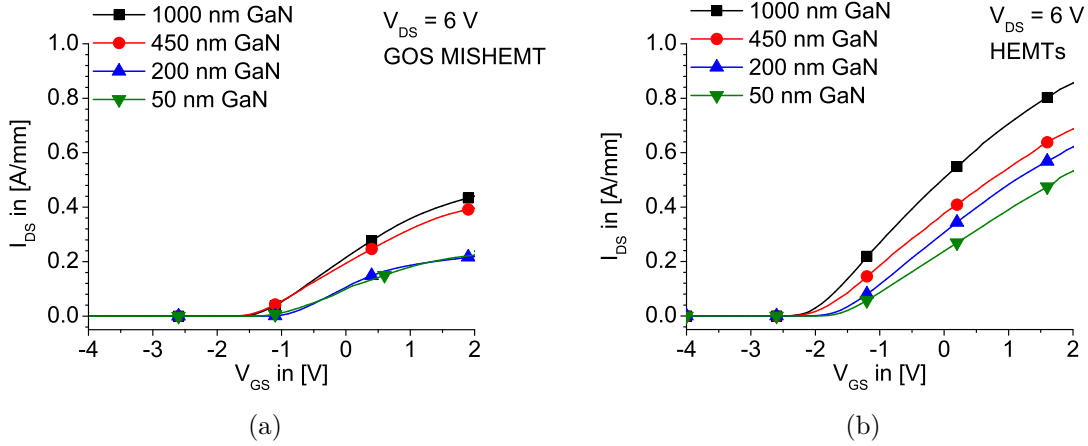


Figure 3.9: Corresponding linear transfer characteristics recorded at $V_{DS} = 6$ V of (a) the GOS MISHEMTs and (b) the standard HEMTs.

increased access resistances or to a reduction of 2DEG mobility. Indeed, an attempt to calculate the intrinsic transconductance $g_{m,i}$ after [63]

$$g_{m,i} = \frac{g_m}{(1 - g_m \cdot R_S)} , \quad (3.1)$$

where g_m is the measured extrinsic transconductance and $R_S = \frac{1}{3}R_{on}$ is the source resistance, leads to a deviation of the intrinsic transconductance $g_{m,i}$ of less than 10 % (from HEMT to MISHEMT). However, due to the constant barrier layer thickness of all samples a constant $g_{m,i}$ can be expected, which is only given for the three samples with thicker GaN buffer. Furthermore, a close look to the trend of $g_{m,i}$ reveals a similar behavior as the electron mobility extracted from Hall measurements. Since the maximum transconductances are extracted around gate-source voltages of $V_{GS} \approx -0.5$ V, the assumption that the maximum peak current density ($V_{GS} = +2$ V) is dominated by the saturation velocity may still be valid.

3.3.3 Subthreshold Behavior

Since it reveals information on the overall device leakage properties, the discussion of the subthreshold behavior is of particular interest for this work. The subthreshold behavior of the different samples shall also be discussed using transfer characteristics, here presented in semilogarithmic scale in figure 3.11. Also depicted in the figure are the absolute values of the simultaneously recorded gate source currents. For the sake of clarity, the curves of the eight samples are depicted in four graphs, where figures 3.11(a) (1000 nm and 450 nm samples) and 3.11(b) (200 nm and 50 nm samples) show the transfer characteristics of the GOS MISHEMTs and figures 3.11(c) (1000 nm and 450 nm samples) and 3.11(d) (200 nm and 50 nm samples) those of the standard HEMTs.

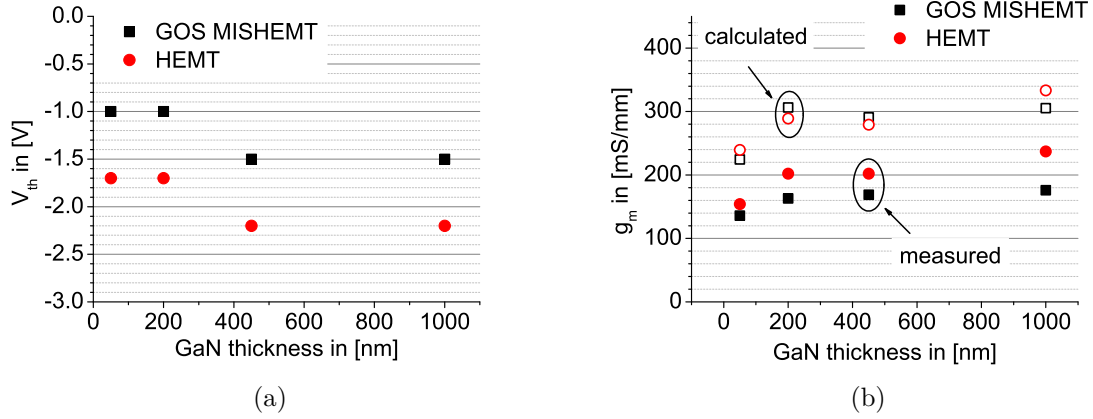


Figure 3.10: Threshold voltage V_{th} extracted through linear extrapolation (a) and measured, maximum extrinsic (solid symbols) and calculated, intrinsic (open symbols) transconductance g_m (b) vs. GaN buffer thickness for MISHEMTs (black squares) and the conventional (red circles) GaN HEMTs. The respective transconductances were extrapolated at $V_{GS} \approx -0.5$ V.

Since the graphs are depicted in absolute current scale, it is worth remembering that the presented devices have a gate-width of $50 \mu\text{m}$. The off-state current I_{off} is the residual current under complete pinch-off conditions and includes all parasitic leakage currents, i.e. gate-source leakage, buffer leakage and leakage around the active device area. Apart from the 450 nm and 1000 nm GaN GOS MISHEMT samples, the measured gate-source and drain-source currents below threshold are almost identical ($I_{GS} \approx I_{DS}$). This suggests that I_{off} is usually dominated by gate leakage (as discussed in section 2.4). Independent of the buffer layer thickness, the gate leakage currents of the MISHEMTs are in the lower pA range. These very low gate-leakage currents are due to the thermal oxide on the InAlN surface [38]. The residual I_{DS} of the two thick samples are due to a residual buffer conductivity (leakage between contact pads is negligible as suggested by figure 3.6(b)) and are in the range of a few hundred pA, however, slightly decreasing with decreasing V_{GS} for the 450 nm GaN sample and nearly constant at 0.5 nA for the 1000 nm sample. As a result the current on/off ratios are larger than 10^7 . For the 200 nm and the 50 nm GaN sample the residual I_{DS} are approximately $I_{off} \approx 5$ pA and even $I_{off} \approx 1$ pA, respectively. Consequently very high current on/off ratios of larger than 10^9 and 10^{10} are obtained for the 200 nm and the 50 nm GaN buffer sample. Yet, no clear relationship between buffer layer thickness and I_{off} can be observed. However, the trend of reduced I_{off} with decreasing buffer thickness is evident. In contrast, standard HEMTs exhibit significantly larger gate leakage currents ranging from 20 nA (50 nm GaN sample) to 1.6 μA (200 nm GaN sample), which is the reason why the residual buffer leakage currents (or leakage around the active device) cannot be estimated. Although these devices exhibit much higher output current densities (up to 40 % more, see figure 3.8(a)), due to the much higher leakage currents (several orders of magnitude) the current on/off ratios are reduced to values between 10^4 and 10^6 . These findings are a very strong

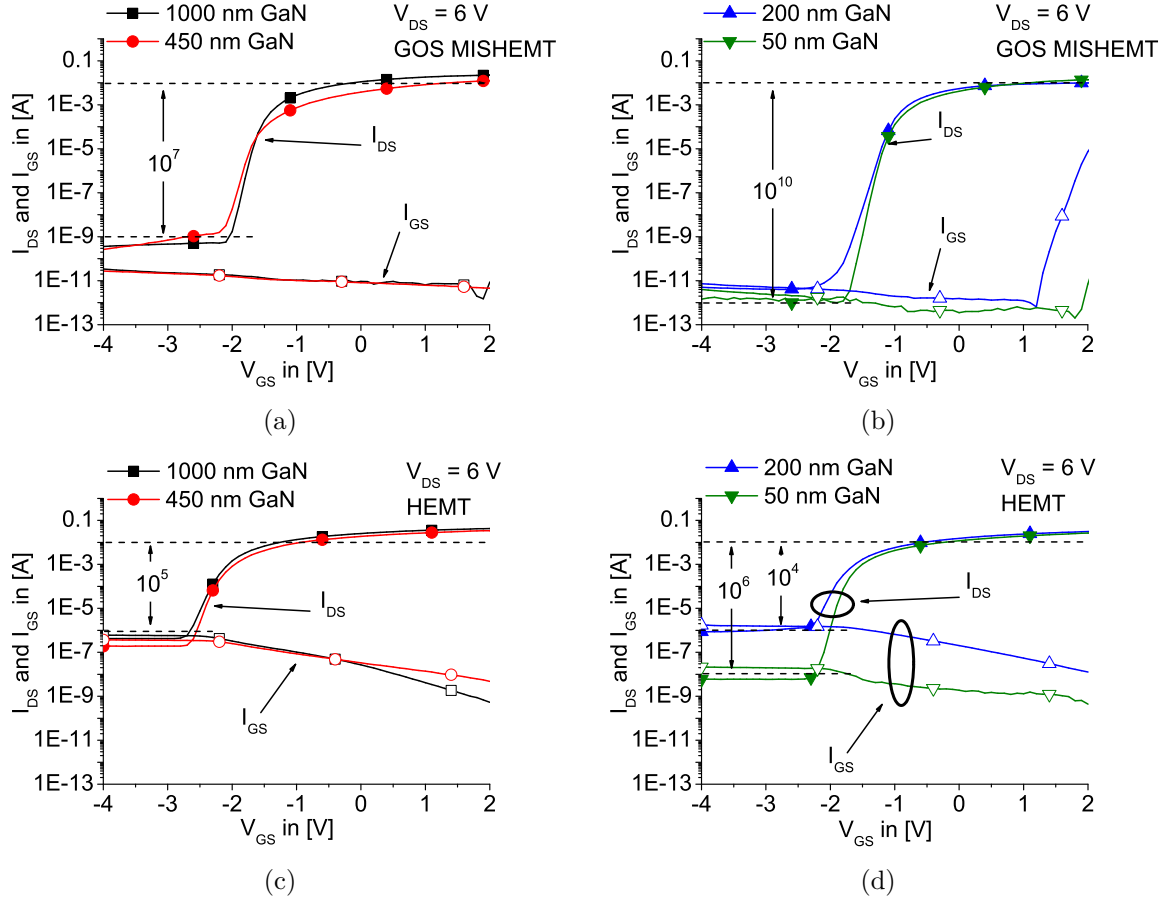


Figure 3.11: Transfer characteristics in semilogarithmic scale of (a) the 1000 nm and 450 nm MISHEMTs, (b) the 200 nm and 50 nm MISHEMTs, (c) the 1000 nm and 450 nm HEMTs, and (d) the 200 nm and 50 nm HEMTs. Solid symbols correspond to measured I_{DS} , open symbols to simultaneously recorded I_{GS} . The gate-width is 50 μm .

evidence for the efficient improvement of leakage properties when employing the GOS technology in combination with InAlN/GaN heterostructures with extremely thin GaN buffers.

The extremely low off-currents of the two thin buffer samples are surprising, because a high defect density is expected close to the 2DEG channel (see figure 3.3). However, they confirm results previously reported on thin buffer InAlN/GaN HEMTs [75]. While the reduction of the gate leakage currents can clearly be assigned to surface oxidation, the only evident explanation for the reduction of buffer leakage with decreasing GaN thickness is the reduction of the device cross-section. In order to pursue this idea further figure 3.12 summarizes the extracted off-currents of devices with different gate width. The off-currents are extracted at $V_{GS} = -4.0$ V and $V_{DS} = 6.0$ V and are depicted for the GOS MISHEMTs in figure 3.12(a) (1000 nm, 450 nm) and 3.12(b) (200 nm, 50 nm) and for the standard HEMTs in figure 3.12(c) (1000 nm, 200 nm) and 3.12(d)

(450 nm, 50 nm). Note the different scales of the individual graphs as well as the different combinations of samples within one figure. The investigated gate-widths are $W_G = 25 \mu\text{m}$, $W_G = 50 \mu\text{m}$, and $W_G = 100 \mu\text{m}$. As mentioned above, the lowest off-currents are observed for the two thin GaN buffer MISHEMTs (figure 3.12(b)). Their respective off-currents are independent of W_G and are approximately 1 pA to 2 pA for the 50 nm sample and vary between 5 pA and 11 pA for the 200 nm sample. Thus, within the resolution limit of the measurement equipment no correlation can be found between the device cross-section and the off-current. Different behavior is observed for the 450 nm GaN and 1000 nm GaN samples. These two MISHEMT samples are the only FETs, where the off-current is clearly dominated by a residual buffer leakage, since leakage between contact pads could be excluded. They exhibit a linear dependency of I_{off} on W_G . The extracted residual buffer conductivity is $6.9 \text{ pA}/\mu\text{m}$ and $5.4 \text{ pA}/\mu\text{m}$ for the 1000 nm and the 450 nm GaN sample, respectively. Taking into account the results of the four samples no clear relation between device cross-section and off-currents can be observed. However, the reduction of I_{off} with decreasing GaN thickness is evident.

Considering the standard GaN technology the same trend of decreasing I_{off} with decreasing buffer thickness cannot be observed. Moreover, for none of the buffer layer system a linear relation between I_{off} and W_G can be seen. Nevertheless, in the case of the 1000 nm and the 200 nm sample I_{off} decreases with W_G . A conservative estimate of an I_{off} versus W_G relationship leads to $20 \text{ nA}/\mu\text{m}$ for the 1000 nm and to $15 \text{ nA}/\mu\text{m}$ for the 200 nm sample. It shall be mentioned again that in this case I_{off} is dominated by gate leakage and the estimated relationship does not reflect residual buffer layer leakage. The off-currents of the 450 nm and 50 nm samples vary over a wide range and therefore do not allow the estimation of any gate-width dependency. Speculating on possible explanation for this behavior may lead to the individual crystalline quality of the In-AlN barrier allowing for a certain conductivity along a defect network on the surface or through the barrier (see again 2.4 and reference [53]). In turn, surface oxidation may lead to a strong reduction of the conductivity by screening the effective defect network.

Another interesting parameter, which can be extracted from semilogarithmic transfer characteristics, is the subthreshold swing (SS). The SS is a measure of carrier confinement in the channel and is limited by thermal carrier diffusion to $59.2 \text{ mV}/\text{dec}$ at room temperature. Commonly it is extracted in the voltage regime between the threshold voltage V_{th} and the pinch-off voltage V_{off} and reflects how sharp a HEMT device can be biased from the on-state to the off-state or vice versa, where low values of SS present sharp transitions. Shown in figure 3.13 are the at $V_{\text{DS}} = 6 \text{ V}$ extracted SS of $50 \mu\text{m}$ wide devices. In general, pinch-off of the MISHEMT devices is sharper compared to the standard GaN devices and SS well below $100 \text{ mV}/\text{dec}$ are extracted. The exact values of SS for the GOS MISHEMTs are: $\text{SS} = 80 \text{ mV}/\text{dec}$, $\text{SS} = 98 \text{ mV}/\text{dec}$, $\text{SS} = 82 \text{ mV}/\text{dec}$, and $\text{SS} = 73 \text{ mV}/\text{dec}$ for the 1000 nm, the 450 nm, the 200 nm, and the 50 nm GaN buffer sample, respectively. Especially the $73 \text{ mV}/\text{dec}$ of the 50 nm GaN sample suggests a rather strong carrier confinement in the 2DEG channel and compares well to values that are reported in literature for planar GaN-based HEMTs [59]. A possible explanation

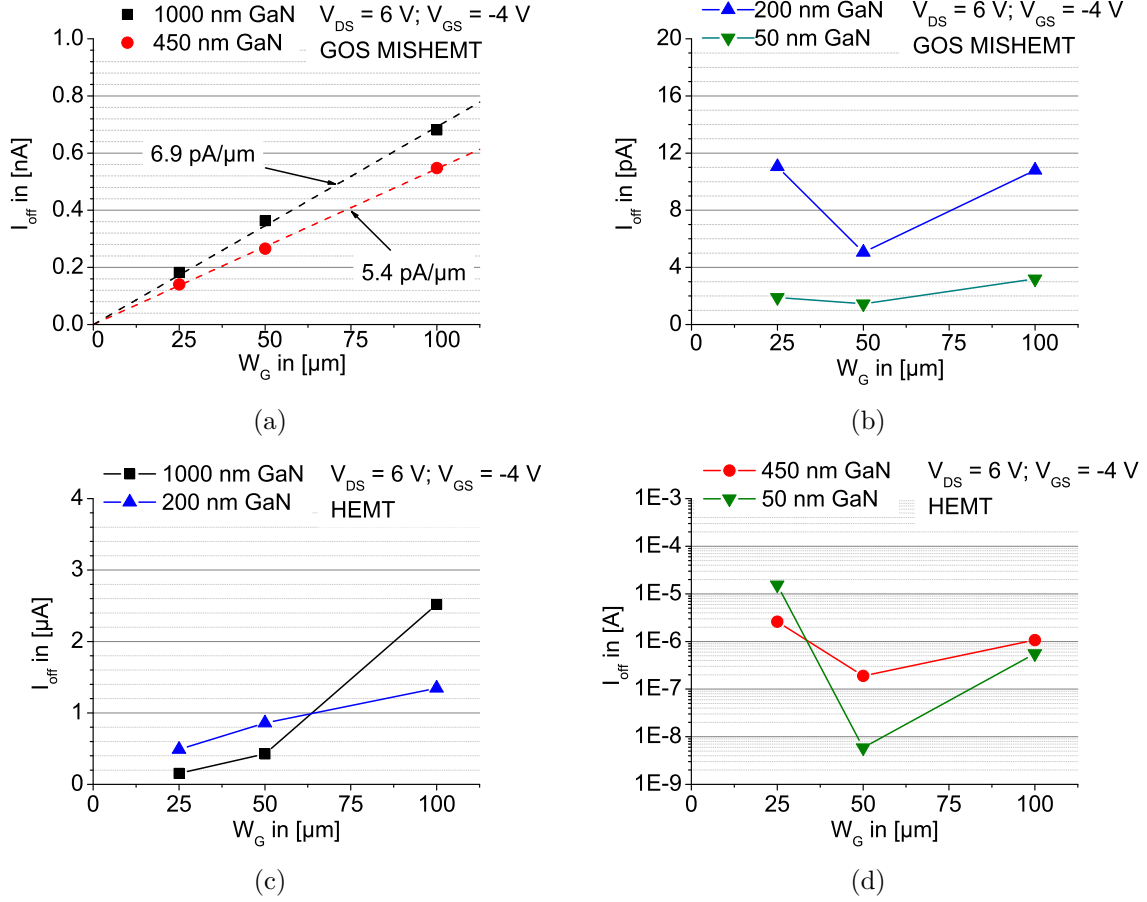


Figure 3.12: I_{off} vs. gate-width W_G extracted at $V_{\text{DS}} = 6 \text{ V}$ and $V_{\text{GS}} = -4 \text{ V}$ for (a) the 1000 nm and the 450 nm MISHEMTs, (b) the 200 nm and 50 nm MISHEMTs, (c) the 1000 nm and 200 nm HEMTs, and (d) the 450 nm and 50 nm HEMTs. A residual buffer current of 6.9 pA/ μm (black dashed line in (a)) and 5.4 pA/ μm (red dashed line in (a)) can be extracted for the two thick GaN buffer MISHEMTs. Note the different scales of the presented graphs.

for this low value may be that, due to the thin GaN layer, the low temperature AlN layer serves as an efficient back barrier. Then, the whole system can be considered as double heterostructure system, which is known to enhance carrier confinement [60, 61, 82]. Apart from the 50 nm sample ($\text{SS} = 92 \text{ mV/dec}$), all standard HEMT devices exhibit a SS larger than 120 mV/dec. A strong correlation between SS and gate leakage currents was reported in [28], which is qualitatively confirmed in this experiment (see figure 3.12).

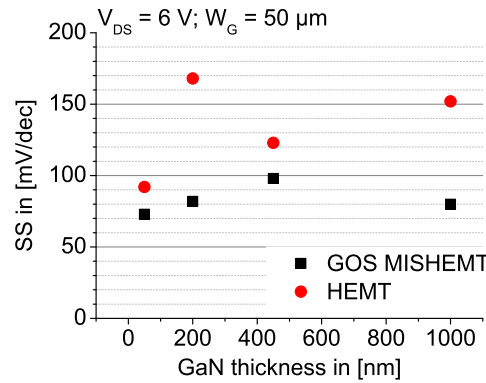


Figure 3.13: Subthreshold swing (SS) vs. GaN buffer thickness extracted for 50 μm wide MISHEMTs (black squares) and HEMTs (red circles).

3.4 Partial Summary

As a summary of this chapter, it may be concluded that the GaN-on-Sapphire technology is a powerful tool to address leakage currents like gate-source leakage, buffer leakage, and inter device or pad leakage. The key features of this technology are the deep mesa isolation process, the thermal oxidation of the InAlN barrier, and the downscaling of the GaN buffer thickness. Deep mesa isolation process allows to confine the active device area to a small region and the positioning of the contact pads directly on the highly insulating sapphire. In consequence, leakage currents between contact pads and different devices can be neglected. Thermal oxidation reduces leakage currents through the gate diode to the lower pA regime. The reduction of the GaN buffer layer thickness is accompanied by a strong reduction of buffer leakage. In total, the leakage currents of such prepared GOS MISHEMTs are in the range of few pA and at least three orders of magnitude smaller compared to their standard HEMT counterpart, leading to sharp pinch-off, high-current on/off ratios and good carrier confinement. Such GOS MISHEMT device features are very attractive for high power and high-temperature applications, where device degradation is commonly ascribed to parasitic leakage currents.

4 Thin Body InAlN/GaN MISHEMT: Device Operation up to 600 °C

To this day, high-temperature semiconductor electronics often refers to temperatures of approximately 200 °C [83], and is mainly discussed within the frame of Si and GaAs technologies. Although for both technologies high-temperature operation beyond 400 °C was demonstrated by either using the Silicon-on-Insulator (SOI) technology [84] or utilizing a low-temperature GaAs buffer [85], this temperature regime had remained the domain of ceramics and electro-ceramics. Silicon carbide (SiC) has been investigated for several decades and was the first semiconductor penetrating this temperature regime, lately resulting in long-term analogue device operation at 500 °C [86] and digital logic devices at 550 °C [87]. However, the rather new GaN-based heterostructures can also possess ceramic-like properties [88] and therefore may be an attractive alternative in the field of high-temperature applications. Indeed, InAlN/GaN HEMTs in its lattice-matched material configuration have already demonstrated device operation at temperatures as high as 1000 °C [13, 24]. The key to access such harsh ambient temperatures was the use of a device metalization scheme similar to that of the GOS device technology presented in section 3.2. Although no degradation of the heterostructure itself was observed, those results indicated that the high-temperature device operation was seriously limited by buffer leakage, also caused by areas outside the active device. Thus, lattice matched InAlN/GaN HEMTs prepared in the GOS technology, where leakage currents outside the active device are essentially eliminated, may lead to more stable and reliable high-temperature electronics.

As mentioned previously, leakage currents may be one source for device degradation, thus limiting the reliability and the life-time of a device. Ideally, the intrinsic carrier concentration in the GaN buffer reaches that of Si at around 600 °C and device leakage should still be controllable at such temperature. However, other leakage current mechanisms may be activated with increasing temperature (defect activation in the buffer, enhanced electron emission across the gate barrier), which is why the choice of HEMTs with initially low overall device leakage characteristics for high-temperature tests is apparent. Among the prepared GOS MISHEMTs, the two thin samples, i.e. with a 50 nm and with a 200 nm GaN buffer, exhibit the lowest off-currents and therefore present the ideal candidates for high-temperature operation. Since it might be of particular interest, in this work the high-temperature device operation of the thinnest GOS MISHEMT (50 nm GaN buffer + 50 nm AlN nucleation layer) will be discussed. Nonetheless, apart

from increased leakage currents also other phenomena might be observed when rising the temperature and can have a significant influence on the FET characteristics at high temperatures. For example, the properties of the 2DEG, i.e. the carrier concentration n_s and the electron mobility μ_{el} , thus the sheet resistance $R_{sh} = \frac{1}{qn_s\mu_{el}}$, can vary with temperature. At temperatures above room temperature (RT) the electron mobility is expected to be limited by phonon scattering given by a temperature dependent mobility of $\mu_{el} \propto T^{-3/2}$. The charge carrier concentration in the 2DEG is a result of the discontinuity of the total polarization between the InAlN barrier and the GaN buffer. Thus, changes of the polarization (piezoelectric or spontaneous), e.g. due to different thermal expansion coefficients of the lattices, result in a changed n_s . In addition, this would then lead to mechanical stress in the heterostructure. Nevertheless, these effects can be assumed as reversible effects only occurring during temperature stress (although mechanical stress could lead to the generation of defects). However, there might be other phenomena leading to a permanent change or degradation of the FET properties. Such permanent changes could possibly occur on the FET surface, e.g. through high-temperature corrosion or continued oxidation, or in the bulk material, e.g. through diffusion of Ga-atoms into the barrier or In- and Al-atoms to the buffer.

The first experiments presented in the following, shall give an insight into the high-temperature behavior of such thin body InAlN/GaN MISHEMTs. An estimation of the temperature dependent 2DEG properties is done by an evaluation of the sheet resistance and the threshold voltage, which in turn is also based on a discussion of the temperature dependent FET characteristics. Like in the previous chapter, the discussion of the subthreshold behavior is based on semilogarithmic transfer characteristics, which simultaneously will be used in an attempt to extract the activation energy of parasitic conduction mechanisms. In case of this thin heterostructure system (InAlN/AlN/GaN/AlN : 5/1/50/50 nm), an investigation of the (long-term) compound and surface stability may be of particular interest, since a rather high defect density can be expected within the device structure (see again section 3.3). To gather a first set of information on the stability, long-term storage, large-signal RF operation and break-down measurements (at high temperatures) were performed. Apart from the break-down measurements, all measurements presented in the following were conducted using one individual device. Nonetheless, these results may present an indication for the reliability and life-time of thin body GOS MISHEMTs. To analyze the device with respect to these before mentioned parameters the measurement procedure presented in the following was used.

High-temperature measurements were done using two different measurement setups. Measurements from room temperature (RT) up to 300 °C were conducted in atmosphere with a conventional probe station, where the sample was placed on a hot plate. To avoid high temperature corrosion, measurements at temperatures between 400 °C and 600 °C were performed under vacuum conditions in a self-made high-temperature measurement chamber (HTMC). The base pressure inside the chamber during experiments was $p \approx 10^6$ mbar. High-temperature stable tungsten carbide (WC) needle probes

were used for device contacting. The investigated temperatures above room temperature ranged from 100 °C to 600 °C in temperature steps of 100 °C. A complete set of HEMT DC characteristics was recorded at each temperature. For temperatures above 300 °C and before characterization at the next higher temperature, the sample was always cooled down to RT and characterized again at RT, thereby monitoring any permanent change in the device properties. To avoid temperature spikes ramping up to the test temperature in the HTMC was done within a two hours period, regardless of the exact test temperature. Soon after the test temperature was reached a first set of DC characteristics was recorded. A second set of characteristics was recorded after a 100 hour storage period (unbiased device). Before cooling down additional break-down and large-signal class A measurements at a test frequency of 1 MHz were performed. It shall be noted already here that no significant differences between the various RT characteristics were observed. Therefore, in the following only the data after the 600 °C stress are depicted. Likewise, the high-temperature characteristics before and after the 100 hours storage were nearly identical, which might be linked to the rather slow ramp up process. All high-temperature characteristics presented in the following were recorded after the 100 h storage. Furthermore, apart from breakdown measurements all presented data were obtained from the identical device. At this point, the support of David Maier, member of InAlN/GaN group in the EBS, shall be mentioned, who designed the HTMC, established the corresponding data acquisition system, and whose collaboration, especially for measurements in the HTMC, was essential.

4.1 2DEG Properties at High Temperatures

Figure 4.1 summarizes the change of the sheet resistance, extracted from TLM measurements, and the change of threshold voltage, extracted from linear transfer characteristics at $V_{DS} = 6$ V (see below), with temperature. More precisely, plotted in figure 4.1(a) is the change of the sheet conductivity $1/R_{sh}$ against $1000 \cdot T^{-3/2}$. The corresponding temperature in °C and the sheet resistance is given on the top x-axis and right y-axis. Most noticeably is the different behavior of R_{sh} under vacuum and under ambient conditions. The initial sheet resistance at room temperature was $R_{sh} = 710 \Omega$. Under vacuum, it increased to a maximum value of $R_{sh} = 1438 \Omega$ at 600 °C, which is approximately the double of its room temperature value. For phonon scattering dominated behavior the change of the sheet conductivity is expected to follow the $T^{-3/2}$ law, and indeed a linear relationship can be extracted. This, together with a nearly unchanged threshold voltage (see figure 4.1(b)), suggests that the 2DEG electron mobility at 600 °C is $\mu_{el} \approx 550 \text{ cm}^2/\text{Vs}$. Different behavior is observed for measurements in atmosphere, where the sheet resistance is dramatically affected at even lower temperatures. Following the $T^{-3/2}$ trend-line in figure 4.1(a), the mobility at 300 °C could be estimated to $\mu_{el} \approx 680 \text{ cm}^2/\text{Vs}$, where the sheet resistance should be $R_{sh} = 1150 \Omega$. Instead, the resulting sheet resistance was nearly three times higher at $R_{sh} = 3350 \Omega$. This high

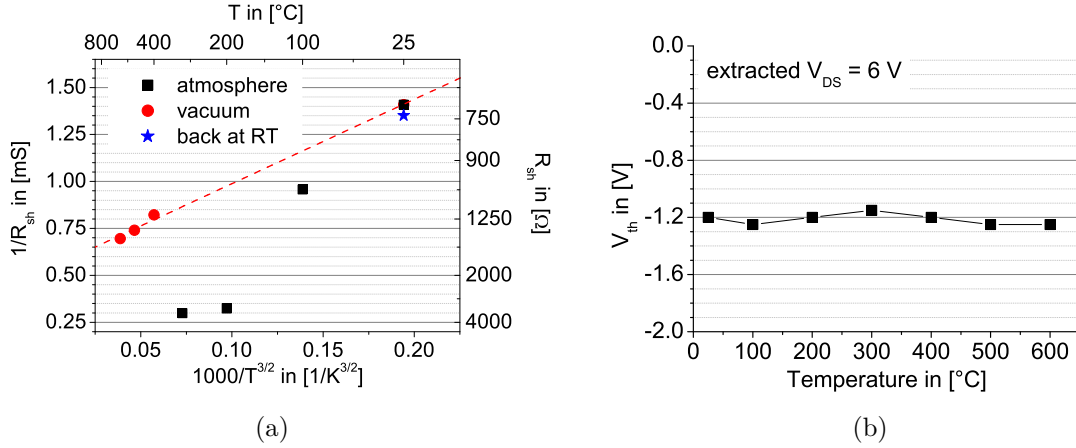


Figure 4.1: (a) Change of sheet conductivity $1/R_{sh}$ with temperature. The corresponding sheet resistances are labeled on the right axis. The temperatures in $^{\circ}\text{C}$ are given on the top axis. Under vacuum (red circles) $1/R_{sh}$ follows the $T^{-3/2}$ law. (b) Change of V_{th} with temperature. V_{th} varies only slightly around its RT value.

difference between estimated and measured R_{sh} then needs to be related to a change of the 2DEG carrier concentration of approximately $N_{S,300} \approx \frac{1}{3} \cdot N_{S,RT}$. However, the threshold voltage varies only slightly ($\Delta V_{th} \approx 50 \text{ mV}$) with temperature. According to equation (2.7) such a variation of V_{th} corresponds to a change in the carrier concentration of $\Delta n_s \approx 4 \%$. This suggests that this effect is linked to the free, unpassivated gate-source and gate-drain region. Since the measurements in atmosphere had been conducted before the measurements in vacuum, this seems like a non-permanent and reversible change and supports the suggestion that the depletion might be caused by adsorbates from the environment on the free surface depleting the surface donor and consequently the 2DEG electrons (compare figure 2.4). Then, it may be concluded that a proper passivation on top of the oxidized InAlN surface can reduce the influence of adsorbates on the 2DEG concentration.

4.2 High-Temperature FET Characteristics

Figure 4.2(a) compares the output characteristics at different temperatures for a fully open channel, i.e. for a gate-source voltage of $V_{GS} = 2 \text{ V}$. The relative change of the peak current density I_{max} with temperature is shown in figure 4.2(b). Similar to the case of TLM measurements different behavior is observed for measurements in atmosphere and in vacuum. The initial peak current density at room temperature was $I_{max} = 0.38 \text{ A/mm}$. In atmosphere I_{max} decreased with temperature down to $I_{max} = 0.12 \text{ A/mm}$ at 300°C . This is equivalent to a reduction of approximately 68 % and is consistent with the reduction of n_s extracted by the TLM measurements. In vacuum the surface adsorbates

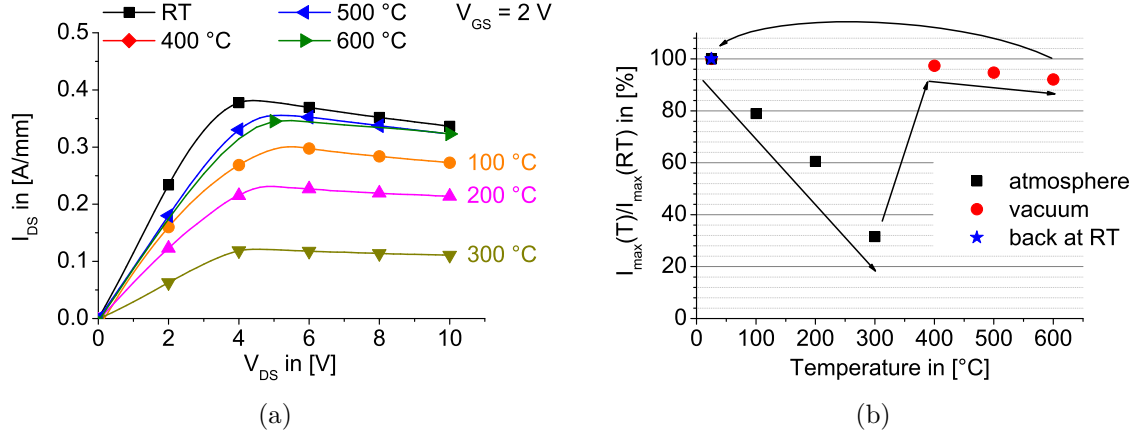


Figure 4.2: (a) Temperature dependent output characteristics at $V_{GS} = 2$ V. (b) Corresponding change of peak current density relative to RT.

have desorbed and the initial n_s was restored (no change of V_{th} , R_{sh} follows $T^{-3/2}$ law). The peak current density at 600 °C was $I_{max} = 0.35$ A/mm. Hence, the relative change of I_{max} from RT to 600 °C is less than 8 % and much less than expected by the change in the mobility. This supports the assumption that, despite of the elevated temperature, device operation is still dominated by the electron saturation velocity. The weak temperature dependency might be linked to a rather temperature insensitive electron saturation velocity under high electrical fields [89, 90] and the associated extremely high electron temperature of larger than 2000 K [91].

The linear transfer characteristics recorded at different temperatures at a drain-source voltage of $V_{DS} = 6$ V are shown in figure 4.3(a). To keep the graph simple, only the curves at RT, 100 °C, 300 °C, and 600 °C are presented. At a first glance it seems the threshold voltage V_{th} has changed with temperature, especially for the measurements in atmosphere, which could also be expected due to the depleted 2DEG channel. However, it can be seen later (compare figure 4.4) that this observation is related to the reduced output current and to the linear presentation. Therefore, the depletion of the 2DEG carrier concentration occurred only under the free InAlN surface, but not under the gate metal itself indicating that the depletion was caused by surface adsorbates. Although the extraction of the transconductance at different temperatures (see figure 4.3(b)) results in a graph of similar shape as the sheet conductivity $1/R_{sh}$ the change of g_m from RT to any other temperature is significantly lower than the change of $1/R_{sh}$. Considering for example the values obtained at RT and 600 °C, the sheet conductivity at 600 °C was approximately 50 % of its RT value. In contrast the transconductance at RT was $g_m = 136$ mS/mm and changed at 600 °C to $g_m = 110$ mS/mm, which is still more than 80 % of its initial value. Furthermore, at 400 °C the extracted g_m remained nearly unchanged at 130 mS/mm. These findings are in line with the nearly unchanged I_{max} at temperatures beyond 400 °C, again being a strong indication for saturation velocity dominated device operation.

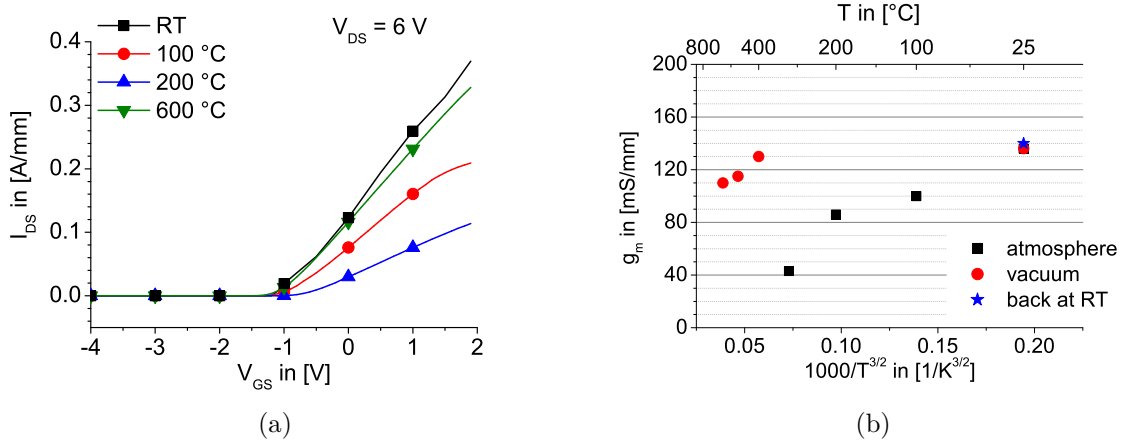


Figure 4.3: Linear transfer characteristics recorded at $V_{DS} = 6$ V presented for RT, 100 °C, 300 °C, and 600 °C (a). Change of the extracted transconductance g_m versus temperature (b). Black squares, red circles, and the blue star correspond to measurements in atmosphere, in vacuum, and at RT after high-temperature tests, respectively.

4.3 Subthreshold Behavior

The discussion of the subthreshold behavior at higher temperatures is in particular interesting, because parasitic leakage currents as discussed in chapter 2.4 may be activated with temperature and can slowly lead to device failure. Like before, also here the subthreshold behavior of such a thin body InAlN/GaN MISHEMT shall be discussed by its semilogarithmic transfer characteristics presented for different temperatures in figure 4.4. It shall be mentioned that for measurements in the high-temperature measurement chamber it is not possible to simultaneously record the drain-source and gate-source current, which is the reason why the I_{GS} curves are not presented in this figure. Instead, the two-terminal gate-source characteristics (floating drain contact) were recorded revealing in reverse direction a gate-source leakage current of the same order of magnitude as the presented off-currents (see appendix C). This suggests that the off-currents at higher temperatures are limited by leakage currents arising at the gate diode. However, a contribution of the buffer cannot be excluded. The voltage, where the channel is completely depleted, is $V_{off} \approx -1.9$ V and remained nearly constant for all temperatures indicating again a constant sheet charge concentration in the channel, thus the absence of pyroelectric effects and a high thermal stability of this very thin lattice matched InAlN/GaN heterostructure system. The small variations are due to the temperature sensitivity of the subthreshold swing (see below). As already mentioned, the off-current at room temperature was $I_{off} \approx 1$ pA and increased only slightly to $I_{off} \approx 5$ pA and $I_{off} \approx 13$ pA at 100 °C and 200 °C, respectively. For both temperatures this still corresponds to current on/off ratios of 10^9 . At 300 °C the off-current increased further to $I_{off} \approx 220$ pA and consequently the on/off ratio decreased to 10^7 . With higher temperatures the off-currents increased further reaching a value of $I_{off} \approx 13$ nA at 600 °C, which is equivalent to a,

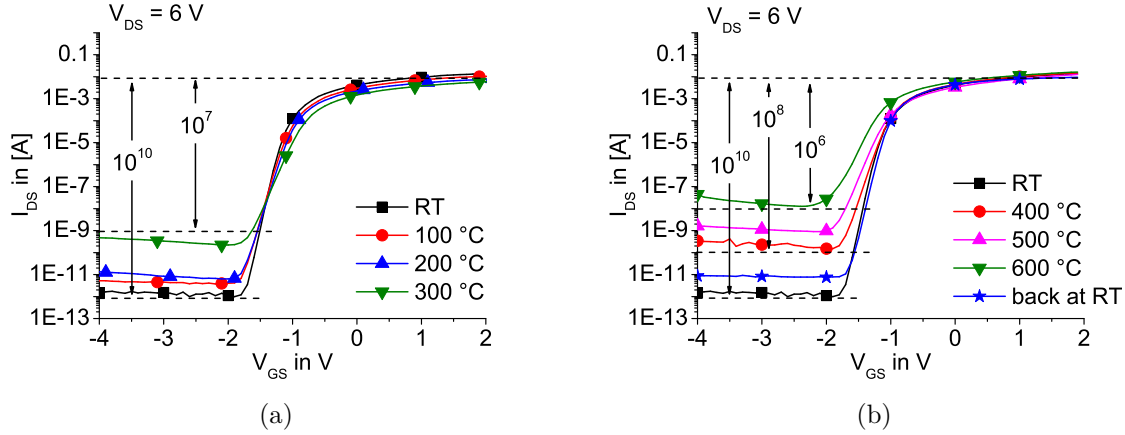


Figure 4.4: Semilogarithmic transfer characteristics recorded at $V_{DS} = 6$ V for temperatures up to 300 °C in atmosphere (a) and up to 600 °C in vacuum and back at RT after high-temperature test (b). First published in [92].

at this temperature, extremely high current on/off ratio of larger than 10^6 . Owing to its superior room temperature performance, this I_{off} of 13 nA together with the current on/off ratio of larger than 10^6 at 600 °C is still better than what was extracted at RT for devices with standard GaN technology (compare section 3.3). Also of interest is the transfer characteristics (see figure 4.4(b)) recorded at room temperature, after all high-temperature tests had been conducted including RF large-signal class A measurements under strong forward and reverse gate bias conditions (see below). Apart from a slightly increased off-current to $I_{off} = 8.7$ pA, no evidence for any device degradation was observed and nearly identical HEMT characteristics as before were obtained, again indicating the very high stability of both, the device metallurgy and the heterostructure system despite the ultrathin buffer configuration.

Figure 4.5(a) summarizes the resulting off-currents in an Arrhenius plot representation. Two different regions can be identified in the Arrhenius diagram. One, with a moderate increase of I_{off} , from RT to 200 °C and another, associated with a steeper increase, ranging from 400 °C to 600 °C. The obtained data at 300 °C does not fit any of these two regions. This might be related to the use of different measurement setups, but could also be due to a not identified third activation energy between 200 °C and 400 °C. However, no additional experiments were conducted. The total change from room temperature to 200 °C was approximately 11 pA, which is equivalent to an increase by one order of magnitude. With such a rather low increase of I_{off} an activation energy of $E_A = 0.15$ eV can be extrapolated from the Arrhenius diagram. The role of surface adsorbates as a source of surface leakage currents remains unclear, but their effect seems negligible. In the temperature region between 400 °C and 600 °C, the off-state currents increased further by approximately 2 orders of magnitude from which an activation energy of $E_A = 1.1$ eV can be extrapolated. The two extracted activation energies are commonly observed for defects in GaN structures [93], but, due to thin buffer

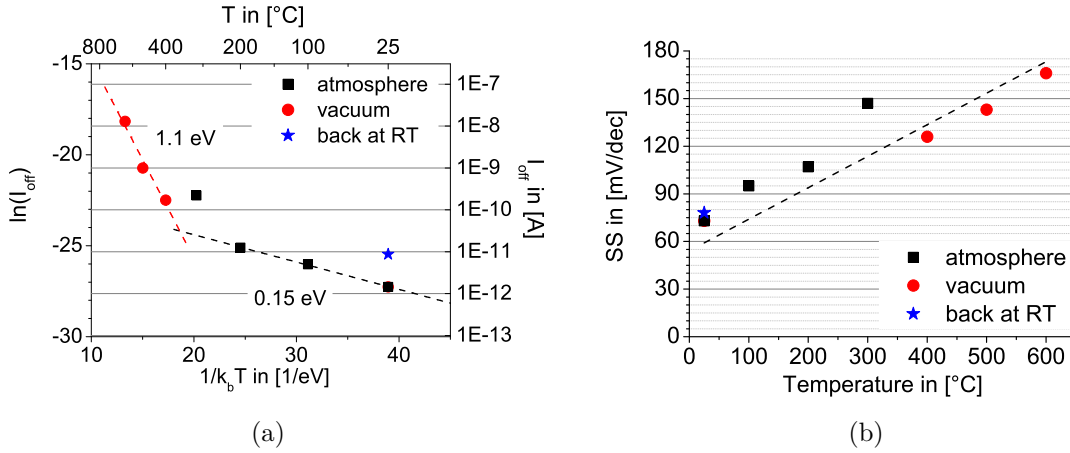


Figure 4.5: (a) Change of the minimal off-currents I_{off} with temperature in Arrhenius plot representations. Activation energies of $E_A = 1.1 \text{ eV}$ (red dashed line) and $E_A = 0.15 \text{ eV}$ (black dashed line) can be extracted. (b) Change of the subthreshold swing SS with temperature extracted from the semilogarithmic transfer characteristics of figure 4.4.

configuration used in this case, they may also be linked to defects in the low temperature AlN nucleation layer.

As already mentioned, the subthreshold swing SS of the HEMT is strongly affected by the ambient temperature, but presents a measurable quantity for carrier confinement and pinch-off behavior. Thus, very sharp pinch-off and a strong carrier confinement is not possible at very high temperatures. In consequence leakage currents through the buffer may become more noticeable. The change of the extracted and the calculated SS (calculated after equation (2.9)) is shown in figure 4.5(b). At room temperature, a very low value of $SS = 73 \text{ mV/dec}$ was extracted. The extracted SS increased with increasing temperature approaching 165 mV/dec at 600°C . Within temperature measurement precision, SS follows closely the theoretical predictions again indicating the high thermal stability of the material system.

Additional measurements supporting the high stability of such an ultrathin buffer lattice matched InAlN/GaN HEMT are breakdown measurements under pinch-off conditions $V_{\text{GS}} < V_{\text{off}}$. Measurements were performed at different temperatures on other devices with the identical geometry. Since the knowledge of the device geometry is essential for a proper analysis it is briefly repeated in the following: $W_G = 50 \mu\text{m}$, $L_G = 0.25 \mu\text{m}$, $L_{\text{DS}} = 3 \mu\text{m}$, and $L_{\text{GS}} = 1 \mu\text{m}$. For these breakdown measurements a gate-source bias point in pinch-off was chosen. Simultaneously, the drain-source voltage was ramped up, while monitoring the resulting drain current. In order to avoid breakdown through the air, the sample was passivated with a fluorine-based liquid (Fluorinert). Its boiling point is approximately 56°C , which is why its application in atmosphere is limited to measurements around room temperature. On the other hand, due to the high vacuum

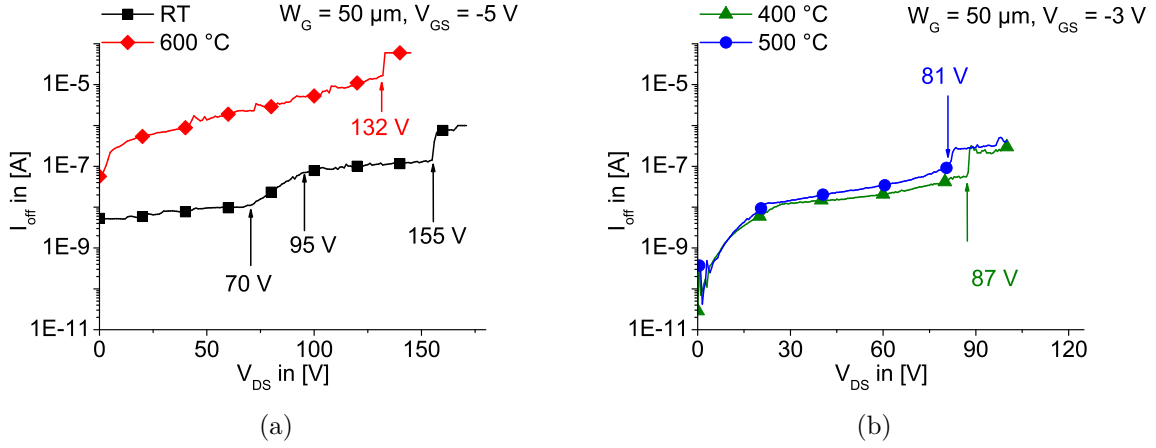


Figure 4.6: Measurements of HEMT breakdown under pinch-off conditions (a) at RT and 600 °C with $V_{\text{GS}} = -5 \text{ V}$ and (b) at 400 °C and 500 °C with $V_{\text{GS}} = -3 \text{ V}$. First published in [96].

inside the high-temperature measurement chamber ($p \approx 10^{-6} \text{ mbar}$), the sample can be considered vacuum passivated and an additional passivation was not necessary. The results of breakdown measurements at different temperatures are shown in figure 4.6.

At room temperature, 400 °C and 500 °C two current plateaus of rather constant I_{off} can be identified. At room temperature I_{off} was nearly constant up to $V_{\text{DS}} = 70 \text{ V}$. Between 70 V and 95 V I_{off} increased by approximately one order of magnitude and remained again constant up to 155 V, where catastrophic breakdown leading to device failure occurred. At 400 °C and 500 °C a sudden increase of I_{off} (also approximately one order of magnitude) was observed at $V_{\text{DS}} = 87 \text{ V}$ and $V_{\text{DS}} = 81 \text{ V}$, respectively. In order to avoid catastrophic breakdown, the measurement had been stopped at $V_{\text{DS}} = 100 \text{ V}$. The different current plateaus indicate the existence of trap levels, which can be filled at higher fields causing the nondestructive, soft breakdown behavior. Similar behavior was reported in GaAs FETs [94] or thin SiO_2 gate dielectric layers [95] and is usually ascribed to the so-called trap-filling phenomenon. However, a detailed analysis would require time resolved measurements and may lead beyond the scope of this work. At 600 °C, the plateau of lower off-current vanished and the device had been driven into destructive breakdown occurring at $V_{\text{DS}} = 132 \text{ V}$, which is only slightly lower compared to the RT value. This indicates that high-power operation of thin buffer InAlN/GaN MISHEMTs is possible even at temperatures as high as 600 °C with only slightly degraded characteristics compared to room temperature.

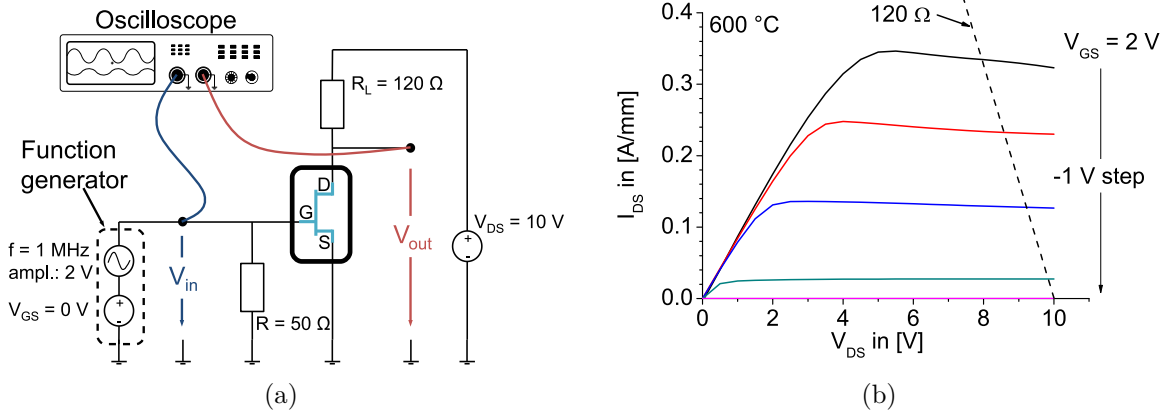


Figure 4.7: (a) Sketch of the measurement setup used for RF large-signal class A measurement. The input and output voltage is monitored with an oscilloscope. (b) DC HEMT output characteristics at 600 °C with depiction of the 120 Ω load line.

4.4 RF Large-Signal Class A Measurements

As already mentioned, at temperatures beyond 400 °C additional large-signal measurements under class A conditions had been performed after the DC characterization and the 100 hour long high-temperature storage. Also a reference measurement at room temperature was done. Due to the lack of high-temperature microwave probes, the test frequency was limited to the lower MHz regime and 1 MHz was chosen. The used measurement setup is sketched in figure 4.7(a). The device inside the high-temperature measurement chamber was contacted by tungsten carbide needle probes. The gate-source input voltage was generated by a function generator, where the DC bias point was $V_{GS} = 0$ V and, in order to determine the gate-diode stability, the applied voltage swing was $\Delta V_{GS} = \pm 2$ V spanning the full range of modulation from fully open channel ($V_{GS} > V_{max}$, with V_{max} being the flat band potential; see again section 2.3) to below threshold ($V_{GS} < V_{th}$). In contrast, in these first experiments the output voltage stress was kept small with a DC bias point of $V_{DS} = 10$ V and a load resistance of $R_L = 120 \Omega$, generating a steep load line to avoid the linear or Ohmic regime of the HEMT. The position of the load line inside the DC HEMT output characteristics recorded at 600 °C is shown in figure 4.7(b). The input and the output waveforms were monitored by an oscilloscope and recorded every 20 seconds over a period of 33 minutes, limited by the data acquisition system (equivalent to 100 recordings). Apart from a small reduction of the maximum peak current density (compare figure 4.2), no significant change of the DC and AC HEMT characteristics from RT to 600 °C (in vacuum) was seen. Therefore in the following only the 600 °C characteristics will be discussed. It shall be noted that results presented in the following are again obtained from the identical device, which was already discussed above (prior breakdown measurements).

The main results of the 600 °C large-signal operation are summarized in figure 4.8. The input and output waveforms (figure 4.8(a)) were recorded after 30 minutes of operation. While the input signal represents a nearly perfect sine wave, the output signal already indicates distortion in both, in forward and reverse direction, which is due to the chosen, large input voltage swing. Clipping in reverse direction was due to driving the input below threshold ($\Delta V_{GS} = \pm 2$ V, $V_{th} = -1.5$ V); clipping in forward direction arose from pronounced gate leakage current of several mA/mm. The rather low peak-to-peak output voltage swing of $V_{pp} = 2.43$ V was obtained through the steep load line of $R_L = 120 \Omega$. The calculated output current swing is depicted in figure 4.8(c) showing more clearly clipping effects in forward and reverse direction. As indicated by figure 4.8(b) the recorded mean current density remained constant at $I_{DS,mean} = 0.18$ A/mm over the whole measurement period, not revealing any evidence for device degradation despite the high gate diode stress (V_{GS} larger than the flat band potential V_{max}) at 600 °C. The peak-to-peak current density was $I_{pp} = 0.36$ A/mm, which is in good agreement with the earlier mentioned DC output current density of $I_{max,600} = 0.35$ A/mm. The resulting output power at 600 °C, calculated after equation (4.1), is $P_{out,600} \approx 109$ mW/mm.

$$P_{out} = \frac{1}{8} \cdot V_{pp} \cdot I_{pp} \quad (4.1)$$

The calculated output power at room temperature is $P_{out,RT} \approx 122$ mW/mm. Therefore, the reduction from RT to 600 °C is approximately 10 % and is in good agreement with the degradation of DC characteristics. These results indicate once again the extremely high, ceramic-like stability of the thin body InAlN/GaN MISHEMT, in this context especially of the gate diode, thus the stability of the native oxide. Owing to the excellent leakage properties provided by the thin buffer (buffer leakage) and the thermal oxidation (gate leakage), large signal class A operation from pinch-off to fully open channel was possible even at 600 °C without any evident degradation. Considering that the device was operating for more than 30 minutes under these harsh conditions the obtained HEMT characteristics when returning back to RT are in particular remarkable, since only a small increase of the off-current was observed. Even though this experiment was not designed for high power amplification, these results together with those of the breakdown measurements indicate that large signal high power operation at 600 °C is feasible using such thin body InAlN/GaN MISHEMTs.

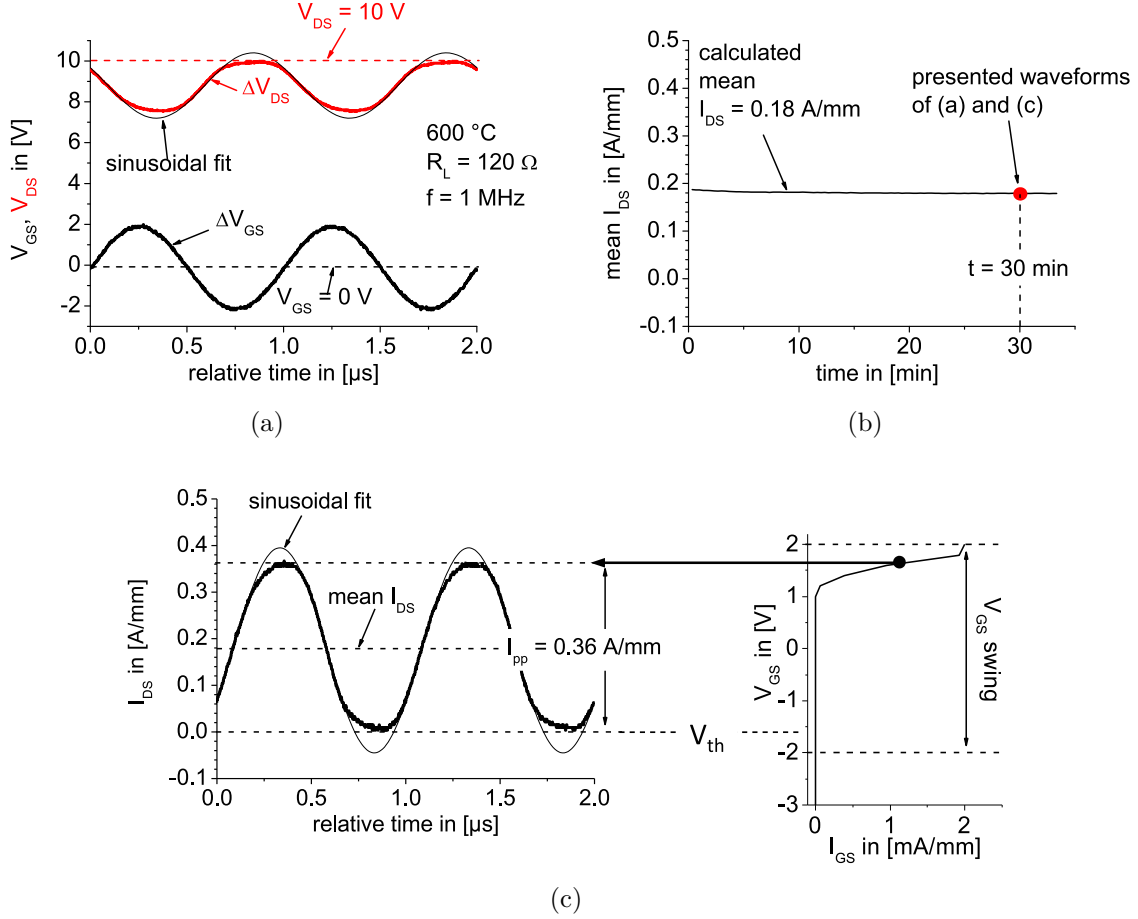


Figure 4.8: Results of large-signal operation at 600 °C. (a) Recorded input (lower black curve) and output (upper red curve) waveforms after 30 minutes of operation. (b) Calculated mean I_{DS} recorded over the whole 33 minutes of operation. (c) Calculated output current swing ΔI_{DS} (left) and two-terminal gate-source characteristics (right) indicating that clipping in forward direction is due increased gate leakage. The thin black curves in (a) and (c) represent a sinusoidal fit of the output signal visualizing clipping in forward and reverse directions. First published in [96].

5 Diamond Electrodes for the Integration with InAlN/GaN HEMTs

Today, diamond has been established as a very versatile material and is used in a wide range of applications like FETs and MEMS [97, 98, 99], microfluidic channel systems [100] or sensors for motion [101] and UV detection [102] or, like in this work, as electrochemical sensor [21, 103]. The growing interest in diamond electronics, and here especially in the field of high-power, high-temperature and high-frequency applications, mainly arose due to its outstanding material properties like its large band gap ($E_G = 5.4$ eV), the high electron and hole mobility ($\mu_h = 3800 \frac{\text{V}\cdot\text{s}}{\text{cm}^2}$, $\mu_{el} = 4800 \frac{\text{V}\cdot\text{s}}{\text{cm}^2}$ [104]), its high breakdown strength ($10 \frac{\text{MV}}{\text{cm}}$ [98]) and the extremely high thermal conductivity (larger than $2000 \frac{\text{W}}{\text{m}\cdot\text{K}}$ [104]). Different diamond FET concepts are discussed in literature. Among these concepts are the surface channel FET, where a p-type conductive layer is induced by the hydrogen termination of the diamond surface, as well as the boron-doped diamond (BDD) FET, where usually a thin boron-doped diamond layer provides p-type conduction [98, 99]. Although fairly good device characteristics, mainly on the single crystalline surface channel FETs, were obtained [105, 106, 107] diamond electronics still lags far behind its predicted performance and in terms of high-power and high-frequency applications is superseded by the competing GaN-based electronics. In this field, due to its high thermal conductivity, diamond is now mainly considered as a top heat spreading layer to boost the performance of high power GaN electronics [18, 108, 109].

As mentioned in the beginning of this chapter, diamond is also used in other applications, where other material properties are more important and diamond may be the material of choice for future device concepts. MEMS applications benefit from its mechanical strength and hardness [110, 111]. Chemical and biological applications take advantage of its high chemical resistance and biocompatibility [7, 8]. If fabricated on a transparent substrate like e.g. sapphire the whole assembly is transparent even into the UV range and allows electrochemical and simultaneous optical spectroscopy measurements [112]. Like noble metal electrodes, BDD allows both, amperometric and potentiometric measurements, but with a significantly larger potential window and lower background current, which potentially allows the analysis of redox systems, even with lower concentrations and in a potential regime that cannot be accessed with conventional electrodes [5, 113].

A prerequisite for the implementation of diamond electrodes for these electrochemical applications is the existence of a conductive layer at the electrode surface. However, there are only few dopants available for diamond and all possess activation energies above 300 meV. Only boron (p-type: $E_A = 0.37$ eV) can be incorporated in such high concentration that quasi-metallic conduction can be obtained even at room temperature. All diamond electrodes discussed in this work are boron-doped diamond electrodes and are referred to as BDD electrodes. Additionally, diamond can exhibit different surface terminations, where mainly the hydrogen- and oxygen-termination are investigated. While H-termination creates a surface channel, O-termination leads to an insulating surface (on intrinsic diamond). O-termination seems more stable than H-termination. In atmosphere the H on the diamond surface is slowly replaced by O leading to different surface properties. Due to the higher stability, oxygen terminated BDD was used. Diamond is usually grown on foreign substrates by a chemical vapor phase deposition (CVD) process, hence usually results in poly- or nanocrystalline diamond (NCD). All BDD electrodes in this work were prepared on sapphire substrates grown by Ziyao Gao, Michele Dipalo or Stefano Rossi, coworkers in the laboratories of the Institute of Electron Devices and Circuits at Ulm University.

The prime focus of this chapter is to introduce the BDD electrode as electrochemical sensor, which presents the second building block of the envisaged electrochemical sensor system, i.e. in combination with GaN-based electronics (see chapter 6). Properties and different applications of BDD electrodes, also with different electrode structures, were previously investigated in detail among others by Carsten Pietzka [113], who also contributed to this work with his experience in the field of electrochemistry and helped with the analysis of several measurements. Based on the results established in [113], this work discusses two sample applications of BDD electrodes on both, planar large area electrode structures and surface modified microelectrode array structures. The first application is related to the detection of ion concentrations in an electrolyte. Here, the concentration of H_3O^+ ions, thus the pH of the electrolyte, leading to a potential difference at the electrode/electrolyte phase boundary, shall be investigated. In combination with the InAlN/GaN HEMT this will then lead to an ion-sensitive FET (ISFET), where the HEMT serves as impedance transformer or amplifier. The second application discussed, is the detection of redox reactions, which are monitored by an electrode current across the BDD/electrolyte interface. In combination with an FET such electrode currents shall be switched on or off meaning that the FET will serve as switch. Both measurement concepts establish different boundary conditions for the combination with the FET, which shall be deduced in this chapter. However, here the electrode shall solely be treated as individual component. Concepts or aspects regarding the integration with GaN electronics, especially with respect to array integration, will be discussed in chapter 6. Although this chapter is very specific to electrochemistry, a detailed discussion of this field is omitted at this point. A more detailed introduction to electrochemistry can be found in the appendix D or in the literature [114, 115].

5.1 BDD Electrode Growth and Fabrication

The growth of diamond layers is usually done in a chemical vapor deposition (CVD) process and relies to relatively low pressures (kPa) and high temperatures ($T > 650\text{ }^{\circ}\text{C}$) in hydrogen-rich atmosphere. Thus, it can be considered a rather harsh process. The source of C-atoms is methane (CH_4) gas, which is highly diluted in molecular hydrogen gas. The methane concentration in the process gas mixture is only up to approximately 2 %. Essential for the growth of diamond is the dissociation of the process gas into carbon-hydrogen radicals and atomic hydrogen, where the atomic hydrogen is used to etch sp^2 -bonds (graphite) at the diamond surface and to stabilize the sp^3 -bonds (diamond). The carbon-hydrogen radicals can then react on the diamond surface, where the C-atom is incorporated into the diamond lattice. The energy needed to crack the process gas molecules into radicals can be supplied by microwave-plasma (MPCVD) or by high temperatures (hot-filament (HF)CVD). In this work the HFCVD process was chosen for diamond growth, where the temperature of the tungsten filaments during growth is above $2000\text{ }^{\circ}\text{C}$. The substrate is positioned approximately 2 cm away from the filaments, which typically results in a substrate temperature of $750\text{ }^{\circ}\text{C}$ to $820\text{ }^{\circ}\text{C}$ [116]. Although CVD diamond was successfully grown at significantly lower temperatures ($T = 400\text{ }^{\circ}\text{C}$ [117]), growth at low temperatures usually results in an increased amount of sp^2 bonded phases in the diamond film [20]. However, in electrochemical applications the sp^2 bonds widely influences the electrode characteristics like its background current and the potential window [19]. Currently, high quality diamond electrodes, thus with a low electrode background current and a large potential window, can only be achieved at high growth temperatures.

Crucial to this work is the growth of doped diamond films. However, doping of diamond is difficult and, presently, there are only few choices like boron (acceptor; $E_A = 0.37\text{ eV}$) and nitrogen (donor; $E_D = 1.7\text{ eV}$) to achieve doped diamond films. Obviously, the activation energies of either doping species are too high for activation at room temperature. However, boron can be incorporated into the diamond lattice in such high concentrations that its activation energy is lowered. Quasi-metallic conduction behavior is obtained at doping concentrations larger than $N_A > 10^{20}\text{ cm}^{-3}$ [20]. Additionally, oxygen-termination of moderately boron-doped diamond (BDD) layers creates a depletion layer at its surface, which might block any currents across the electrolyte/BDD interface [118]. Thus, to allow electron tunneling across the phase boundary (amperometric measurements) a high doping concentration of the BDD electrode is essential. The growth of boron-doped diamond layers in the HFCVD system follows the above described routine, but a boron-containing carrier gas with rather low concentration, in this case trimethyl borate (TMB; $\text{B}(\text{OCH}_3)_3$), is added to the process gas, thereby incorporating boron into the lattice leading to a boron-doped diamond (BDD) film.

Prerequisite for the diamond growth process is the existence of a diamond or a diamond-like surface onto which the growth can be continued. Therefore, methods

to grow diamond onto foreign substrates had been developed, which are related to the creation of diamond nuclei on the substrate surface. One such method is seeding, where diamond seed particles are brought, through mechanical force, onto the surface of a predeposited dielectric film [20, 116]. Then, these seeds can be used as a start layer for the following diamond growth. A second method, and the method used for all grown diamond layers in this work, is bias-enhanced nucleation (BEN). This method mainly relies on two aspects. First, a conductive substrate surface is needed and, second, the substrate surface needs to be a carbide-forming layer [20, 116]. Amorphous silicon deposited by plasma-enhanced CVD (PECVD) had been established as the surface layers, which can form silicon carbide (SiC) and is conductive under diamond growth conditions. The conductive layer on the surface is needed to apply an additional electrical field under which carbon radicals are attracted towards the substrate and bombard the Si surface, where SiC is generated, which is then used as the starting layer for the diamond growth. Compared to seeding, the BEN method will generally lead to more robust layers with superior adhesion properties, because the binding between the diamond film and the Si/SiC layer is based on covalent bonds. As mentioned above, the chosen substrate material was sapphire.

The actual fabrication process started with the deposition of 50 nm silicon nitride (SiN) followed by the deposition of 50 nm amorphous silicon (α -Si) in a plasma-enhanced (PE)CVD system. Then, the sample was put into the HFCVD system and subjected to the BEN process. Subsequently, a 150 nm thick intrinsic diamond buffer layer for backside insulation (to amorphous Si) was grown on top of the whole sample. At this stage the growth process was interrupted to pattern the diamond electrode shape. Outside the electrode area the diamond and the Si-based interlayer were etched down to the sapphire substrate. Diamond etching was achieved by reactive ion etching in an Ar/O₂ plasma (gas flow ratio 2:5 Ar/O₂) at 600 W on a 6 inch substrate holder. Etching of the SiN and α -Si was performed in pure CF₄ plasma in the same chamber with the same power. 300 nm thick aluminum patterned by optical lithography was the etch mask for both processes. The as-prepared sample was then put again into the HFCVD system, where diamond growth was continued with a 150 nm thick boron-doped layer. It was mentioned earlier that diamond growth requires a diamond surface on which the growth process can be continued. Therefore, this growth step resulted in selective growth of the BDD layer on top of the intrinsic diamond layer. On the other hand, diamond growth is a rather isotropic growth mechanism. As a result, the whole material stack as well as its sidewalls were overgrown by BDD, which at this stage was then the only material exposed to air (see figure 5.1). Hence, in an electrode array configuration cross-talking between the individual BDD electrodes is greatly suppressed by exploiting the insulation properties of sapphire [21]. Oxygen termination of the BDD surface is achieved by wet chemical treatment in a H₂SO₄/H₂O₂ solution and by a pure oxygen plasma treatment with low power (100 W on 6-inch substrate holder).

If macroscopic BDD electrodes were fabricated, the fabrication could be finalized with the deposition of the contact metals and the epoxy passivation. However, as will be seen

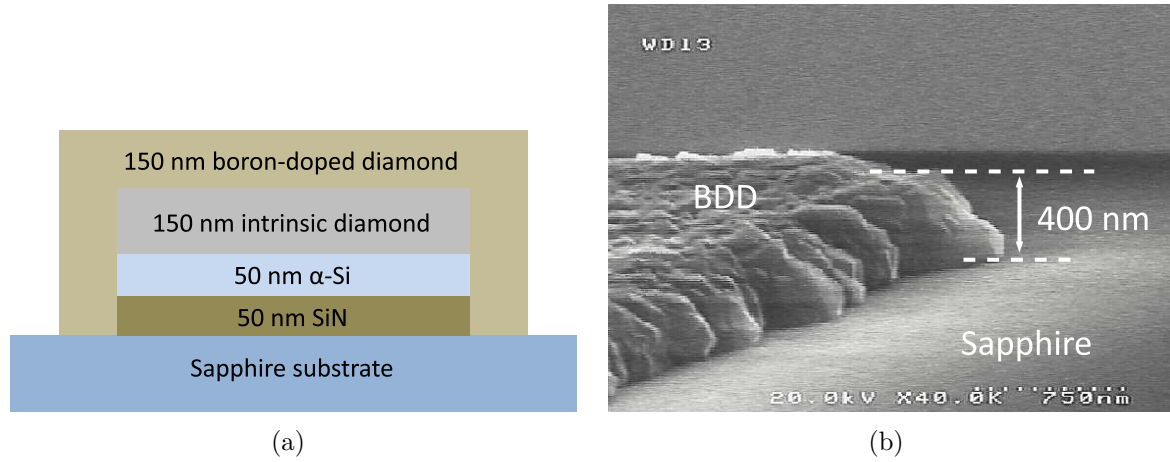


Figure 5.1: (a) Schematic representation of a BDD layer structure, where the BDD diamond was grown around the pre-patterned intrinsic diamond. (b) SEM picture of the edge of a BDD electrode. The BDD covers also the sidewalls and is in contact with the sapphire substrate. The material was grown by Z. Gao and S. Rossi.

later, microelectrode arrays (MEAs) exhibit fast diffusion and offer certain benefits, especially for amperometric measurements [119]. Here, the fabrication of MEAs is linked to an additional growth step of an intrinsic diamond cap layer onto the BDD. However, the intrinsic diamond film should have openings to allow the electrolyte being in direct contact with BDD surface. Such openings are again attained by selective diamond growth. The growth masked used was a Ti/Pt (100/50 nm) metal stack patterned by electron beam lithography and deposited by electron beam evaporation onto the BDD surface (see figure 5.2(a)). If large area, macroscopic electrodes and MEAs shall be produced on the same substrate, the Ti/Pt mask simply needs to be deposited onto the complete surface of the macro electrode. The intrinsic diamond cap layer was grown to a thickness of approximately 150 nm. Theoretically, a very thin cap layer is desired, but at the same time a closed intrinsic diamond film is needed and 150 nm presents a good compromise between both boundary conditions. The growth mask was removed in aqua regia ($\text{HNO}_3 : 3\text{HCl}$). To assure an oxygen terminated BDD surface the wet chemical treatment ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) and the oxygen plasma treatment was repeated. A SEM picture of a single microelectrode with a diameter of 1 μm is shown in figure 5.2(b).

5.2 Sample Preparation and Measurement Setup

The final BDD sensor system is arranged in a 3 by 3 matrix configuration in the center of a $5 \times 5 \text{ mm}^2$ chip (see figure 5.3). Each electrode is connected to Ti/Au (20/200 nm) bond pads positioned around the edge of the chip. For improved adhesion of the metal on the sapphire substrate the sample was subjected to a 30 second long 800 °C annealing step

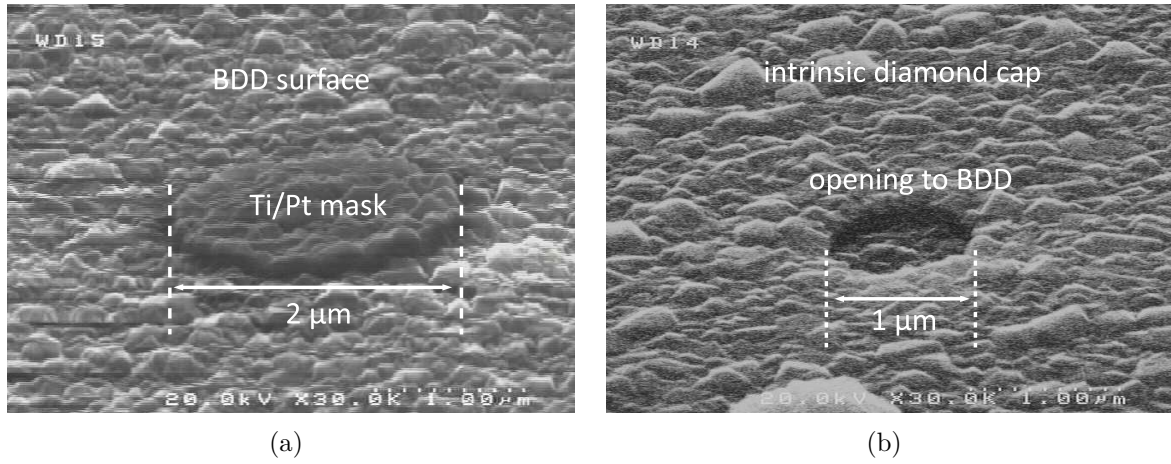


Figure 5.2: SEM pictures of (a) the Ti/Pt growth mask deposited onto the BDD surface and (b) opening in the intrinsic diamond cap layer after removal of the Ti/Pt growth mask (growth by Z. Gao and S. Rossi).

in nitrogen atmosphere. To prevent all metal components from being in contact with the electrolyte a 5 μm thick SU 8 epoxy passivation layer was deposited onto the chip leaving open a $200 \times 200 \mu\text{m}^2$ window on top of each electrode. The BDD electrode array chip was then glued onto a self designed Teflon-based sample holder (figure 5.3(b)). Individual electrodes were connected to the conductor lines on the holder by wire bonding. These thin bond wires were protected using an UV-curing adhesive. Finally, the chip and the sample holder was covered by Teflon adhesive tape.

A detailed micrograph of the nine BDD electrode array is shown in figure 5.3(c). The displayed section corresponds approximately to the opening in the Teflon adhesive tape and therefore presents the part of the chip, which is in direct contact with the electrolyte (the picture was taken before SU 8 passivation). The six electrodes on the left are prepared as microelectrode arrays for enhanced amperometric measurements. The top two MEAs consist of 100 microelectrodes with a diameter of 2 μm, the two MEAs in the middle consist of 400 microelectrodes with a diameter of 1 μm, and the bottom two have 1600 microelectrodes with a diameter of 0.5 μm. This means that the actual active BDD area is kept constant for the different microelectrode arrays and is approximately $314 \mu\text{m}^2$. Thus, the surface coverage, i.e. the ratio between active and passive area, is only around 0.8 %. Simultaneously, the closest distance between two microelectrodes is reduced from 20 μm to 10 μm and 5 μm, respectively, thus being in line with the MEA design recommendation that the separation between two microelectrodes is at least 20 times its radius [119]. The electrodes on the right hand side present macroscopic BDD electrodes, where in case of the top two electrodes the complete surface can be considered active. The lower electrode is completely covered by the intrinsic diamond cap layer and serves as test and calibration structure for this intrinsic diamond layer. As mentioned, there is no SU 8 passivation present in figure 5.3(c). Instead, the two blue rectangles shall exemplarily indicate the position and dimensions of open windows in the

epoxy passivation layer. These $200 \times 200 \mu\text{m}^2$ large openings are identical for all nine electrodes and define the base area of each BDD electrode. In case of the macroscopic electrodes this presents the electrode surface, while in case of MEAs the active surface is given by the openings in the intrinsic cap layer, which, as mentioned above, is only 0.8 % in reference to the large area electrode. This might lead to (at first glance) an underestimation of the performance of MEAs, for instance during the discussion of amperometric measurements (see section 5.4). However, they exhibit other interesting device features still making them the preferred electrode structure.

Electrochemical measurements are performed using a three electrode measurement setup, where all measurements are related to a reference electrode with constant electrode potential (independent of the pH). The three electrodes are the working electrode (BDD), whose electrode/electrolyte phase boundary will be investigated, the Pt counter electrode, which is used to apply a potential to the electrolyte, and the reference electrode (here, saturated calomel electrode SCE). A photograph of the used electrochemical glass cell is presented in figure 5.4(a). A simplified sketch of the measurement setup controlled by a potentiostat is presented in figure 5.4(b). The actual potential is applied through an operational amplifier between the Pt counter electrode and the BDD working electrode. The feedback of the reference electrode assures that the potential at SCE is equal to the applied voltage. The potential at the counter electrode is driven accordingly. Additionally, because of the high input impedance of the operational amplifier it is guaranteed that there is no current flowing through the reference electrode, which could distort the measurement.

The rationale for the use of a three electrode configuration is that, generally, it is not possible to form an Ohmic contact between a solid electrode and an electrolyte. Therefore, the exact potential drop at the investigated BDD/electrolyte phase boundary is unknown and all measurements need to be related to an electrode with constant (reference electrode) or at least predictable electrode potential (pseudo-reference electrode [120]). A reference electrode with defined and constant electrode potential is the standard hydrogen electrode SHE, which, however, is not of practical use. The reference electrode (of second kind) used for all electrochemical measurements in this work is the saturated calomel electrode with a constant electrode potential of $E_0 = +0.24 \text{ V}$ (vs. SHE) (further information on the electrochemical scale are provided in appendix D; see figure D.1).

The electrochemical measurements presented hereafter were conducted on a BDD sensor array prepared according to the above discussed technology. Although, the final goal will be the development of a sensor array consisting of a BDD electrode array integrated with its InAlN/GaN read-out electronics (see chapter 6), the following results present a basic electrochemical characterization of the building block "BDD electrode".

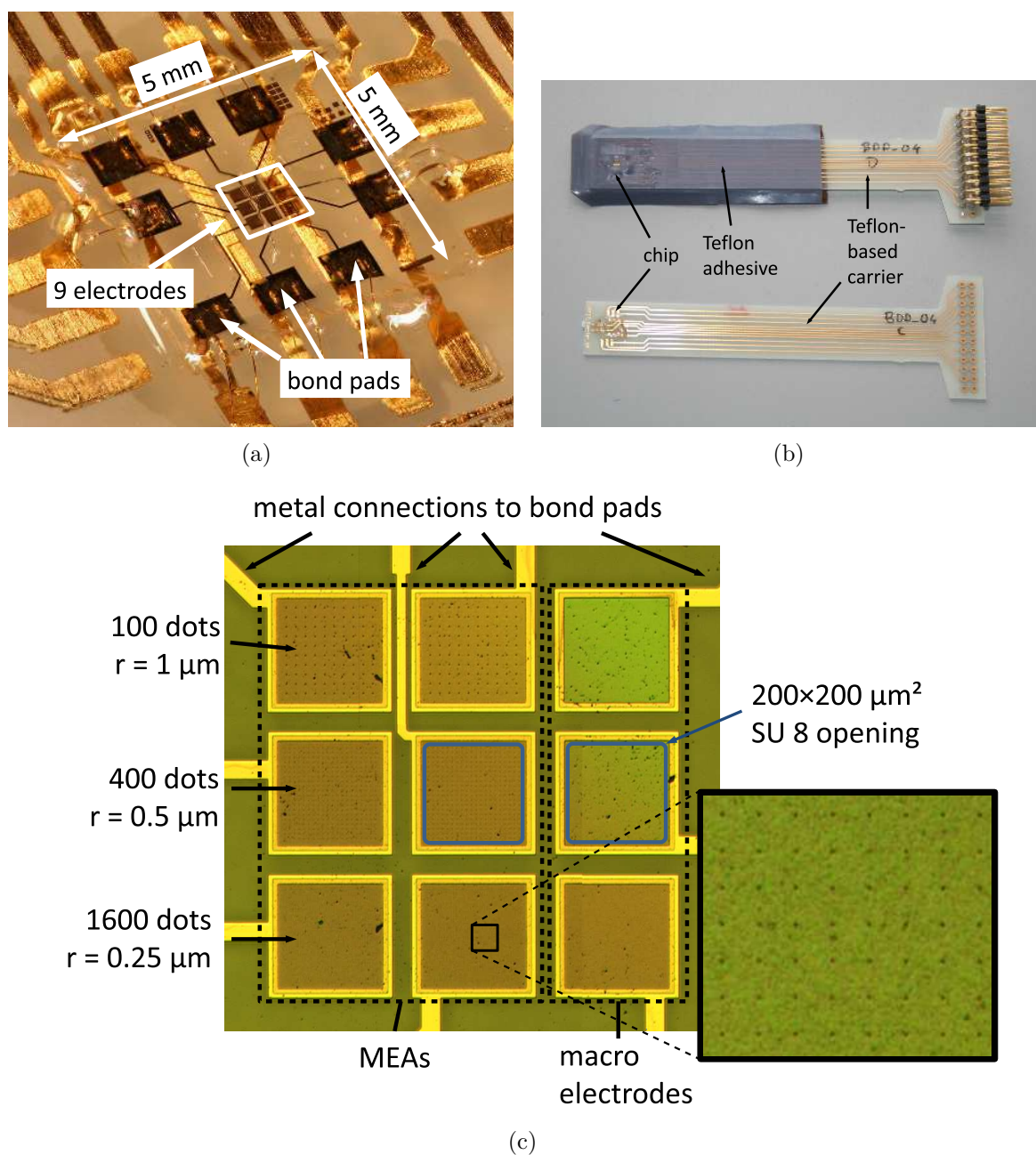


Figure 5.3: Different pictures of the sensor chip prepared for electrochemical measurements. (a) Close-up of the chip glued and bonded on the sample holder. (b) Picture of the Teflon-based sample holder with and without Teflon adhesive tape protection. (c) Microscope picture of the 9 electrodes in the chip center.

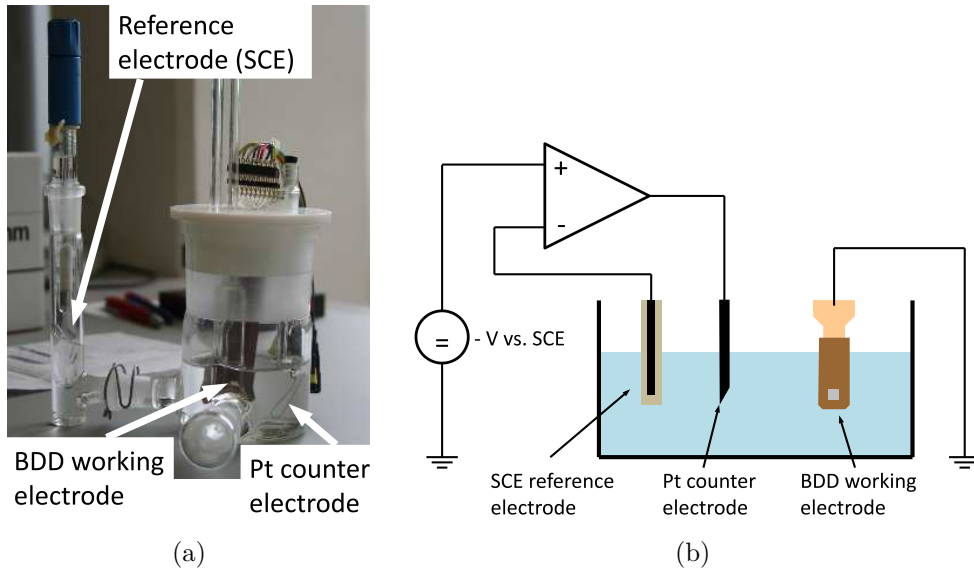


Figure 5.4: Photograph of an electrochemical glass cell (a) and simplified sketch of the three electrode measurement setup (b).

5.3 BDD Electrodes for pH Identification

In the following the BDD electrode shall be introduced as the pH sensitive element ($\text{pH} \propto \text{concentration of } \text{H}_3\text{O}^+ \text{ ions}$) as part of an ISFET, which will be discussed in more detail in chapter 6. Thus, this section shall give a brief and simple explanation of the pH sensitivity, by discussing the BDD/electrolyte phase boundary, and provide some electrochemical characteristics of the BDD electrode, which are used to extract the relevant information for the combination with an InAlN/GaN HEMT to an ISFET. Such information includes, of course, the pH sensitivity, but also the potential window, the background current, and an equivalent circuit model of the BDD/electrolyte interface, which is helpful for design or layout considerations for the combination of BDD electrodes and InAlN/GaN HEMTs. The corresponding measurements were conducted with three different electrolytes, where sulfuric acid (0.1 M H_2SO_4) with $\text{pH} \approx 1$, potassium chloride (0.1 M KCl) with $\text{pH} \approx 5.5$ and potassium hydroxide (0.1 M KOH) with $\text{pH} \approx 13$ were used. However, mainly the characteristics in $\text{pH} = 1$ and $\text{pH} = 13$ solutions will be discussed. For the discussions presented in the following a basic knowledge of electrochemistry is required. Therefore, appendix D provides a more detailed introduction into the field of electrochemistry and explains terms like, e.g. electrolyte, electrode potential, or the pH scale. Also worth mentioning is the fact that all evaluation techniques discussed within this section rely on external electrical fields, which are limited to a range within the potential window of the electrode (except for the determination of the potential window itself). This means that charge transfer between the electrolyte and the electrode is explicitly excluded.

5.3.1 The BDD/Electrolyte Interface

When a semiconductor (here BDD) is brought in contact with an electrolyte, the electrochemical potential μ of the electrolyte and the Fermi level E_F of the semiconductor (which is equivalent to the electrochemical potential of electrons in a solid) will align to each other, similar to the case of pn or Schottky diodes. The electrochemical potential in the liquid combines the energy chemically stored in the electrolyte (chemical potential μ_c) and the electrostatic potential E , which can be applied through an external electrical field. The electrochemical potential is closely related to the Nernst equation (equation (D.7) in appendix D) and can be expressed as [114]

$$\mu = \mu_c + z \cdot F \cdot E, \quad (5.1)$$

with

$$\mu_c \propto \frac{k_b T}{q} \ln(c[H_3O^+]) = 2.303 \frac{k_b T}{q} \times pH, \quad (5.2)$$

where z is the number of charges per ion, $F = 96485$ C/mol is the Faraday constant, $k_b = 1.380 \times 10^{-23}$ J/K is the Boltzmann constant, T the absolute temperature, q the elemental charge, and $c[H_3O^+]$ is the hydronium ion concentration. In essence, this means that the electrochemical potential of the electrolyte is dependent on both, the applied voltage and the ion concentration (= pH) in the liquid.

This is further illustrated by the schematic band diagrams of figure 5.5, where the electrode is in contact with an electrolyte of different compositions (pH = 1 and pH = 13). The BDD electrode is a p-type semiconductor and in equilibrium the electrochemical potential of the liquid and the Fermi energy of the electrode are aligned. To maintain the picture of a pn or Schottky diode, this would correspond to a heavily doped p-type semiconductor (BDD) being in contact with two different n-type materials (e.g. different donor species or concentration in the same material). This would lead to two different positions of the Fermi energy, thus to different expansions of the space charge region or the diffusion layer in the n-type semiconductor. Similar behavior is observed in an electrolyte being in contact with the BDD electrode. However, different electrolyte compositions (different pH) will rather lead to a different charge in the "space charge region" of the liquid (here the double layer composed of Helmholtz and diffusion layer; details in appendix D) causing a pH dependent potential drop at the interface (potentiometric measurements). Thus, the pH sensitivity can be interpreted as a pH dependent capacitance $C = f(pH)$ or as a pH dependent build-in potential $V_{bi} = f(pH)$ at the BDD/electrolyte interface.

However, in electrochemical measurements (without reference electrode) such behavior could be observed on both electrodes, i.e. at the BDD working and at the Pt-counter electrode and therefore would compensate each other. This would mean that the same measurement, conducted in different electrolytic compositions should result in identical curves. The pH sensitivity can only be observed, if the measurement is related to a

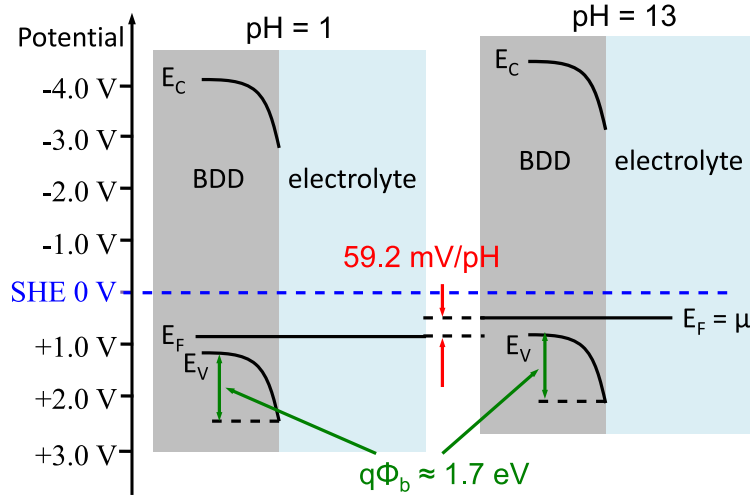


Figure 5.5: Schematic representation of the BDD/electrolyte interface for pH = 1 (left) and pH = 13 (right) in equilibrium. The Fermi level and the electrochemical potential are aligned.

reference electrode (like SHE or SCE) with constant electrode potential. In turn, this points out the importance of the pinned surface ($q\Phi_b \approx 1.7$ eV, slightly depending on the individual surface treatment [113]) offered by Oxygen terminated diamond. Thus, the band bending in the BDD can be considered independent of the pH in the electrolyte and allows for an evaluation of the total barrier height (in reference to SCE or SHE), which according to equation (5.2) changes by 59 mV per pH (at room temperature).

5.3.2 Extraction of the pH Sensitivity

Since it can be interpreted as a pH dependent capacitance, the ideal tool to analyze the pH sensitivity of BDD electrodes are capacitance-voltage measurements. CV measurements are based on the measurement of the complex impedance Z dependent on a DC potential, onto which a small oscillating signal (the oscillation level was $V_{osc} = 30$ mV for all presented CV measurements) is overlaid. Due to the rather slow ionic conduction mechanism in the electrolyte the test frequency is limited to below 10 kHz. Here, 80 Hz and 1000 Hz were chosen as test frequencies. As a result of the measurements one obtains the real part $\Re(Z)$ and imaginary part $\Im(Z)$ of the complex impedance. Nevertheless, one drawback of CV measurements is, that the evaluation of the capacitance is generally limited to a rather simple parallel or series RC equivalent circuit model as presented in figure 5.6(a). However, an equivalent circuit model of the BDD/electrolyte interface should include a parallel $R_{scr}||C_{scr}$ to account for the space charge region in the BDD, a parallel $R_{DL}||C_{DL}$ for the double layer at the interface, and a series resistance R_S for the ionic conduction of the electrolyte (see 5.6(b)). Thus, for an evaluation of CV measurements the following assumptions need to be taken into account:

- The expansion of space charge region in the BDD is independent of the pH.
- The properties of the double layer are independent of the applied potential.
- Without charge transfer across the interface all resistances may be negligible.
- C_{DL} is large compared to C_{scr} . Typically C_{DL} is between $5 \mu F \cdot cm^{-2}$ and $20 \mu F \cdot cm^{-2}$ [118]

These assumptions already allow for further simplification of the circuit to the model (derived below; used for the combination with the HEMT in chapter 6) presented in figure 5.6(c), where $R_{par} \parallel C_{par}$ presents a combination of $R_{scr} \parallel C_{scr}$ and $R_{DL} \parallel C_{DL}$. However, CV analysis is still limited to the model of figure 5.6(a), which is still applicable under the given assumptions. The rationale for this is that a single CV measurement in one electrolyte will mainly trace a modulation of the space charge region in the BDD. The same measurement in an other electrolyte (other pH) should reveal similar information. However, the two curves should experience a constant shift, which is equivalent to the pH sensitivity of the BDD electrode, where the obtained total capacitance presents a combination of a pH dependent C_{DL} and a pH independent C_{scr} .

Depicted in figure 5.7(a) is the capacitance of a large area $200 \times 200 \mu m^2$ BDD electrode calculated using the series and the parallel model of figure 5.6(a). The measurements were conducted in pH = 1 and pH = 13 electrolytes and at test frequencies of 80 Hz and 1000 Hz. Considering only one electrolyte, the calculated capacitance is nearly independent of the chosen frequency and the applied model, which is also an evidence for a strong capacitive dominated behavior of the investigated phase boundary, where parasitic resistances within the potential window seem negligible. The deviations observed at large overpotentials are related to the onset of H_2 or O_2 evolution (explained below), where the assumption of no charge transfer breaks down and the simple models can no longer be applied. Figure 5.7(b) shows the corresponding $1/C^2$ plot ($f = 1000$ Hz, series model). As expected, the resulting CV curves in pH = 1 and pH = 13 are nearly identical, but are shifted by approximately $\Delta V = 0.75$ V, which then results in a nearly ideal pH-sensitivity of 58 mV/pH. However, in the depletion regime the extracted capacitance is in the range of $C \approx 0.5 \mu F \cdot cm^{-2}$ and increases to $C \approx 1.0 \mu F \cdot cm^{-2}$ in accumulation, which is less than expected for heavily doped BDD electrodes [113] and supports the assumption of a boron doping concentration below $N_A = 10^{20} cm^{-3}$. Indeed, an attempt to estimate the boron doping concentration resulted in rather moderate boron doping concentrations of $N_A \approx 2.5 \times 10^{19} cm^{-3}$, which may be found problematic for the investigation of charge transfer reactions (see section 5.4).

The same CV analysis was conducted using the fabricated microelectrode arrays. However, considering that more than 99 % of the surface is presented through the 150 nm thick intrinsic diamond layer, the MEA capacitance is expected to be dominated by the capacitance of this cap layer, making an evaluation, as presented for the large area

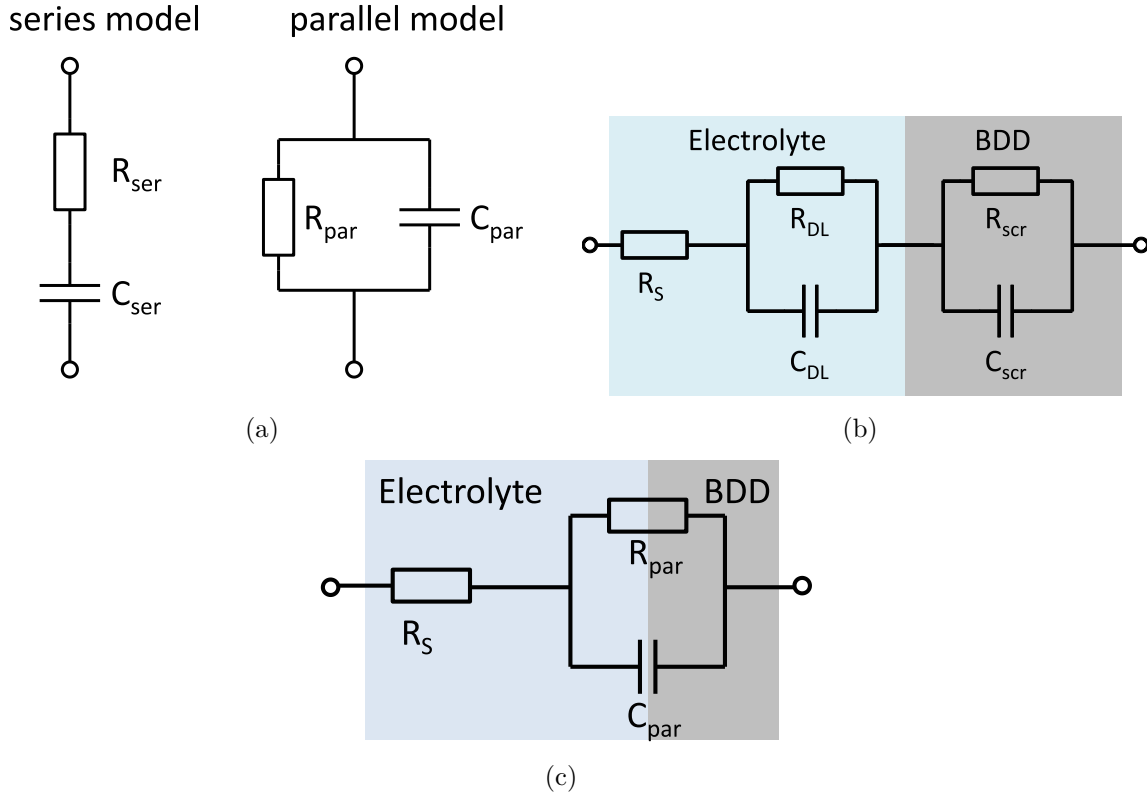


Figure 5.6: (a) Simple series and parallel equivalent circuit model for the evaluation of CV measurements. (b) Equivalent circuit model of the BDD/electrolyte interface taking into account the double layer, the space charge region and the ionic conduction mechanism. (c) Simplified equivalent circuit model of (b) sufficient for modeling, where $R_{par} \parallel C_{par}$ presents a combination of $R_{scr} \parallel C_{scr}$ and $R_{DL} \parallel C_{DL}$.

electrode, very difficult. Within the measurement precision of the used potentiostat the pH sensitivity could not be evaluated by these measurements. Nevertheless, results from CV analysis might be useful for the equivalent circuit modelling (see below). Figure 5.8(a) compares the calculated capacitances of the different MEAs to that of the large area BDD electrode (series model, $f = 1000$ Hz, $pH = 13$). As expected, the resulting MEA capacitances are significantly lower than the capacitance of the macroscopic electrode. However, the calculated capacitances do not remain constant over the investigated potential range. The observed increase of the capacitance at positive potentials could be related to the onset of oxygen evolution, but the increase is sharp and already observed around 0 V, which might be linked a background doping concentration of the intrinsic cap layer. Therefore, additional CV measurements on the all intrinsic diamond control structure were conducted. Figure 5.8(b) compares its resulting capacitance to those of the MEAs and, indeed similar behavior of the MEAs and the intrinsic diamond electrode is observed. Further evaluation of this intrinsic diamond electrode led to a background doping concentration in the range of $N_{A,int} \approx 10^{17} \dots 10^{18} \text{ cm}^{-3}$. Taking into consideration the depletion region only, i.e. the potential regime between -2 V and

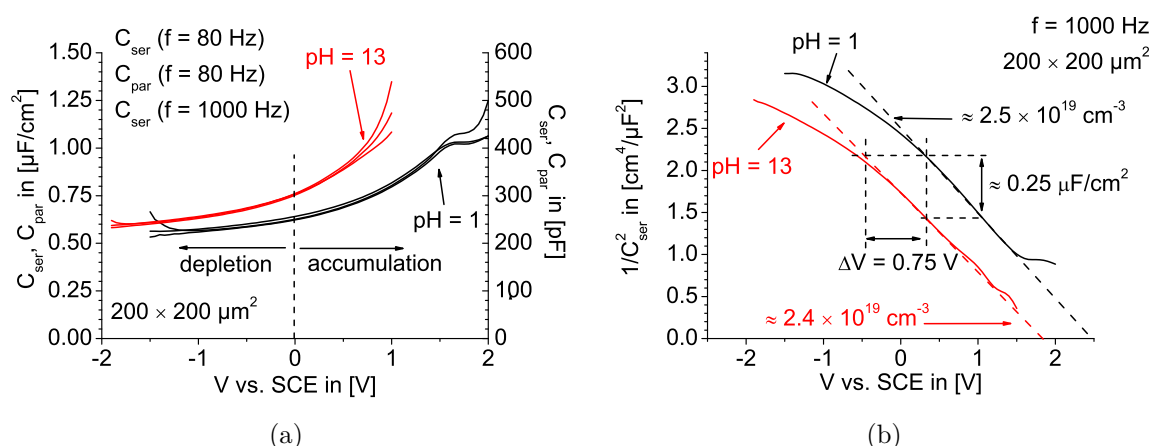


Figure 5.7: (a) Resulting capacitances for different frequencies using the parallel and the series model in pH = 1 and pH = 13. The resulting curves are nearly independent of the model or the frequency. (b) $1/C^2$ plot of the capacitance extracted for $f = 1000 \text{ Hz}$. The offset between pH = 1 and pH = 13 is 0.75 V.

0 V, the capacitances of the different electrode structures remain constant at values of approximately 30 pF to 40 pF. Assuming a relative permittivity for diamond of $\epsilon_r = 5.5$ and a thickness of the intrinsic diamond layer of 150 nm, this is a factor of 3 to 4 higher than expected. This could be correlated to a parasitic depletion layer capacitance of the intrinsic diamond film, where the width of the space charge region would be approximately 50 nm. However, the constant capacitance rather suggests the existence of other parasitic components. Nevertheless, a more elaborate investigation of this phenomenon would require additional experiments and was omitted for this work.

5.3.3 Potential Window and Background Current

Two other important parameters of the BDD electrode, the background current and the potential window, can be extracted from cyclic voltammetry measurements, where the electrode potential is changed between two vertex potentials. The potential change rate during one measurement was constant and presents the important parameter scan rate $s = \frac{dV}{dt}$ (the scan rate is more important for the investigation of charge transfer reactions). At first, the macroscopic large area ($200 \times 200 \mu\text{m}^2$) BDD electrode shall be considered. The results of the cyclic voltammetry in different electrolytes at a scan rate of 50 mV/s are shown in figure 5.9. With the previous considerations of the BDD/electrolyte interface (section 5.3.1) also the electrode potentials of the oxygen and hydrogen evolution are supposed to be shifted by approximately 59 mV per pH. Thus, here a slightly below Nernstian behavior of 47 mV/pH is obtained through this measurement. However, the electrode potentials of the O_2 and H_2 evolution are not strictly defined (here, an electrode current exceeding $\pm 1 \text{ nA}$ was used). The potential window extracted from the

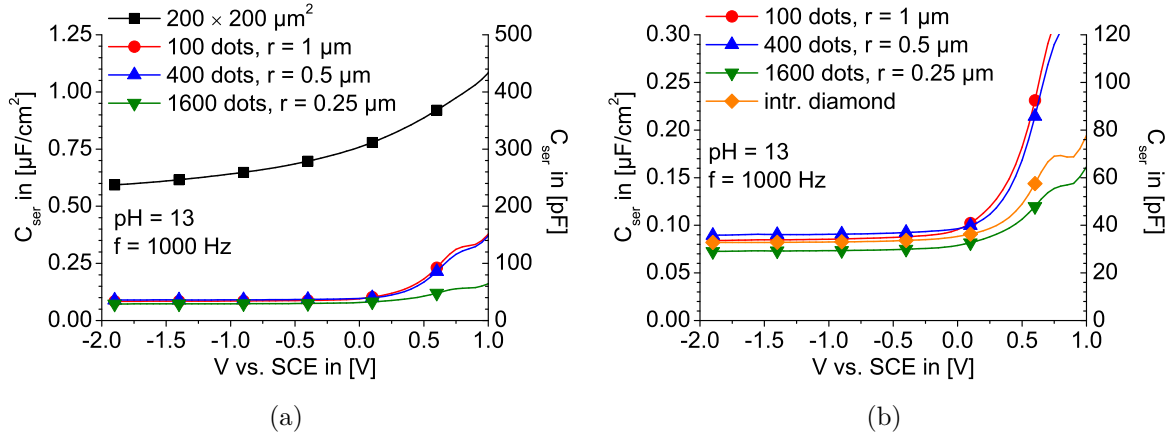


Figure 5.8: (a) Extracted capacitances of different MEAs compared to a large area BDD electrode. (b) Capacitances of the different MEAs compared to an all intrinsic diamond electrode. Measurements were done in pH = 13 electrolyte at $f = 1000$ Hz.

cyclic voltammogram in linear scale (see figure 5.9(a)) is the potential difference between the onset of O_2 and H_2 evolution (= water dissociation). Theoretically, this potential window is $\Delta V = 1.23$ V [114], where values of $\Delta V \approx 1.5$ V are observed in experiments using noble metal electrodes. Here, the extracted potential window (indicated for pH = 1 and pH = 13) is $\Delta V \approx 2.8$ V. This wide observed potential window on diamond electrodes is usually ascribed to a suppressed interaction of molecules in the electrolyte with the diamond surface (suppression of side reactions, which are needed for oxygen or hydrogen generation [6]). This large potential window is of special interest for ISFET applications, since it allows for a wide modulation of the pH dependent output current density (details in chapter 6).

The maximum electrode currents were kept low in order to achieve a high resolution of the electrode background currents. Higher currents could simply be achieved by driving the electrode potential further into the water dissociation regime. The electrode background current can be determined through the cyclic voltammogram in semilogarithmic representation (figure 5.9(b)). However, it can be seen that an exact definition of the background current is also difficult mainly due to a strong dependency of current on the scan direction. In the figure, the scan direction is indicated for the pH = 13 curve (blue arrows) and is the same for the other two curves. Generally, the background current is higher when scanning from inside the potential window towards the O_2 or H_2 evolution and lower when scanning backwards. Therefore, this phenomenon might be related to adsorption and desorption processes on the BDD electrode surface or to capacitive charging effects. Nevertheless, 0.1 nA seems a reasonable value for the BDD electrode background current. An interesting feature of the curves is the different shape of the hydrogen and the oxygen evolution peaks. The slope towards the oxygen evolution is steeper compared to the slope towards the hydrogen evolution. The reason for this is that at H_2 evolution the BDD electrode is biased in reverse direction (depletion) and

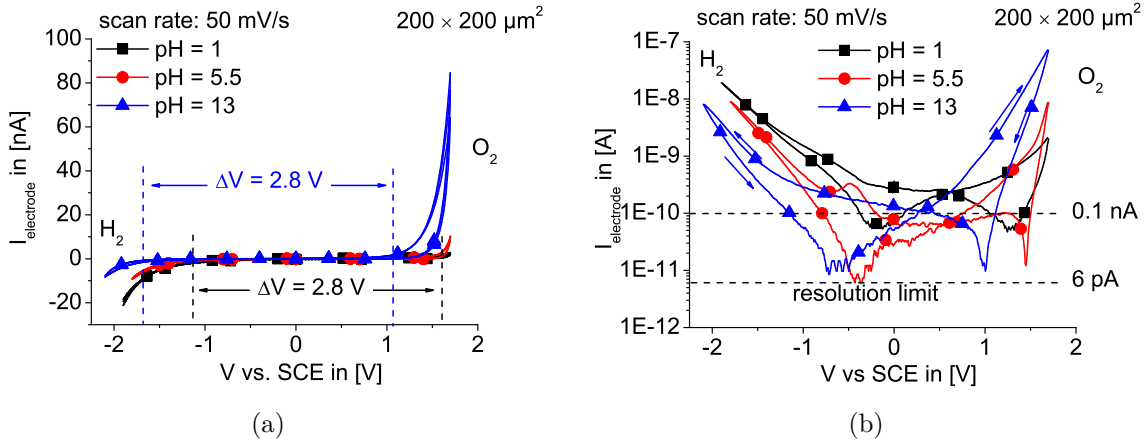


Figure 5.9: Results of cyclic voltammetry measurements of a $200 \times 200 \mu\text{m}^2$ macro BDD electrode in different electrolytes (black squares: pH = 1; red circles: pH = 5.5; blue triangles: pH = 13) in linear (a) and semilogarithmic (b) scale.

it is biased in forward direction (accumulation) at the O_2 evolution. This indicates the existence of a non-negligible tunneling barrier (depletion layer in the BDD electrode) and consequently a boron-doping concentration lower than 10^{20} cm^{-3} , which was already confirmed through CV measurements.

Although, they were mainly designed for their application in amperometric measurements, thus for the analysis of charge transfer reactions involving redox couples, a basic characterization of MEAs in pure electrolytes is essential also for the envisaged combination of BDD electrodes and InAlN/GaN HEMTs. Therefore, figure 5.10 compares the cyclic voltammograms in pH = 1 (0.1 M H_2SO_4) of the three different fabricated MEAs to a large area BDD electrode. In order to obtain comparable conditions the two vertex potentials were kept identical, while keeping the maximum electrode currents small for the four measurements. As expected, in all four cases the onset of oxygen and hydrogen evolution and the overall shape of the curves are comparable. Again, the current peak on the oxygen site is steeper compared to the hydrogen site. Furthermore, the four electrodes behave nearly identical at the O_2 evolution, but very differently at the H_2 evolution, which again seems related to the different electrode biasing conditions ($\text{O}_2 \rightarrow$ forward bias; $\text{H}_2 \rightarrow$ reverse bias). Hence, differences due to the electrode design might be screened in accumulation, but become more prominent in the depletion regime of the diamond electrode. However, the reduction of the electrode current in hydrogen evolution does not compare to the reduction of the active BDD surface (active BDD surface is less than 1 %) and presents already an indication for the efficient diffusion process on MEA structures (see later). Due to the reduced currents the definition of the potential window of MEAs is more difficult. However, with the comparable shape of the individual curves the same potential window as above ($\Delta V = 2.8 \text{ V}$) may be assumed. Of greater interest might be the corresponding cyclic voltammogram in semilogarithmic scale (figure 5.10(b)), since it reveals information on the electrode background currents,

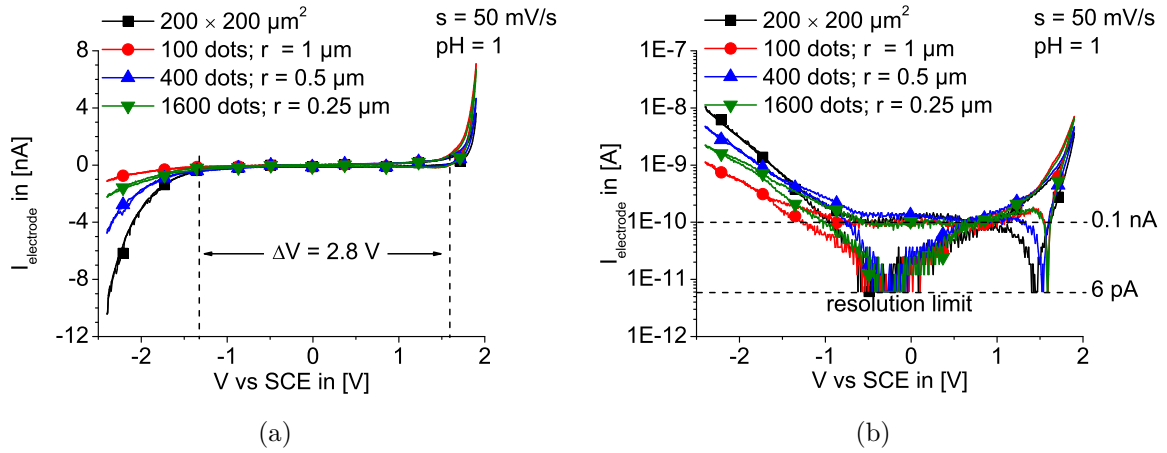


Figure 5.10: Cyclic voltammetry measurements of different BDD electrodes in pH = 1 (0.1 M H_2SO_4) in linear (a) and semilogarithmic (b) scale.

which are expected to be reduced with the reduced active area. Surprisingly, the electrode background current is again in the range of 0.1 nA independent of the individual electrode design. However, this findings shall not generally exclude a dependency of the background current on the electrode dimensions or design, but rather point out the importance of the crystalline quality of the nano-diamond film (amount of sp^2 bonds) on this parameter [19, 20]. Similar surface modifications on single crystalline BDD electrodes already led to a significant reduction of the background current [121].

5.3.4 Equivalent Circuit Model of the BDD/Electrolyte Interface

As mentioned before, the identification of an equivalent circuit model of the BDD/electrolyte interface is useful for design considerations when combining BDD electrodes and InAlN/GaN HEMTs to ISFETs. The equivalent circuit of the BDD/electrolyte phase boundary (that of the HEMT will be given in chapter 6) was already predicted in section 5.3.2 in figure 5.6(b). However, simple CV measurements cannot provide information on the individual components of such "complex" networks. A measurement technique for the analysis of more complex networks is the impedance spectroscopy with electrochemical background. In contrast to CV measurements the complex impedance is measured as a function of frequency, but at a fixed DC potential. From the measured frequency response the determining components of the equivalent circuit model can be derived, where their respective values are obtained by a numerical simulation tool specifically adapted for electrochemical behavior (here, ZSimpWin from Princeton Applied Research). Nevertheless, a variety of different circuits, also including different circuit elements, can produce similar or equal measurement results. Additionally, different circuit elements can only be identified, if their influence can be resolved within the measured spectrum. Thus, also in this case a careful prediction of the underlying network is indispensable

for a quantitative interpretation of the measurement results. It is worth remembering again that for this discussion charge transfer reactions will not be considered (explicitly excluded), which means that the derived quantities of the individual components and also the introduced simplifications are only applicable to potentiometric measurements within the potential window. The investigation of charge transfer reactions using electrochemical impedance spectroscopy would be based on the equivalent model of figure 5.6(b) or may involve additional elements [113]. Then, this would lead to other quantities of the components, thus to other simplifications. Such analysis was omitted in this work.

As mentioned before, the inert BDD/electrolyte interface can be modeled by an parallel $R_{\text{scr}} \parallel C_{\text{scr}}$ circuit for the depletion region at the BDD surface in series to another parallel $R_{\text{DL}} \parallel C_{\text{DL}}$ circuit for the double layer in the electrolyte. An additional series resistance R_{S} presents the access resistances, i.e. the resistance through the BDD volume to the bond pads as well as the resistance of the electrolyte (compare figure 5.6(b)). However, the background currents in the potential window were in the range of 0.1 nA or below, resulting in an overall parallel resistances of the interface in the $\text{G}\Omega$ regime. In addition, typical values of the double layer capacitance are above $5 \mu\text{F} \cdot \text{cm}^{-2}$ [118], which is significantly larger than the previously extracted C_{scr} (CV measurements). This means that the additional impedance generated by C_{DL} is much smaller than that of the depletion layer in the BDD, which allows to simplify the circuit model of the phase boundary to the model already presented above in figure 5.6(c), where the $C_{\text{par}} \parallel R_{\text{par}}$ circuit presents a combination of the double layer and the space charge region. Then, this simplified model gives an indication of the overall behavior of the BDD electrode, which is only applicable under certain boundary conditions (absence of charge transfer, potentials within the potential window). This model may be inadequate to analyze the electrochemical process, but is useful to combine the electrode with the InAlN/GaN HEMT input, where additional components of the HEMT will have to be considered (see chapter 6), and therefore may be sufficient for this work.

The frequency response of the large area BDD electrode is shown in figure 5.11 by Bode plot representation. The corresponding measurements were conducted in $\text{pH} = 1$ electrolyte at four different DC potentials of $V_{\text{DC}} = -0.6 \text{ V}$, -0.3 V (not shown), $+0.3 \text{ V}$, and $+0.6 \text{ V}$ (not shown) and therefore lie inside the potential window. As mentioned earlier, the test frequency range is limited to below 10 kHz. Assuming the simplified circuit model of figure 5.6(c) it can be stated that at high frequencies the parallel capacitance C_{par} presents a short circuit and the total impedance is presented by the series access resistances R_{S} . On the other hand, in the quasi-static case at low frequencies this capacitance presents an open circuit and its parallel resistance R_{par} is dominating the impedance. Therefore R_{S} and R_{par} can be estimated from the Bode magnitude plot (figure 5.11(a)) at very high and very low frequencies, respectively. However, the influence of R_{par} cannot be observed in the Bode magnitude plot (no plateau at low frequencies), but becomes visible in the phase diagram (figure 5.11(b)), where the phase angle ϕ is reduced for lower frequencies. Then, this can be used to extrapolate the value

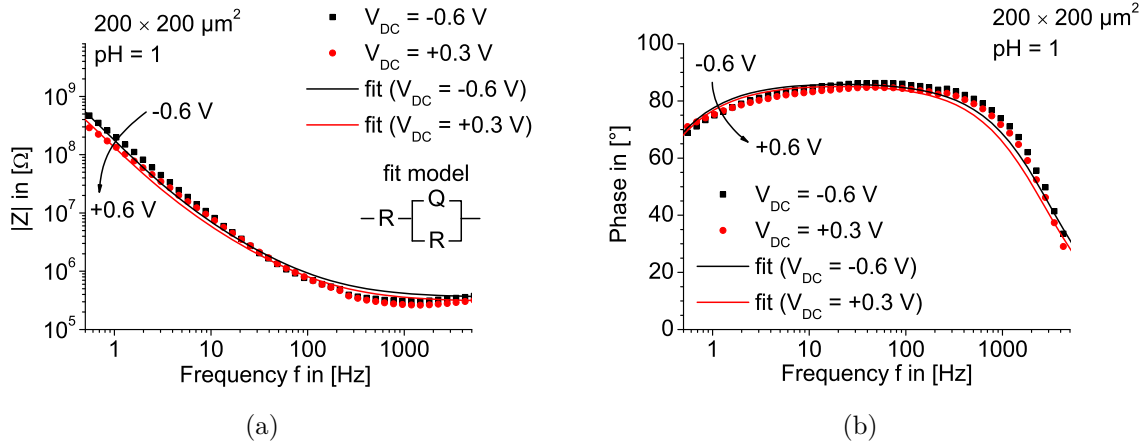


Figure 5.11: Results of impedance spectroscopy depicted in (a) Bode magnitude and (b) Bode phase diagram. The measurements were done in pH = 1 electrolyte. Depicted are the results of measurements together with their fitted curves at $V_{DC} = -0.6$ V (black squares, black line) and at $V_{DC} = +0.3$ V (red circles, red line).

of R_{par} . However, a close look to the two diagrams also reveals that a constant decay of approximately -11 dB/dec (instead of -10 dB/dec) is observed for the magnitude of the impedance and that the phase angle does not approach 90° . This non-ideal behavior is assigned to a non-ideal capacitor due to the surface roughness of the BDD electrode and can be taken into account by a constant phase element (CPE; symbol: Q). The impedance of such a Q -element is calculated by [122]

$$Z_Q = \frac{1}{(j \cdot \omega)^n \cdot Q}, \quad (5.3)$$

where ω is the angular frequency and $n = 0 \dots 1$ an ideality factor. For $n = 1$, this element corresponds to an ideal capacitor, where $C = Q$ is the value of the capacitance. For $n = 0$ the element presents an ideal resistor with $R = 1/Q$ being the value of the resistance. In this experiment the ideality factor is $n \approx 0.97$ for a DC potential of $V_{DS} = -0.6$ V and increases to $n \approx 0.99$ at $V_{DS} = +0.6$ V indicating a nearly ideal capacitor. Nevertheless, curve fitting was done assuming a constant phase element instead of an ideal capacitor. The measured data and the presented fits agree very well over the whole investigated frequency regime, which is also consistent with findings from CV analysis. Since only one time constant can be identified in the Bode diagram, numerical fitting using the more complex equivalent circuit model of figure 5.6(b) may not result in a higher accuracy of the fit. However, an attempt to apply this model resulted in similar values for the access resistance R_s and the depletion layer could be identified with C_{par} and R_{par} , but generated very diverse values for the double layer capacitance C_{DL} and resistance R_{DL} . Therefore, only the simplified model shall be considered in the following.

A detailed evaluation of the individual components R_S , R_{par} , and C_{par} dependent on the DC electrode potential and the pH value is given in figure 5.12. To simplify the evaluation and for simpler comparisons to CV measurements the constant phase element shall be treated like a capacitance with unit [F]. The series access resistance R_S mainly presents the resistance of the electrolyte and can be estimated with a rather high accuracy, because its influence can be observed over a wide frequency range. At $V_{\text{DS}} = -0.6$ V its normalized value ($R_S \times A$, with $A = 0.0004 \text{ cm}^2$) is $R_S = 144 \Omega \cdot \text{cm}^2$ and decreases linearly by $\Delta R_S = 24 \Omega \cdot \text{cm}^2/\text{V}$ to $R_S = 112 \Omega \cdot \text{cm}^2$ at $+0.6$ V. Therefore it seems justified to assume that the double layer resistance R_{DL} is partially reflected in R_S . A constant offset of $16 \Omega \cdot \text{cm}^2$ is observed between $\text{pH} = 1$ and $\text{pH} = 13$ electrolyte. However, this seems a property of the ionic conduction mechanism in the different solutions and does not reflect a pH sensitivity in the usual sense. Considering that mainly the H_3O^+ ($\text{pH} = 1$) or the OH^- ($\text{pH} = 13$) ions contribute to the electrolytic conduction this may be ascribed to different diffusion coefficients or ion mobilities of the two species. In contrast to R_S , the estimation of the parallel resistance R_{par} is based on the extrapolation to frequencies below 0.5 Hz, which cannot easily be measured. Therefore, the presented values of R_{par} (see figure 5.12(b)) inherit larger uncertainties. Nevertheless, all extracted R_{par} (as a combination of the depletion and the double layer) are above $2 \text{ G}\Omega$ as also expected from cyclic voltammetry. For more positive DC potentials the BDD electrode is driven in accumulation, thereby reducing the width of the space charge region (tunneling distance) and consequently the value of the parallel resistance. Also, a significant reduction of R_{par} from $\text{pH} = 1$ to $\text{pH} = 13$ is observed, which, in this case, certainly is linked to a pH sensitivity due to a changed total barrier height. Figure 5.12(c) compares C_{scr} extracted by CV measurements to those obtained by impedance spectroscopy (Q_{par}). Although the extracted values are in good agreement, impedance spectroscopy generally leads to approximately 10 pF higher values, which is probably linked to the assumption of C_{scr} being an ideal capacitor in the CV analysis. However, within the investigated range the difference is constant, thereby also confirming the previously calculated doping concentration of $N_A = 2.5 \times 10^{19} \text{ cm}^{-3}$. With the observed tendencies the values of the individual components R_S , R_{par} and C_{par} can be predicted for any electrode potential, as long as the applied potential lies within the potential window of the BDD electrode. As will be explained in chapter 6, the FET input has to match such values, which also triggered the development of the GOS MISHEMT technology.

The equivalent circuit model of the fabricated microelectrode arrays is derived on the basis of the model for large area BDD electrodes. The proposed circuit model is depicted in figure 5.13, where the simplified model of the macroscopic electrode is applied for an individual microelectrode. This means that inside the opening of the cap layer again a $C_{\text{par}} \parallel R_{\text{par}}$ circuit presents the combination of $C_{\text{DL}} \parallel R_{\text{DL}}$ and $C_{\text{scr}} \parallel R_{\text{scr}}$. The intrinsic cap itself is considered as a capacitor C_{cap} in parallel to the opening. However, CV analysis revealed that the intrinsic diamond comes with a boron background doping concentration of up to $N_A = 10^{18} \text{ cm}^{-3}$ and that at positive electrode potentials the MEAs approach the behavior of a macroscopic BDD electrode. Thus, an evaluation

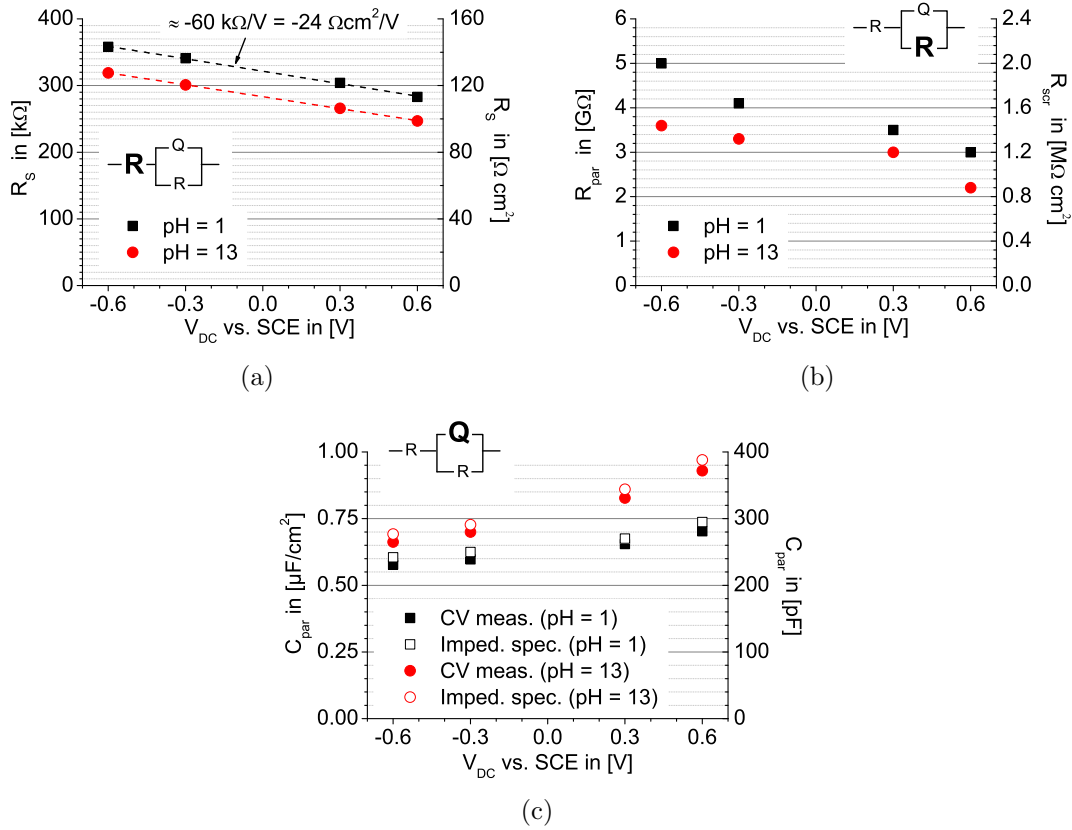


Figure 5.12: Values of R_s (a), R_{par} (b), and C_{par} (c) extracted by numerical fitting of impedance spectroscopy at different potentials in pH = 1 (black square) and pH = 13 (red circles). The extracted C_{par} are also compared to the values obtained by CV analysis.

of microelectrode arrays by impedance spectroscopy is limited to negative electrode potentials. Furthermore, in this potential regime the extracted capacitance is dominated by parasitic capacitances. As a consequence, here the value of C_{cap} will be identified with this parasitic capacitance.

The Bode magnitude and phase diagram of the different MEAs compared to the large area electrode are depicted in figure 5.14(a) and 5.14(b), respectively. The measurements were conducted at a DC potential of $V_{DC} = -0.6 \text{ V}$ in pH = 1 electrolyte. Since the active BDD area is kept constant for all MEAs, their respective frequency responses are expected to be identical. Indeed, the obtained data show a very good agreement over a wide frequency range. Only for frequencies below 10 Hz a deviation of the curves can be identified in the phase diagram, which is probably linked to a very high parallel resistance and therefore to measurement inaccuracies. For very high and low frequencies the magnitude curves of the MEAs seem parallel shifted, i.e. compared to the large area electrode shifted towards higher impedances. Indeed, a decay of approximately

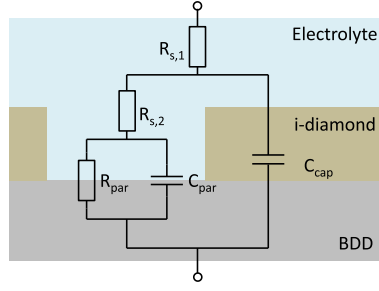


Figure 5.13: Proposed equivalent circuit model of the microelectrode array. The opening itself is modeled by the circuit derived for large area electrodes and is complemented with a parallel capacitor presenting the intrinsic cap.

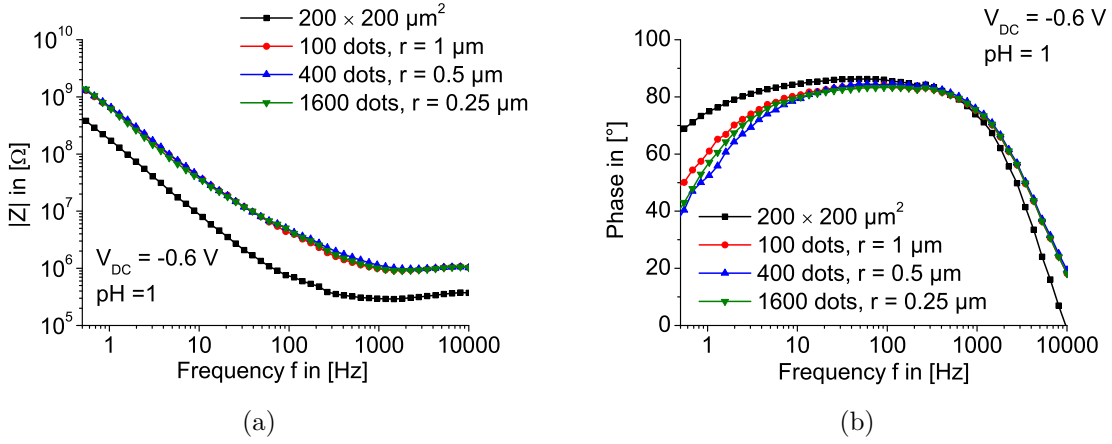


Figure 5.14: (a) Bode magnitude and (b) Bode phase diagram of the three different MEAs compared to the macroscopic BDD electrode recorded at $V_{DC} = -0.6$ V.

-11 dB/dec is also observed for the MEAs up to frequencies of $f \approx 20$ Hz. Afterwards, a significantly lower decay in the range of -8 dB/dec can be extrapolated up to 1000 Hz. Therefore, the assumption of an additional time constant given by C_{cap} and $R_{s,1}$, as proposed by the model of figure 5.13, seems justified.

Fairly good results are obtained by numerical curve fitting, where, as expected, the overall quantities seem mainly dominated by the cap layer. As an example, the obtained values for the different components of the MEA with 400 openings are summarized in table 5.1 for measurements at a DC potential of $V_{DC} = -0.6$ V in $pH = 1$ electrolyte. As indicated in the Bode diagram, similar results are obtained for the MEAs with 100 and 1600 openings. Although it is larger than determined through CV analysis, the capacitance of the intrinsic diamond cap is $C_{cap} = 39$ pF. From simple downscaling considerations a parallel resistance R_{par} (here, also combined depletion and double layer) in the range of several hundred G Ω could be expected. However, the background current of the different MEAs and the large area electrode were in the same range (≈ 0.1 nA, compare figure 5.10) correlating to only few G Ω , as extracted in both cases. With the

| $R_{S,1}$ | $R_{S,2}$ | C_{cap} | R_{par} | C_{par} |
|----------------|---------------|-----------|---------------|-----------|
| 1.0 M Ω | 25 M Ω | 39 pF | 12 G Ω | 6.9 pF |

Table 5.1: Values of the individual circuit components (figure 5.13) obtained by numerical fitting of the measured frequency response of a microelectrode array. The measurement conditions were: pH = 1; $V_{DC} = -0.6$ V.

same considerations a depletion layer capacitance of approximately 2 pF was expected, while a value 3 to 4 times larger was obtained by curve fitting. Although this is in good agreement with expectations, nearly identical values could be obtained by fitting measurements at other negative potentials or in other electrolytes strongly suggesting that the frequency response of MEAs with the given design are mainly dominated by parasitic components, which were not yet identified. Therefore, the pH sensitivity of the MEAs did reflect on the values of the individual circuit components, which is the reason why an evaluation as presented for the macroscopic electrode (compare figure 5.12) was omitted. It shall be noted that the capacitors were modeled as ideal capacitors. Using a CPE instead of either capacitor did not significantly influence the results indicating that the dominating parasitics present ideal capacitors.

5.4 Detection of Redox Reactions with BDD Electrodes

The investigations of charge transfer reactions involving a redox system shall be limited to negative electrode potentials, where the influence of the background doping concentration of the intrinsic cap layer can be neglected. This means that only redox couples with negative redox potentials will be investigated. Such a redox system with a negative redox potential is the $Ru(NH_3)_6^{2+/3+}$ redox system. For the sake of simplicity this analysis shall further be limited to the investigation of the reduction peak by only dissolving oxidized species in the electrolyte. This brings the advantage of having rather precise control over the concentration dissolved in the electrolyte. The prepared electrolyte was 1 mMol $Ru(NH_3)_6^{3+}$ dissolved in 0.1 Mol KCl solution. A complete electrochemical characterization of charge transfer reactions could comprise cyclic voltammetry, capacitance voltage analysis, and impedance spectroscopy. Impedance spectroscopy may be of particular interest for electrochemical analysis, because it can allow an investigation of redox signals with higher resolution. However, it would require a model of the electrode/electrolyte phase boundary specifically adapted for the investigation of charge transfer, which would lead beyond the scope of this work. In this work, where the final goal is to use the FET as switch to turn on and off the redox reaction, the evaluation shall be limited to the analysis of IV characteristics resulting from cyclic voltammetry.

The cyclic voltammograms obtained from the different electrode structures are shown in figure 5.15, where figure 5.15(a) shows the measurements at a scan rate of $s = 50$ mV/s and figure 5.15(b) those at a scan rate of $s = 200$ mV/s. Independent of the electrode structure or the scan rate the onset of the reduction reaction occurs at an electrode potential of approximately -0.15 V (vs. SCE). This potential is a parameter of the investigated redox system and is correlated to its standard electrode potential E_0 or redox potential. The sharp increase of the electrode current then follows the exponential relation described by the Butler-Volmer equation (equation (5.4)), where the current is limited by the reaction kinetics. The Butler-Volmer equation is given by [115]

$$j = j_0 \left[\exp \left(\frac{\alpha z F}{R_g T} (V - V_0) \right) - \exp \left(-\frac{(1 - \alpha) z F}{R_g T} (V - V_0) \right) \right], \quad (5.4)$$

where j_0 is the exchange current density at equilibrium, $\alpha = 0 \dots 1$ the anodic transfer coefficient, z the number of transferred electrons, $F = 96485$ C/mol the Faraday constant, $R_g = 8.314 \frac{\text{J}}{\text{mol} \cdot \text{K}}$ the universal gas constant, T the absolute temperature, and V_0 is the equilibrium potential of the reaction, where the net current density is zero. At a certain electrode potential (here around $V \approx -0.35$ V) a further increase of the electrode potential does not result in a larger electrode current. In this regime the current is limited by diffusion. Here, the reduction reaction is investigated and the total current is limited by the time dependent concentration profile of oxidized species in the electrolyte. Thus, the limitation is based on the diffusion of reduced species away from and of oxidized species towards the active BDD surface. Diffusion on MEA structures results in a fast, three-dimensional hemispherical pattern, whereas in case of planar electrodes it is a one-dimensional linear diffusion process. The corresponding diffusion limited current densities are calculated by

$$j = z F c_b \cdot \sqrt{\frac{D}{\pi t}} \quad (5.5)$$

for large area electrodes [114] and by

$$j = \frac{4\pi c_b F D r^2}{4t_{\text{cap}} + \pi r} \quad (5.6)$$

for a single (recessed) microelectrode as fabricated in this work [123]. In these equations c_b is the bulk concentration of the $\text{Ru}(\text{NH}_3)_6^{3+}$ molecules at the start of the experiment (at $t = 0$) and $D = 6.0 \times 10^{-6}$ cm²/s the diffusion constant [124]. $t_{\text{cap}} = 150$ nm is the thickness of the intrinsic diamond cap layer and r is the radius of the microelectrode.

Generally, the total electrode current of a MEA is around half of the planar electrode. However, keeping in mind that less than 1 % of the MEA surface is open to the BDD layer, this compares to a very high current density of the active BDD in a MEA structure. Although this might be interesting, MEAs exhibit other important features making them extremely attractive for applications. In accordance to equations (5.5) and (5.6) a significant time dependence, thus scan rate dependence, is obtained for the

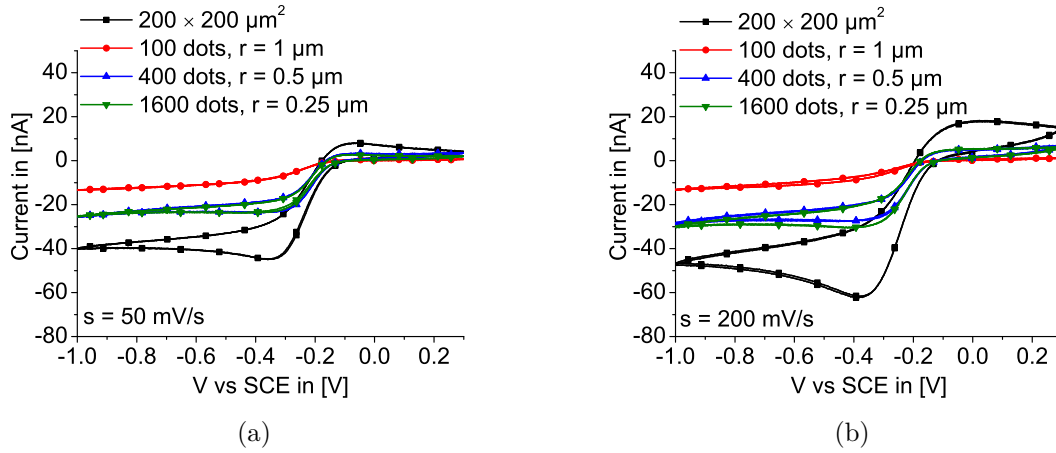


Figure 5.15: Comparisons of cyclic voltammograms for the reduction of 1 mMol $\text{Ru}(\text{NH}_3)_6^{3+}$ using different BDD electrode structures at a scan rate of $s = 50 \text{ mV/s}$ (a) and $s = 200 \text{ mV/s}$ (b).

planar electrodes, which is reduced or nearly vanished for the MEAs (compare also figure 5.16(a)). Furthermore, the rather slow linear diffusion on planar electrodes leads to the evolution of current peaks, whereas the fast hemispherical diffusion on MEAs may lead to the evolution of current plateaus [123]. Those improved characteristics of MEAs make them especially attractive for advanced electrochemical applications.

The extracted peak currents of the $200 \times 200 \mu\text{m}^2$ electrode, obtained at $V \approx -0.35 \text{ V}$, are $I_{\text{max}} = -44.5 \text{ nA}$ and $I_{\text{max}} = -62.3 \text{ nA}$ for scan rates of 50 mV/s and 200 mV/s , respectively. Thus, the expected dependency of $I_{\text{max}} \propto 1/\sqrt{t}$ could not be attained in this experiment. However, with a diffusion constant of $D = 6.0 \times 10^{-6} \text{ cm}^2/\text{s}$ and using 4 s and 1 s in equation (5.5) (correlated to the scan rate of 50 mV/s and 200 mV/s with $\Delta V \approx -0.35 \text{ V} + 0.15 \text{ V} = 0.2 \text{ V}$) results in calculated peak electrode currents of $I_{\text{max}} = -26.6 \text{ nA}$ and $I_{\text{max}} = -53.3 \text{ nA}$. Such a deviation may be explained by a slightly larger concentration of $\text{Ru}(\text{NH}_3)_6^{3+}$ molecules of $c_b = 0.0017 \text{ mol/l}$ instead of $c_b = 0.001 \text{ mol/l}$ in the electrolyte.

The diffusion limited currents of the three different MEA structures at $s = 50 \text{ mV/s}$ were calculated using a bulk concentration of $c_b = 0.001 \text{ mol/l}$ in equation (5.6). This resulted in currents of $I_{\text{max}} = -19.5 \text{ nA}$, $I_{\text{max}} = -33.6 \text{ nA}$, and even $I_{\text{max}} = -52.7 \text{ nA}$ for the MEA with 100 dots with $r = 1 \mu\text{m}$, 400 dots with $r = 0.5 \mu\text{m}$, and 1600 dots with $r = 0.25 \mu\text{m}$, respectively. At a scan rate of 200 mV/s the electrode current theoretically increases by 0.2 nA and therefore is negligible. The obtained I_{max} (calculated and extracted from figure 5.15) for the different MEAs at the two scan rates are summarized in figure 5.16(a). The agreement between measurements and calculation is fairly good, especially for the MEAs consisting of 100 and 400 microelectrodes, and the trend of increasing current density with decreasing radius of an individual microelectrode is confirmed. However, the largest deviation from calculation (close to 45 %) is obtained

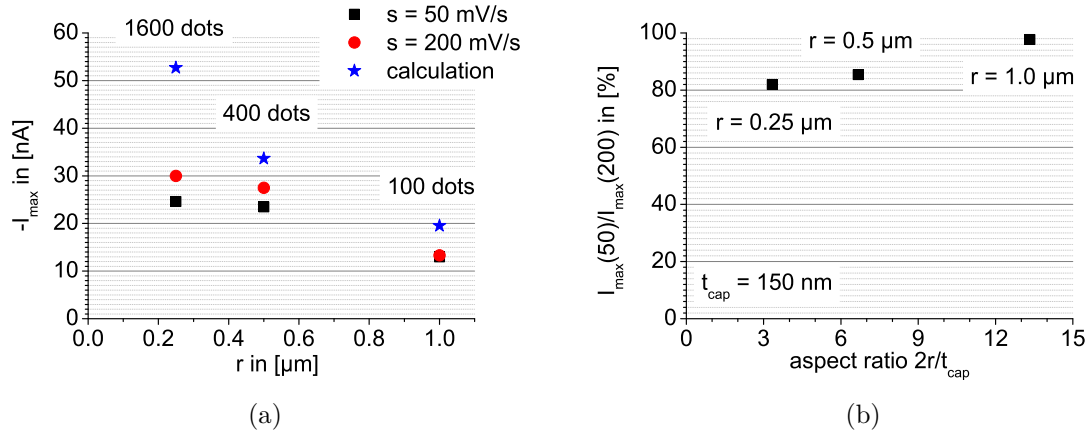


Figure 5.16: a) Change of I_{\max} with the microelectrode radius r , where the active electrode surface is constant. (b) Change of the ratio $I_{\max}(s = 50 \text{ mV/s})/I_{\max}(s = 200 \text{ mV/s})$ with aspect ratio $2r/t_{\text{cap}}$.

from the MEA with $r = 0.25 \mu\text{m}$. Similar behavior is observed for the measured scan rate dependence, when calculating the ratio $I_{\max}(s = 50 \text{ mV/s})/I_{\max}(s = 200 \text{ mV/s})$. This ratio decreases from approximately 98 % to 85 % and 82 % with decreasing electrode radius. Although the influences of the scan rate is not vanishing (apart from the $1 \mu\text{m}$ electrode) it is significantly reduced compared to the planar electrode. A possible explanation for both phenomena might be the reduction of the aspect ratio given by the electrode diameter and the intrinsic diamond layer thickness $2r/t_{\text{cap}}$ (see figure 5.16(b)). As a consequence of the reduced aspect ratio an additional linear diffusion path could form inside the cavity of a single microelectrode, which then would generate again the dependencies of a planar electrode, but on a microscopic scale. Then, this problem could be solved by shrinking the thickness of the diamond cap layer. However, if further downscaling of the microelectrode diameter is envisaged the problem would arise again. A probably more elaborate way to address this issue might be the introduction of an additional selective BDD growth process. In this additional growth process the active BDD layer could be grown to a thickness ideally slightly exceeding the cap layer thickness. The resulting microelectrode structure could then exhibit further improved diffusion, enhanced current densities and further reduced scan rate dependence [119].

6 Combining InAlN/GaN HEMTs and BDD Electrodes for Electrochemical Sensing Applications

Since they offer the possibility of high integration density and miniaturization, modern electrochemical sensor systems are usually based on solid state devices. Today, such devices are usually realized in Si and are compatible to standard CMOS technology [125], which consequently enabled the development highly integrated sensor systems consisting of ISFET sensor arrays for pH tracking, electrode arrays for current monitoring, and all relevant circuitry for signal amplification or temperature drift compensation [126, 127, 128, 129, 130]. Such smart sensor systems were already demonstrated for the measurement of neuron cell activities with high spatial resolution [131] and also for DNA sequencing of bacterial genome [132]. One key enabling the compatibility to CMOS technology was the implementation of ISFETs as "extended gate" ISFETs onto the CMOS circuitry and, today, this presents a standard ISFET design. This means that a separate, remote, pH sensitive electrode (often tantalum oxide Ta_2O_5 or titanium nitride TiN) is connected to the gate of the FET, where only the electrode is in contact with the liquid. One advantage of the extended gate ISFET structure is that the actual FET can be optimized for high performance by taking advantage of common FET scaling (e.g. gate length reduction). However, to achieve best performance such a structure requires a careful design of the individual components (e.g. matched impedances [131, 133]).

The relatively low corrosion resistance of the used electrode materials limits the application of such sensor systems to rather mild media (commonly $\text{pH} = 4$ to $\text{pH} = 10$). To access more aggressive environments, e.g. $\text{pH} = 1$ or $\text{pH} = 13$, a more robust electrode material is desired. Thus, the chemically inert diamond presents the ideal electrode material, which, as BDD electrode, additionally allows amperometric and potentiometric measurements with the same electrode. However, the available diamond electronics does not satisfy the specific requirements of integrated sensor systems and standard CMOS technology is not compatible with diamond growth of electrochemical grade. Therefore, the BDD electrode needs to be integrated with other electronic materials. In this context, lattice-matched InAlN/GaN HEMTs with their excellent material and HEMT properties are the ideal electronics for the combination with BDD electrodes. Hence, in the beginning of this chapter two possible integration strategies, i.e. the "GaN first" and

the "diamond first" approach will be discussed, which, however, will generally result in different integration complexity and chemical stability.

This chapter shall discuss the combination of the two building blocks, i.e. the BDD electrode and the InAlN/GaN HEMT. The electrodes and the HEMTs were previously discussed as individual components in chapter 5 and chapter 3, respectively. Although sensor arrays were already fabricated, the focus in this work was kept on the analysis of the electrochemical performance of the combination of two individual elements, however with the perspective of developing a highly integrated sensor system ready for potentiometric and amperometric measurements. Thus, two basic combinations of the two elements, which are the basis for the implementation of such sensor systems, will be discussed. The first discussed combination is the extended gate ISFET configuration, where the remote BDD electrode is connected to the gate of the InAlN/GaN HEMT. In this case the FET is used as transducer or amplifier element and the corresponding potentiometric analysis is linked to the resolution of the pH sensitivity. Here, it shall be mentioned again that a change in the pH value manifests as a changed interface potential at the BDD surface. Thus, the pH value may be considered either as an additional input variable (like in this work) or as an intrinsic parameter affecting the threshold voltage of the device (compare oxide charges in a MOSFET [63]). In the second combination the BDD electrode is connected to the drain terminal of the HEMT, which in this case serves as a switch to turn on or off the electrode current (detection of redox reaction) of a BDD electrode and is needed to address an individual pixel of an array.

The chip layout is based on the layout of the electrode array chip described in chapter 5, therefore also consists of nine BDD electrodes arranged in a 3 by 3 matrix in the center of the $5 \times 5 \text{ mm}^2$ chip (see figure 6.1). For each electrode two FETs were implemented close to the bond pads of the chip, such that each electrode can be connected to the drain or to the gate of one separate FET (compare the sketches in figure 6.1), thereby being ready for dual mode operation (in terms of amperometric and potentiometric measurements with the same electrode). However, in this work the combination of the HEMT and the electrode was achieved by hybrid integration. This may add some additional resistance or may be a source of additional noise. However, the concept itself remains the same and allows to give fast feedback to the design of the HEMT.

With the BDD electrode being the actual electrochemical sensor and the InAlN/GaN HEMT being the supporting electronic element it is evident that the HEMT needs to match the boundary conditions established by the electrode. Thus, a large part of this chapter is dedicated to a discussion of these boundary conditions, which shall be used to establish certain design criteria for the FET. Although these boundary conditions are discussed separately for the two different applications, in an integrated system the FET would need to match the requirements of both applications.

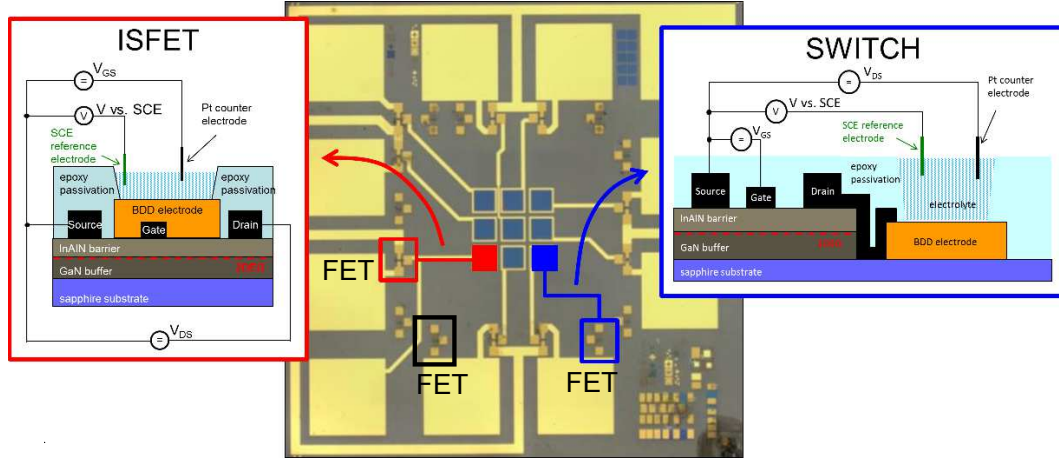


Figure 6.1: Picture of the fabricated $5 \times 5 \text{ mm}^2$ sensor array chip, where each electrode can be connected the gate (ISFET; left schematic) or the drain (switch; right schematic) of an InAlN/GaN HEMT.

6.1 InAlN/GaN HEMT and BDD Electrode Integration Technologies

Especially for the realization of sensor arrays, possibly with small pixel dimensions but extremely high density, monolithic integration of the sensor element and its electronic read-out circuit is inevitable to enable individually addressable pixels and a high spatial resolution. Generally, the monolithic integration of BDD electrodes and InAlN/GaN HEMTs on sapphire can be achieved via the two following processes:

1. "GaN first" approach:

The process starts with the complete HEMT fabrication, preferably following the GOS MISHEMT technology described in section 3.2. Then, the sample is subjected to the diamond growth process and is followed by the electrode patterning as described in the previous chapter. Due to the extreme diamond growth conditions, this method requires a high thermal stability of both, the GaN heterostructure and the employed HEMT device metallurgy.

2. "Diamond first" approach:

Here, the process starts with realization of the BDD electrodes on the substrate. Afterwards, the whole sample is overgrown with the InAlN/GaN heterostructure system. Then, the FETs are fabricated next to the BDD electrodes. The crucial point of this integration method is the preparation of the sapphire surface after electrode structuring, since a smooth, epi-ready surface is required for the subsequent heterostructure growth process.

The two process flows are also illustrated in figure 6.2, where the individual process steps, i.e. HEMT fabrication and electrode structuring, would follow those discussed before in this work. Although not shown in the figure (and not realized in this work), the GaN first approach would generally allow the integration of the BDD electrode directly on top of the InAlN/GaN HEMT, thus allowing a high integration density. Furthermore, this integration method would generally allow using diamond as the HEMT passivation layer. Since diamond is an inert material, such fabricated sensor systems are chemically highly stable and could be used even in aggressive media. In contrast, in the diamond first approach the chemical sensor and its read-out circuit can only be implemented next to each other (as shown in figure 6.2). Hence, the achievable integration density is generally lower compared to the GaN first method. Furthermore, the FET will not be passivated by diamond, thus limiting the application of such systems to rather mild liquid media. On the other hand, the diamond first approach allows the use of the more conventional and more conductive device metalization scheme (with Au overlay). Even more important than the freedom of InAlN/GaN device technology, is the fact that this approach potentially offers the freedom of choosing any semiconductor material like e.g. poly-silicon or zinc oxide, which can be deposited on the same substrate, but may be incompatible with diamond growth.

Since diamond growth is a harsh process, the integration of diamond on GaN-HEMTs is enabled due to the high, ceramic-like stability of the lattice-matched InAlN/GaN heterostructure (also indicated in chapter 4). Among semiconductor electronics, HEMTs based on the lattice-matched InAlN/GaN heterostructure seem the only electronic material system sustaining such harsh ambient conditions and, indeed, fully fabricated HEMTs were already successfully overgrown with diamond using this material system [18] (although the diamond layer was implemented as heat spreading layer in reference [18]). Nevertheless, the deposition of diamond onto fully fabricated InAlN/GaN HEMTs also requires an equally high stability of all materials involved in the HEMT fabrication process including the ohmic and gate contact metalization as well as the HEMT passivation material, at an temperature significantly higher than tested in chapter 4. Therefore, the Au-free device metalization scheme discussed in section 3.2 was developed and complemented by a silicon nitride passivation layer, which already demonstrated its compatibility with diamond overgrowth at such harsh growth conditions [18] and was also successfully employed for InAlN/GaN HEMT devices operating at temperatures beyond 800 °C [13, 24]. However, these experiments were mainly concerned with the open-channel HEMT characteristics (at high temperatures), but so far there seems no information available on a possibly permanent change of leakage characteristics due to materials degradation (contact metals or passivation). Indeed, during this work the SiN layer in combination with the amorphous silicon layer on top of the InAlN/GaN HEMT were identified as the source of additional leakage paths after diamond growth leading to overall device leakage currents larger than $\mu\text{A}/\text{mm}$ (on GOS MISHEMTs). Such leakage currents are significantly larger than reported in chapter 3 and (as will be explained later) are too large for the envisaged electrochemical applications discussed in this work.

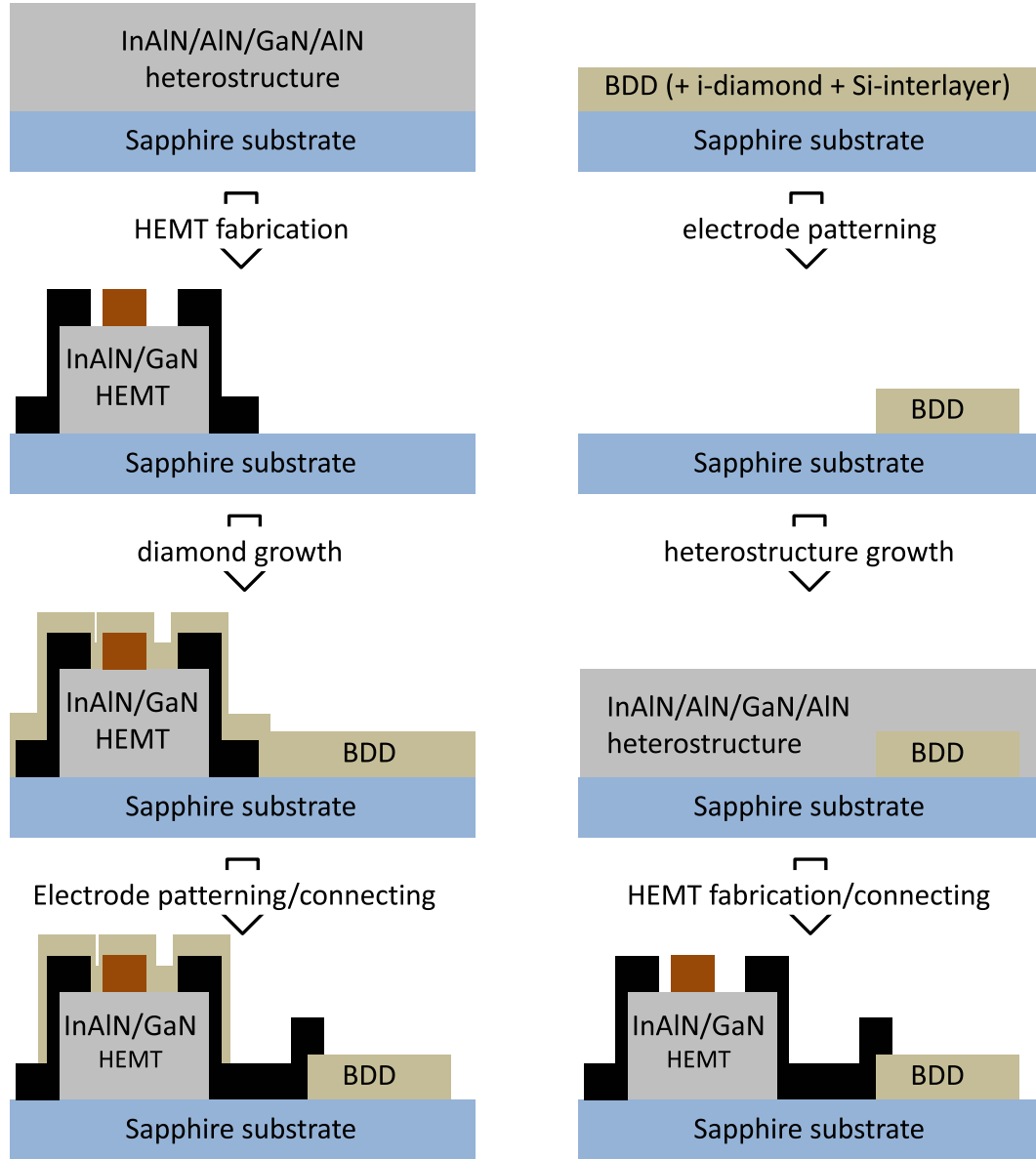


Figure 6.2: Illustration of the GaN first (left) and the diamond first (right) fabrication process to achieve monolithic integration of BDD electrodes and InAlN/GaN HEMTs. Left: Fabrication starts on InAlN/GaN heterostructures grown on sapphire. Process flow: Complete HEMT fabrication, non-selective diamond growth, diamond etching and electrode patterning, BDD electrode and FET interconnection. Right: Process starts on BDD films prepared on sapphire. Process flow: Electrode patterning and complete removal of Si interlayer outside active electrode, non-selective InAlN/GaN heterostructure growth, HEMT device fabrication including mesa etching, interconnection to BDD electrode.

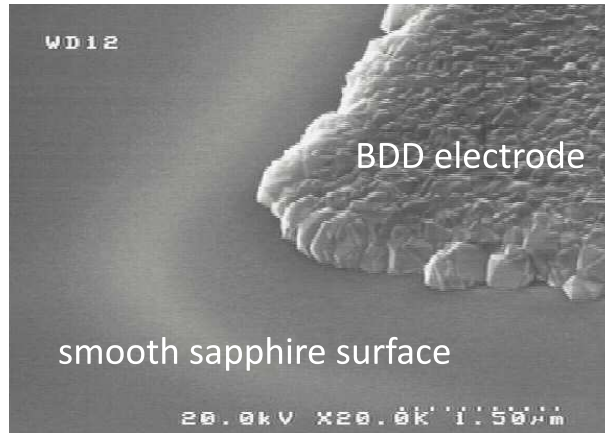


Figure 6.3: SEM picture of the prepared BDD electrode on sapphire with smooth surface. Growth done by S. Rossi and Z. Gao.

To eliminate the concern about the degraded HEMT leakage characteristics after diamond growth, the diamond first integration method was developed in this work. Since this method is new, some more details on the integration process itself and some first HEMT characteristics are provided in the following. It shall be stated here, that the focus of these initial experiments was to demonstrate the feasibility of the diamond first approach and the fabricated HEMTs are not yet completely realized in a GOS MISHEMT technology. Thus, the resulting leakage currents were not in the lower pA regime.

The diamond first integration process starts with the fabrication of the BDD electrodes on a sapphire wafer. Lateral overgrowth of MEA structures can be achieved by following exactly the process flow described in section 5.1. Thus, the BDD electrodes consisted of 50 nm SiN and 50 nm α -Si for bias enhanced nucleation, a 150 nm thick intrinsic diamond buffer and a 150 nm boron doped diamond film. The key to a successful subsequent heterostructure growth certainly is the preparation of the free sapphire surface outside the active electrode. For a high crystalline quality of the heterostructure a sapphire surface of epitaxial grade is desired meaning an atomically smooth surface without any residual diamond or traces of diamond or an interlayer. Here, the diamond was etched by an Ar/O₂ plasma in a RIE system. To avoid any damaging of the sapphire surface, the interlayer were etched using CF₄ plasma under conditions of pure chemical etching. Due to the high chemical stability of diamond also wet chemical etching might be appropriate. A SEM picture of the prepared BDD electrode before heterostructure overgrowth is shown in figure 6.3. The free sapphire surface appears clean and smooth as desired for a high crystalline quality of the InAlN/GaN heterostructure.

Onto the as-prepared sample the lattice-matched InAlN/GaN heterostructure was grown by MOCVD (by L. Lugani and J.-F. Carlin from Prof. N. Grandjeans group at EPFL). For this first experiment a rather conventional material stack was chosen.

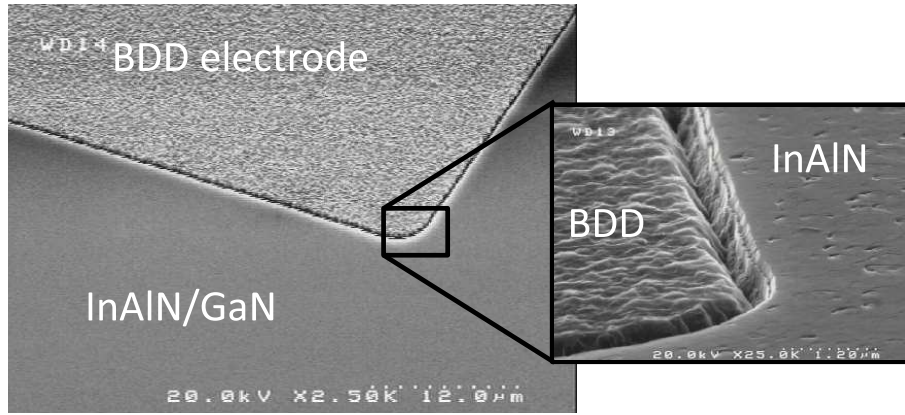


Figure 6.4: SEM photograph of a BDD electrode with overgrown InAlN/GaN heterostructure. The inset presents a zoom to BDD/heterostructure boundary. The InAlN/GaN growth seems selective and does not grow on the BDD.

The heterostructure consisted of a 50 nm AlN nucleation layer, a 500 nm GaN buffer, a 1 nm AlN spacer and a 5 nm lattice matched InAlN barrier. Figure 6.4 shows a SEM picture of a BDD electrode after the heterostructure was deposited. The inset clearly shows a gap between the BDD and the grown heterostructure strongly suggesting that GaN growth on BDD is limited, which is ascribed to the rough electrode surface and points out the importance of the sapphire surface preparation. Furthermore, there is no evidence for a degradation of the electrode structure due to the heterostructure growth process indicating also the high thermal stability of diamond. The rather smooth InAlN surface and the abrupt boundary indicate a high crystalline order, which might be surprising considering the close vicinity to the BDD structure. However, this may indicate that InAlN/GaN HEMTs can have excellent properties, even when fabricated close the diamond structures.

Followed by the heterostructure growth is the HEMT fabrication. As mentioned, the aim of this first experiment was to demonstrate the feasibility of the diamond first integration method. Therefore, the HEMT device technology used mainly followed the conventional GaN technology described in section 3.2. However, the first step to achieve GOS InAlN/GaN MISHEMTs, i.e. the deep mesa isolation process, was already implemented successfully. HEMT fabrication starts with mesa dry etching. To protect the open diamond electrodes (see figure 6.4) during the deep mesa etch process they were covered by a Ni metal mask, which was removed afterwards by a diluted HCl solution. As ohmic contact material stack chosen was the highly conductive Ti/Al/Ni/Au (15/100/40/60 nm) metal stack, which generally led to lower access resistances (see figure 3.5). Surface oxidation was omitted for this first experiment. The gate metalization was Ni/Au (40/160 nm) and the connection between HEMTs and BDD electrodes was achieved by a Ti/Au (20/200 nm) material stack. This also included the electrode surrounding metal and an additional HEMT contact metalization onto the gate, drain, and source contacts. A photograph of a fabricated chip was already shown in figure

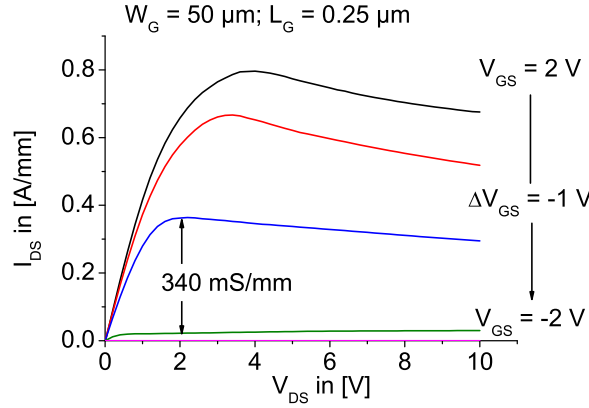


Figure 6.5: Typical DC HEMT output characteristics of a 50 μm wide device. The maximum output current density is $I_{\text{DS}}(V_{\text{GS}} = 2 \text{ V}) = 0.8 \text{ A/mm}$.

6.1, where the combination of BDD electrodes and InAlN/GaN HEMTs was realized in the ISFET configuration, i.e. the electrodes were connected to the HEMT gates. Since the employed HEMT technology does not result in low leakage characteristics (see below; compare section 3.3), ISFET measurements could not be conducted. Thus, the materials characterization provided in the following is limited to HEMT analysis. Nevertheless, this will still reveal information on the material quality of the heterostructure and therefore may give an indication about the feasibility of monolithically integrated ISFET devices using this approach.

A basic characterization of the heterostructure and the device technology was conducted by means of TLM measurements. The resulting sheet resistance was $R_{\text{sh}} = 753 \Omega$ and the extracted specific contact resistance was $\rho_C = 0.85 \Omega\text{mm}$. In general, these values are well comparable to those obtained for the samples discussed in section 3.3 also fabricated in this technology. However, here the resulting sheet resistance is slightly larger and the contact resistance smaller, which might be linked to a slightly thinner InAlN barrier layer (see below). A DC output characteristics of a 50 μm wide device ($L_G = 0.25 \mu\text{m}$, $L_{\text{SG}} = 1 \mu\text{m}$) is shown in figure 6.5. The gate-source voltage swing was from $V_{\text{GS}} = 2 \text{ V}$ to $V_{\text{GS}} = -2 \text{ V}$ in steps of $\Delta V_{\text{GS}} = -1 \text{ V}$. The resulting peak current density is $I_{\text{max}}(V_{\text{GS}} = 2 \text{ V}) = 0.8 \text{ A/mm}$, which is exactly the value of the 450 nm GaN sample in standard GaN technology discussed in chapter 3.3. In consequence to the low specific contact resistance, the on-resistance extracted at $V_{\text{GS}} = 2 \text{ V}$ and $V_{\text{DS}} = 1 \text{ V}$ is $R_{\text{on}} = 2.4 \Omega\text{mm}$. The transconductance, here simply extracted from the output characteristics at $V_{\text{DS}} = 2 \text{ V}$ and at V_{GS} between 0 V and -1 V, is as high as $g_m = 340 \text{ mS/mm}$. All together, these values speak for the high material quality of the InAlN/GaN heterostructure deposited onto the patterned sapphire wafer.

The transfer characteristics at $V_{\text{DS}} = 5 \text{ V}$ (close to I_{max}) in linear and semilogarithmic scale are presented in figure 6.6(a) and figure 6.6(b), respectively. As mentioned, the deep mesa isolation process was already implemented and is compared to a device with

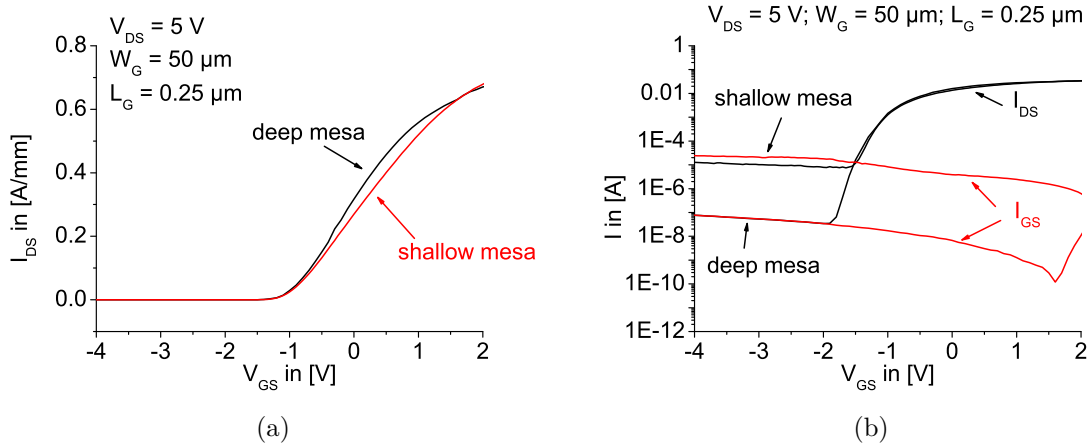


Figure 6.6: (a) Comparison of the linear transfer characteristics of a device with deep mesa (black) and shallow mesa (red). (b) Corresponding semilogarithmic transfer characteristics. Depicted are the output currents I_{DS} (black) and the parasitic gate leakage currents I_{GS} (red). Gate leakage is significantly lower for the deep mesa isolated device.

shallow mesa etching. This means that the gate, drain, and source contact pads were positioned directly on the sapphire (deep mesa) or on the etched free GaN surface (shallow mesa). Above threshold the two curves are nearly identical also resulting in the same threshold voltage of $V_{th} = -1\text{ V}$. For a non-oxidized InAlN surface this threshold voltage corresponds rather to an InAlN barrier thickness of approximately 4 nm instead of 5 nm and consequently to a lower 2DEG carrier concentration n_s (compare figure 6.8). As mentioned, this might be the reason for the larger extracted sheet resistance and smaller specific contact resistance. However, in this case the resulting output current density of 0.8 A/mm is even more surprising, since the carrier concentration should be reduced to $n_s = 1.0 \times 10^{13}\text{ cm}^{-2}$ corresponding to only 70% of the n_s expected with a 5 nm barrier. Due to the implemented deep mesa isolation, a significant difference in the subthreshold behavior can be observed. Employment of the deep mesa isolation eliminated leakage currents around the active device and led to a reduction of the leakage by two orders of magnitude ($I_{off} \approx 12\text{ }\mu\text{A}$ and $I_{off} \approx 75\text{ nA}$ for the device with shallow and deep mesa, respectively). Nevertheless, with the absence of the thermally grown oxide the residual leakage current may be ascribed to gate leakage. Such leakage currents are within the range of what was reported for the standard GaN devices discussed in section 3.3 also utilizing Ni/Au gates on an oxide-free InAlN surface (see figure 3.12).

Further reduction of the off-currents, even to the lower pA regime, seems possible by applying InAlN surface oxidation and using Cu/Pt gate metalization in combination with ultrathin GaN buffers. Thus, high performance monolithic integrated ISFETs consisting of BDD electrodes and lattice matched InAlN/GaN HEMTs seem feasible by using the diamond first integration method. However, possible negative side effects on the BDD electrode due to the heterostructure growth or the oxidation process need

further investigation. An electrochemical characterization of the BDD electrode after the full ISFET fabrication or after heterostructure growth was not conducted. However, so far no obvious degradation of the BDD film was observed (see again figure 6.4). Additionally, probing the HEMT not at the gate contact pad but at the BDD electrode resulted in the same output and transfer characteristics, which can only be expected as long as the diamond film maintains its rather high conductivity. Furthermore, it was mentioned above that this integration method allows the integration of diamond components (not limited to electrodes, see again the introduction of chapter 5) with other electronic materials. Thus, some of these questions may be excluded by choosing other semiconductor materials, like thin film transistors based on polycrystalline silicon [134], zinc oxide [135], or organics [136], which can be deposited under relatively low temperatures and mild conditions (compared to GaN heterostructure growth [79]). However, FETs fabricated in other materials may lack the device performance of InAlN/GaN HEMTs.

6.2 Prerequisites for ISFET Measurements

In the ISFET configuration there are basically two HEMT parameters, which should match to the requirements set by the BDD electrode. In essence, both parameters are linked to the modulation efficiency of the FET. Therefore one parameter is the HEMT threshold voltage V_{th} and the other is the equivalent HEMT input circuit including both, the gate-source capacitance C_{GS} and the gate-source resistance R_{GS} . The latter, of course, presents an indication of the gate leakage current. In case of InAlN/GaN HEMTs V_{th} and C_{GS} are controlled by the barrier layer thickness. In contrast, R_{GS} is widely influenced by the HEMT device processing. As will be shown, a large R_{GS} is desired already indicating the importance of the developed GOS MISHEMT technology. Furthermore, like a FET alone, the FET of the ISFET can be biased into different operation regions. These regions are the linear or Ohmic region at low V_{DS} , the saturation region at larger V_{DS} , and the subthreshold region at a gate voltage below V_{th} . The two regions investigated for this work are the saturation region (maximum transconductance, thus highest pH-sensitivity) and the subthreshold region (low output currents, but exponential pH-sensitivity).

6.2.1 Matching the Threshold Voltage

Since measurements in the ISFET configuration present potentiometric measurements, i.e. the detection of interface potentials at the electrode in contact with different electrolytes, their corresponding measurements are limited to an electrode potential inside the potential window, where no charge is transferred and no electrode current distorts

the measurements. In order to achieve complete HEMT modulation, i.e. from fully open channel to pinch-off, thus allowing precise adjustment of the resulting output current density, the potential window and the modulation range should be identical or at least must not be limited by the InAlN/GaN HEMT. This shall be illustrated by figure 6.7(a), in which the voltammograms of the fabricated $200 \times 200 \mu\text{m}^2$ BDD electrode in pH = 1 and pH = 13 solution are correlated to the transfer characteristic of an InAlN/GaN HEMT. It is important to note that in this case the electrode potential V vs. SCE corresponds to a gate-source potential V_{GS} of opposite sign, because the measurements are related to the reference electrode. The two important potentials are then marked by the oxygen evolution in pH = 1 (V vs. SCE $\approx 1.7 \text{ V} \rightarrow V_{\text{GS}} \approx -1.7 \text{ V}$) and the hydrogen evolution in pH = 13 (V vs. SCE $\approx -1.5 \text{ V} \rightarrow V_{\text{GS}} \approx 1.5 \text{ V}$). Thus, an InAlN/GaN HEMT with a threshold voltage (obtained by linear extrapolation) of $V_{\text{th}} = -1.7 \text{ V}$ and a linear response up to $V_{\text{GS}} = +1.5 \text{ V}$ presents the ideal candidate for ISFET application. A measure for the response of the system on changes of the pH value is then given by the HEMT transconductance g_m , where a high pH sensitivity is obtained for HEMTs with a large transconductance ($g_m \nearrow \Rightarrow \Delta I_{\text{DS}}/\Delta \text{pH} \nearrow$). Thus, GaN HEMTs with their large normalized transconductance (up to 800 mS/mm [17]) present the ideal basis for the development of ISFETs with high pH sensitivity and resolution.

However, there might be certain applications, e.g. biological applications, where living cells are investigated [131], for which it is of particular interest to avoid heat generation. In case of a monolithic integrated system such applications are therefore limited to very low currents. Hence, it seems attractive to implement HEMTs with a scaled gate-width even below the sub-micron regime, which were already demonstrated in the InAlN/GaN system exhibiting a current density of $2.9 \mu\text{A/nm}$ [137]. An alternative approach to achieve low currents, while maintaining a more conventional device technology, may be the exploitation of the subthreshold regime of the InAlN/GaN HEMT, where its output current could be reduced to the lower pA regime even for $100 \mu\text{m}$ wide devices (compare chapter 3.3). This case is illustrated in figure 6.7(b), where the cyclic voltammograms of the electrode are correlated to a semilogarithmic transfer characteristics of an InAlN/GaN HEMT. Obviously, in this case the threshold voltage V_{th} obtained by linear extrapolation is no longer the parameter to be matched to the electrochemical requirements. Instead, the voltage where the reverse current reaches a plateau presents the parameter of interest, which, like before, shall be referred to as pinch-off voltage V_{off} . In order to exploit then the full subthreshold regime a pinch-off voltage of $V_{\text{off}} \leq -1.7 \text{ V}$ is desired. However, in the subthreshold regime the dependence of the HEMT output current on the gate-source voltage is described by an exponential law. This means that very small changes of the pH value should result in an extremely large relative change of the output current. The parameter determining the pH response of the system in the subthreshold regime is then the subthreshold swing SS . A low SS translates to a high pH sensitivity ($SS \searrow \Rightarrow \Delta I_{\text{DS}}/\Delta \text{pH} \nearrow$).

While the threshold or pinch-off voltage in InAlN/GaN HEMTs are engineered by the InAlN barrier layer thickness, the linear response up to large positive gate biases is

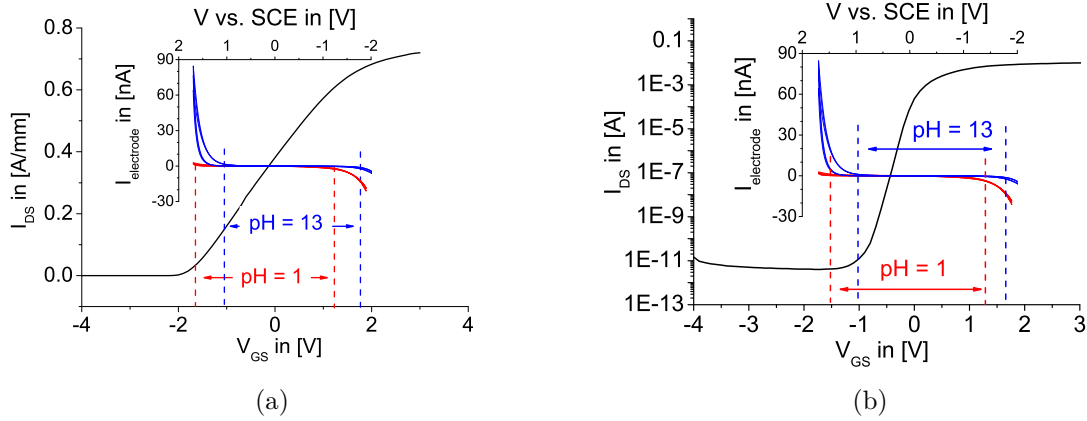


Figure 6.7: Transfer characteristics of an InAlN/GaN HEMT at $V_{DS} = 6$ V in (a) linear) and (b) semilogarithmic scale correlated to the cyclic voltammogram of a BDD electrode in pH = 1 (red) and pH = 13 (blue). The dashed lines indicate the potential window in the respective electrolyte.

mainly achieved by eliminating both, parasitic current limiting effects (proper surface passivation scheme [49, 47]) and parasitic gate leakage currents (surface oxidation, see section 3.3.3).

The change of the threshold and the pinch-off voltage of Cu gates on oxidized (MIS-HEMT) and non-oxidized (HEMT) InAlN barriers with varying thickness is depicted in figure 6.8(a). As expected a linear dependency of V_{th} and V_{off} on t_{InAlN} is observed (compare equation (2.7)) for the HEMT and the MISHEMT, however, oxidation of thin barriers corresponds to a reduction of the 2DEG sheet charge density n_s and therefore causes a positive parallel shift of the threshold or pinch-off voltage, in this case by $\Delta V_{th} = \Delta V_{off} \approx +0.4$ V. The shift of V_{th} is different compared to the one presented in section 3.3, which most likely is related to variations in the oxidation process (manual loading, temperature inaccuracies).

In case of the MISHEMTs an InAlN thickness of 6.0 nm satisfies the desired threshold voltage of $V_{th} = -1.7$ V and a thickness of approximately 5.0 nm matches the desired V_{off} (a thickness of 5.5 nm or 4.5 nm is determined for HEMT devices, respectively). As discussed earlier, the maximum available 2DEG carrier concentration n_s for lattice-matched InAlN/GaN heterostructures is $2.6 \times 10^{13} \text{ cm}^{-2}$, a value which can only be obtained for barrier layer thicknesses larger than 10 nm or if a proper surface passivation scheme is applied (not yet implemented). Figure 6.8(b) shows the change of n_s with barrier thickness, where the desired barrier thickness of MISHEMTs are indicated. At 6.0 nm n_s is approximately $1.8 \times 10^{13} \text{ cm}^{-2}$ still around 70 % of its maximum value and is further decreased to $n_s \approx 1.4 \times 10^{13} \text{ cm}^{-2}$ in case of a 5.0 nm thin barrier. However, surface oxidation will then lead to an additional reduction of n_s , which is already observed by the change in the threshold voltage.

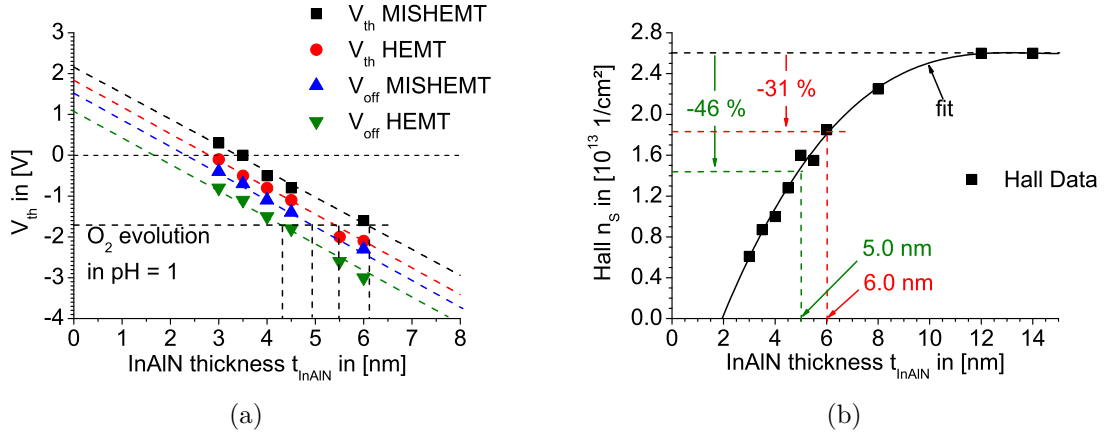


Figure 6.8: (a) Change of V_{th} and V_{off} with InAlN thickness for MISHEMTs (V_{th} : black squares; V_{off} : blue up triangles) and HEMTs (V_{th} : red circles; V_{off} : green down triangles) and their respective linear interpolations. The gate contact material is Cu. The horizontal dashed line marks the O₂ evolution in pH = 1 electrolyte. The vertical dashed lines mark the matching InAlN thicknesses. (b) Corresponding Hall n_s for untreated InAlN surfaces. Black squares indicate extracted values obtained by Hall measurements in this work and after [47]. The green and the red lines indicate the desired barrier thicknesses of MISHEMTs and the corresponding resulting n_s .

With a barrier layer thickness of 5.0 nm both InAlN/GaN FET concepts discussed in chapter 3 (HEMT and MISHEMT) match the desired InAlN thickness and full HEMT modulation exploiting the large potential window could be expected with either device concept. However, the next section will deduce the requirement of low gate leakage currents, which is why only the fabricated MISHEMT devices could be used for ISFET measurements.

6.2.2 Matching the HEMT Input Circuit

The combination of the BDD electrode and the InAlN/GaN HEMT also presents a combination of their respective small signal equivalent circuit models, which describe their dynamic behavior. However, in the following the combination of the equivalent circuit models shall be used to identify the components, which may greatly affect the response of the system. In order to obtain a high pH sensitivity (in terms of $\Delta I_{DS}/\Delta pH$) as well as full HEMT modulation a careful design of the individual components is required [131, 133]. Therefore, figure 6.9 shows the combined small signal equivalent circuit, where the BDD electrode is presented by the simplified model of a large area electrode (compare figure 5.6(c)). The assumed HEMT input circuit consists of a parallel $R_{GS} \parallel C_{GS}$ and a series source resistance R_{source} . C_{GS} presents the capacitive coupling of the 2DEG carrier concentration n_s depending on the potential across the InAlN/AlN barrier layer

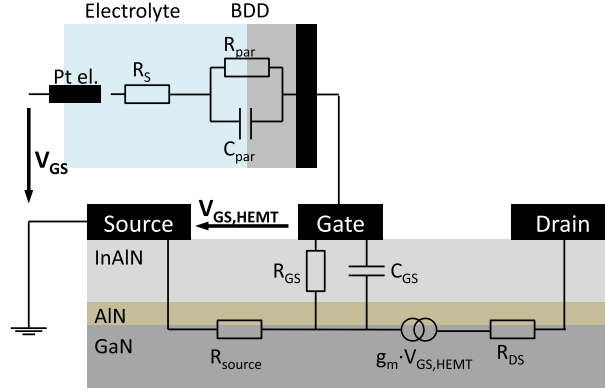


Figure 6.9: Depiction of the equivalent circuit of the ISFET consisting the BDD/electrolyte interface and the HEMT. The HEMT input circuit is presented by the gate capacitance C_{GS} and a parallel resistance R_{GS} . The HEMT access resistance R_{source} is given by a combination of the sheet and contact resistance. The current source $g_m \cdot V_{GS,HEMT}$ and R_{DS} model the HEMT output. V_{GS} is the voltage applied at the PT counter electrode and $V_{GS,HEMT}$ indicates the voltage drop between the HEMT gate and source contact.

and R_{GS} presents a quantity for the gate leakage current. The HEMT output circuit is given by the current source $g_m \cdot V_{GS,HEMT}$, the output resistance R_{DS} , and also the source series resistance R_{source} . R_{source} is a combination of the contact resistance R_C and a resistance determined by the device geometry and the sheet resistance R_{sh} . The focus of this first design study will be the input circuit, because matching the HEMT input circuit to the BDD electrode should allow to fully exploit the available g_m of the HEMT, which is essential to obtain a high pH sensitivity. It shall be mentioned again, that in case of this simplified equivalent circuit of the BDD electrode R_{par} and C_{par} present a combination of the depletion and double layer. Therefore, this model describes the overall behavior of the BDD/electrolyte interface under the conditions of no charge transfer, which seems sufficient for this design study.

The parameter mainly affecting the pH sensitivity is the transconductance g_m , which is defined by the equation

$$g_m = \left. \frac{dI_{DS}}{dV_{GS}} \right|_{V_{DS}=const.} \quad (6.1)$$

and determines the change of the output current per change of the input voltage. However, the change of the output current of the ISFET only depends (at constant V_{DS}) on the potential change occurring on the FET gate ($V_{GS,HEMT}$, compare figure 6.9). The potential $V_{GS,HEMT}$, which establishes at the gate terminal depends on both, the potential applied at the counter electrode and the pH value. In order to achieve a high sensitivity of the output current on the pH value, the gate potential $V_{GS,HEMT}$ must approach the externally applied potential at the counter electrode ($V_{GS,HEMT} \approx V_{GS}$). To be able to calculate the self-establishing potential at the gate terminal it is beneficial to initially approach the problem under pure DC bias conditions. Hence, the input circuit simplifies

to a resistive voltage divider consisting of the four resistances R_S , R_{par} , R_{GS} , and R_{source} . The gate potential (including both, the potential across the InAlN/AlN barrier and the source access region) can be calculated by:

$$V_{GS,HEMT} = \frac{V_{GS}}{R_S + R_{par} + R_{GS} + R_{source}} (R_{GS} + R_{source}) \quad (6.2)$$

The resistances at the BDD/electrolyte interface were previously determined to $R_S = 240 \text{ k}\Omega \dots 360 \text{ k}\Omega$ and $R_{par} = 2 \text{ G}\Omega \dots 5 \text{ G}\Omega$, respectively, slightly depending on the DC bias point and the pH of the electrolyte (compare section 5.3). As mentioned above, the source resistance R_{source} is a combination of the specific contact resistance ρ_C and a resistance determined by the sheet resistance R_{sh} and the corresponding device geometry. It is given by the equation

$$R_{source} = \frac{\rho_C}{W_G} + R_{sh} \frac{L_{GS}}{W_G}, \quad (6.3)$$

where L_{SG} is the gate-source distance and W_G is the gate width. Assuming very high values of $\rho_C = 10 \text{ }\Omega \cdot \text{mm}$ and $R_{sh} = 1000 \text{ }\Omega$ (much higher than extracted in section 3.3 for thin barriers) the resulting source resistance will still be below $R_{source} = 1000 \text{ }\Omega$, as long as the gate width remains larger than $W_G > 11 \text{ }\mu\text{m}$ ($L_{SG} = 1 \text{ }\mu\text{m}$). This means that both series resistances, R_S and R_{source} , are several orders of magnitude smaller than the resistance of the BDD electrode R_{par} and consequently the voltage drop at both resistances can be neglected. Therefore equation (6.2) can be simplified further to

$$V_{GS,HEMT} = \frac{V_{GS}}{R_{par} + R_{GS}} R_{GS}, \quad (6.4)$$

by which immediately the necessity of a very large R_{GS} , ideally well above $100 \text{ G}\Omega$, becomes obvious, if a $V_{GS,HEMT}$ in the same range as V_{GS} is desired. This reveals that gate leakage is a crucial parameter for the development of extended gate ISFETs. However, this is usually less problematic in Si MOSFETs, but it is of special interest for GaN HEMTs, because the gate diode usually presents a Schottky diode. For the fabrication of ISFETs using BDD electrodes, the reduction of gate leakage is even more important, since the background current of the BDD electrode is significantly reduced compared to conventional metal electrodes [5]. Thus, the oxidation of the InAlN surface is a key technology to enable ISFETs consisting of InAlN/GaN HEMTs and BDD electrodes.

Even though the before described analysis gives an indication about the voltage distribution within the system, the capacitors of figure 6.9 must not be neglected, since the modulation of the 2DEG carriers, hence the modulation of the drain-source current I_{DS} , in an InAlN/GaN HEMT is based on the capacitive coupling between the gate metal and the channel, where the parallel resistance R_{GS} actually presents only the leakage characteristics of the gate diode. Thus, the accumulation of charges in the 2DEG channel needs to be considered by taking into account the series connection of the electrode capacitance C_{par} and the capacitance C_{GS} given by the InAlN/AlN barrier layer.

In the series connection of the two capacitors C_{par} and C_{GS} the total amount of accumulated charges $Q_{\text{tot}} = qn_s A$ is constant and calculated by

$$Q_{\text{tot}} = C_{\text{tot}} \cdot V_{\text{GS}} = C_{\text{GS}} \cdot V_{\text{GS,HEMT}} = C_{\text{par}} \cdot (V_{\text{GS}} - V_{\text{GS,HEMT}}), \quad (6.5)$$

where $C_{\text{tot}} = \frac{C_{\text{par}} \cdot C_{\text{GS}}}{C_{\text{par}} + C_{\text{GS}}}$ is the total capacitance of the series connection. This means that the gate potential $V_{\text{GS,HEMT}}$ depending on the externally applied potential V_{GS} is given by the equation

$$V_{\text{GS,HEMT}} = \frac{C_{\text{tot}}}{C_{\text{GS}}} V_{\text{GS}} = \frac{C_{\text{par}}}{C_{\text{par}} + C_{\text{GS}}} V_{\text{GS}}. \quad (6.6)$$

In order to fulfill the requirement that $V_{\text{GS,HEMT}}$ should be in the range of V_{GS} , a large C_{par} (compared to C_{GS}) is desired. Although equation (6.6) already gives the correct indication for the design of the respective capacitances, it might be useful to link the accumulated charges n_s to the resulting drain-source current ($I_{\text{DS}} \propto n_s$), hence to the transconductance (compare equation (6.1)). Therefore, the charge accumulation in the HEMT only (one capacitance with $Q_{\text{tot}} = qn_s A$) will be compared to the charge modulation in the hybrid system (two capacitances with $Q'_{\text{tot}} = qn'_s A$). The comparison of the two models yields

$$\frac{\text{HEMT}}{\text{hybrid system}} = \frac{Q_{\text{tot}}}{Q'_{\text{tot}}} = \frac{qn_s A}{qn'_s A} = \frac{V_{\text{GS,HEMT}}}{V_{\text{GS}}} \frac{C_{\text{GS}}}{C_{\text{tot}}}. \quad (6.7)$$

Assuming that the gate potentials of the two different systems are identical ($V_{\text{GS,HEMT}} = V_{\text{GS}}$) the modulated 2DEG carrier concentration n'_s of the hybrid system can be correlated to that of the HEMT only, by

$$n'_s = \frac{C_{\text{par}}}{C_{\text{par}} + C_{\text{GS}}} n_s. \quad (6.8)$$

In essence, this presents the same relation as equation (6.6) and again the need of a rather large C_{par} is evident. Using equation (6.8) and the fact that the drain-source current is proportional to the accumulated charges in the 2DEG channel ($I_{\text{DS}} \propto n_s$), the extrinsic transconductance of the hybrid system can be expressed by

$$g_{m,\text{hybrid system}} = \frac{C_{\text{par}}}{C_{\text{par}} + C_{\text{GS}}} g_{m,\text{HEMT}}. \quad (6.9)$$

This means that the extrinsic transconductance, which is a measure for the pH sensitivity of the ISFET, is generally smaller than the transconductance of the HEMT alone.

The value of the parallel capacitance within the potential window was previously determined to the range between $C_{\text{par}} = 0.5 \dots 1.0 \mu\text{F} \cdot \text{cm}^{-2}$, slightly depending on the applied electrode potential (see section 5.3). This corresponds to an absolute value of the capacitance of $C_{\text{par}} = 200 \dots 400 \text{ pF}$ for the fabricated $200 \times 200 \mu\text{m}^2$ electrodes. In case of the MEAs, the capacitance was dominated by parasitics resulting in a constant capacitance (within a certain potential regime) in the range of 30 pF. Thus, in order to

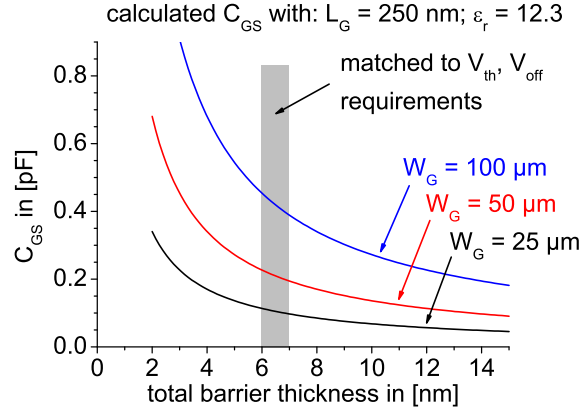


Figure 6.10: Calculated change of the gate-source capacitance C_{GS} with total barrier layer thickness $t_{\text{InAlN}} + t_{\text{AlN}}$ for HEMT devices with $L_G = 250$ nm; $W_G = 25$ μm , 50 μm , and 100 μm . The gray area indicates the window, where the barrier layer thickness matches the requirements of V_{th} or V_{off} .

achieve a high pH sensitivity of the HEMT in combination with both electrode types, the barrier layer capacitance C_{GS} must be significantly smaller than this 30 pF. However, the direct measurement of the barrier layer capacitance, for instance by capacitance voltage measurements, on the realized HEMT device structures, where the gate dimensions typically are extremely small ($L_G = 250$ nm, $W_G \leq 100$ μm), is difficult, especially at low frequencies. Therefore, in this work the determination of C_{GS} relies on the evaluation of CV measurements conducted on large gate test diodes. However, the gate-source capacitance of GaN-based devices does not evolve linearly with the gate area, which generally leads to an underestimation of C_{GS} [138]. A way to circumvent this problem, which is also used in this work, is reported in [139], where the analysis of CV measurements is based on the evaluation of the voltage, where the channel is depleted (in CV measurements), by which the relative permittivity ϵ_r of the barrier layer is obtained. Then, this is used to calculate the capacitance C_{GS} . Further details about this method together with the corresponding CV measurements and analysis are provided in the appendix E. The relative permittivity obtained by this method of the total barrier system for MISHEMTs (the total barrier consists of the oxide, the lattice matched InAlN and the AlN spacer) is $\epsilon_r = 12.3$, which now can be used to calculate the gate-source capacitance according to:

$$C_{GS} = \frac{\epsilon_0 \cdot \epsilon_r \cdot L_G \cdot W_G}{t_{\text{InAlN}} + t_{\text{AlN}}} \quad (6.10)$$

A depiction of the calculated C_{GS} for three typical HEMT device geometries ($L_G = 250$ nm; $W_G = 25$ μm , 50 μm , and 100 μm) depending on the total barrier layer thickness is shown in figure 6.10.

Since C_{par} should be much larger than C_{GS} (to obtain a high pH sensitivity), the resulting gate-source capacitance for $W_G = 100$ μm is of special interest. The gate-source

capacitance at an InAlN barrier thickness of $t_{\text{InAlN}} = 5.0$ nm (MISHEMT matched to V_{off}) is $C_{\text{GS}} \approx 0.5$ pF and at an InAlN thickness of $t_{\text{InAlN}} = 6.0$ nm (MISHEMT matched to V_{th}) it is $C_{\text{GS}} \approx 0.4$ pF. This means that even if a microelectrode array ($C \approx 30$ pF) is connected to the gate of a $100 \mu\text{m}$ wide MISHEMT, nearly full HEMT modulation can be expected. However, it was mentioned that the capacitances of the MEAs were dominated by parasitics and the situation may change, if the theoretical values of $C_{\text{par}} \approx 2$ pF and $C_{\text{cap}} \approx 10$ pF (see chapter 5.3) dominate the MEA behavior. In such cases, HEMT modulation and the pH sensitivity might be reduced even for a $25 \mu\text{m}$ wide device and further HEMT device downscaling might be necessary.

6.3 Requirements in the Switch Configuration

In the switch configuration the BDD electrode is connected to the drain terminal of the InAlN/GaN HEMT and the idea behind is to use the HEMT as a switch for turning on or off the BDD electrode pixel for a subsequent read-out electronic circuit. It shall be mentioned again that measurements in the switch configuration are related to amperometric measurements, where the signal current on the BDD electrode arises from the reduction or oxidation reaction of a redox system (see chapter 5.4). This implies that the electrode potential ($= V_{\text{DS}}$ in the switch configuration, see figure 6.1) must be limited to a potential within the potential window. A switch ideally presents a short circuit in the on-state and an open circuit in the off-state, two requirements that cannot easily be fulfilled using an FET as electronic switch. If a FET is biased into on-conditions, it still exhibits a series resistance determined by its contact resistances, its sheet resistance, and by its device geometry. In contrast, when the device is biased into the off-state, there are leakage paths present in the device causing a residual off-current. This means that the FET can be modeled by a series resistance describing its off-state and another series resistance describing its on-state. The respective FET resistance should be much smaller (on-state) or much larger (off-state) compared to the resistance of the BDD electrode. With the analysis of the individual elements (see chapter 3 for the HEMT and chapter 5 for the electrode) it can clearly be stated that, regardless of the employed InAlN/GaN FET technology and device structure, the FET in its on-state presents a very small resistance (compared to the electrode) and no limitations are expected. On the contrary very different off-currents were observed for the different HEMT concepts, strongly depending on the device technology and structure. Thus, it is worth taking a close look to the switch characteristics with respect to the influence of residual off-state leakage.

The switch transfer characteristics is constructed under the following measurement and boundary conditions: The chosen electrolyte was a KCl solution in which 1 mMol $\text{Ru}(\text{NH}_3)_6^{2+}$ molecules were dissolved. This means that for these measurements only reduced species were in the electrolyte and consequently the oxidation peak was pro-

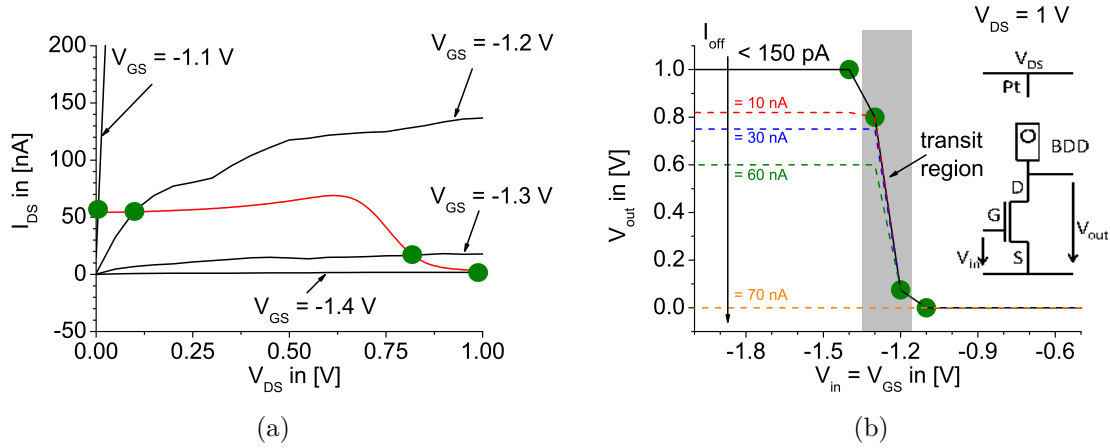


Figure 6.11: (a) HEMT output characteristics of a 50 μm wide device in the subthreshold regime with the IV characteristics of the BDD electrode as load line. (b) Constructed switch characteristics using the values of (a). The colored lines present the resulting characteristics with similar characteristics, but off-currents of 10 nA, 30 nA, 60 nA, and 70 nA.

nounced. The oxidation reaction of this redox system occurs at negative electrode potentials vs. SCE, and therefore correlates to a positive V_{DS} at the Pt electrode (remember that V_{DS} includes the potential drop in the electrolyte and at the BDD electrode). A drain-source voltage of $V_{DS} = 1$ V was chosen to remain inside the potential window. Simultaneously, at this drain-source potential the electrode current can be expected to be limited by the diffusion pattern, but not by the reaction kinetics (compare section 5.4).

In order to construct the switch characteristics the HEMT output characteristics has to be measured in a comparable current and voltage range. However, the electrode current of the large area electrode was 60 nA, which corresponds to the subthreshold regime of the discussed InAlN/GaN HEMTs. Therefore, figure 6.11(a) shows the output characteristics of a 50 μm wide InAlN/GaN MISHEMT (here, 200 nm GaN + 50 nm AlN) recorded in the subthreshold regime. The IV characteristics of the large planar BDD electrode for a simple potential sweep from 0 V to 1 V vs. SCE ($s = 200$ mV/s) is plotted as load line in the same diagram. The intersections of the two characteristics (green circles) are used to construct the switch characteristics of figure 6.11(b). With the selected HEMT the electrode pixel can be completely turned on or off. While this was expected for the on-state, in the off-state this is only possible, due to the extremely low I_{off} , thus indicating the importance of the low overall device leakage current of the FET. Since this MISHEMT offers a subthreshold swing of $SS \approx 80$ mV/dec, the transition from on to off is sharp and occurs, with the chosen parameters, within a range of approximately 200 mV.

The necessity of a low I_{off} , which presents the sum of residual gate and buffer leakage, is further illustrated in figure 6.11(b). Assuming that the device had similar device characteristics, but exhibiting an increased I_{off} (10 nA, 30 nA, 60 nA, and 70 nA) the corresponding switch characteristics would be significantly distorted. With off-currents larger than the oxidation current no switch-off operation would be possible. The need for a low I_{off} gets more pronounced, if the electrode current becomes much smaller, e.g. through downscaling of the electrode as might be desired for the fabrication of a sensor array, or if the ion current of single cells, which may be as low as 15 pA, shall (probably spatially resolved) be measured [103, 22]. This means that such sensor systems require FETs exhibiting low off-currents, which could be obtained already using thin body InAlN/GaN HEMTs prepared in the GOS technology.

In this proof-of-concept study, the analysis shall be limited to the oxidation reaction of $\text{Ru}(\text{NH}_3)_6^{2+}$ molecules. However, in real applications both, the oxidation and the reduction, also of other molecules may be of equal interest. Currents from reduction reactions are negative and other species may have a positive redox potential (vs. SCE) corresponding to a negative V_{DS} . Thus, the following two questions may arise:

1. Is the switching of negative reductions currents possible?
2. Can redox reactions occurring at negative V_{DS} be investigated?

The answer to question 1 is rather simple. The drain-source region of the FET does not have rectifying properties and, consequently, will not prefer currents of either sign. Question 2 is more difficult to answer, since negative V_{DS} cause the FET to operate in its reverse mode (the drain potential is lower than the source potential \Rightarrow the gate-drain potential determines the HEMT bias point). This means that switching operations at negative V_{DS} is possible, if the reverse mode is considered accordingly.

6.4 The InAlN/GaN MISHEMT and BDD Electrode ISFET

The discussion of the two HEMT technologies in chapter 3 revealed that only the thin body MISHEMTs (50 nm GaN + 50 nm AlN heterostructure system or 200 nm GaN + 50 nm AlN heterostructure system) prepared in the GOS technology satisfy the requirements of both applications (ISFET \Rightarrow large R_{GS} , switch \Rightarrow low I_{off}), which would be required in a monolithically integrated system. Mainly due to its larger extrinsic transconductance of $g_m = 160 \text{ mS/mm}$ and the slightly larger output current density of $I_{\text{DS}} = 0.4 \text{ A/mm}$, here devices of the 200 nm GaN + 50 nm AlN sample were chosen for the following analysis. As mentioned before, the combination of electrodes and FETs

was obtained by hybrid integration. This enables to combine different electrode structures (macroscopic electrodes and MEAs) with the same FET or different FETs with the same electrode and might therefore give an indication for device scaling. Additionally, this has enabled to use the identical devices, i.e. the identical GOS MISHEMTs discussed in chapter 3 and the identical electrodes discussed in chapter 5, for the analysis presented in the following.

It is worth remembering that V_{GS} is not directly applied at the gate terminal, but at the Pt counter electrode and includes the potential drop at the BDD/electrolyte interface and therefore will reveal information on the pH sensitivity of the system (see figure 6.1). The applied voltage V_{GS} in reference to SCE was recorded using an additional electrometer. In contrast, the drain-source potential was directly applied at the respective HEMT terminals. For the measurements the electrodes were immersed in electrolytes corresponding to $pH = 1$ or $pH = 13$.

6.4.1 ISFETs with Planar Electrodes and InAlN/GaN MISHEMTs

Initially, the combination of the InAlN/GaN MISHEMTs and a large area $200 \times 200 \mu m^2$ BDD electrode shall be discussed. The easiest way to access the pH response of the system is to analyze its transfer characteristics. Thus, the linear transfer characteristics of the system in $pH = 1$ and $pH = 13$ are shown in figure 6.12. For comparisons, the transfer characteristic of the MISHEMT alone is also shown in the figure. The gate-width was $W_G = 25 \mu m$ and the drain-source voltage was $V_{DS} = 6 V$. As expected, the two curves in $pH = 1$ and $pH = 13$ are parallel shifted, in this case by $\Delta V = 0.67 V$ (extracted at $I_{DS} = 0.05 A/mm$). This corresponds to a pH-sensitivity of $\Delta V/pH = 51 mV/pH$, close to that predicted by equation (5.2) and to that obtained in section 5.3. Compared to the MISHEMT alone the two curves are also parallel shifted. However, a close look reveals that the transconductance g_m is slightly reduced in the hybrid configuration. This arises from the additional capacitance at the BDD/electrolyte interface (C_{par}) and its influence on the modulation of charges in the 2DEG (compare equations (6.8) and (6.9)). Of special interest for an ISFET is the dependency of the output current density on changes of the pH ($= \frac{\Delta I_{DS}}{\Delta pH}$), which is comparable to the transconductance of the FET ($g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}}$). Here, this yields a value of $\Delta I_{DS}/\Delta pH \approx 5.9 \frac{mA}{mm \cdot pH}$ (V_{GS} vs. SCE = 0.5 V). Due to its transconductance of $g_m > 0.1 S$ this value is already several orders of magnitude larger compared to what is reported for other ISFET technologies, like the single crystalline diamond ISFET [140], the AlGaIn/GaN and InAlN/GaN heterostructure ISFET [141, 142] and even for the Si-based extended gate ISFET [125, 126, 143].

The gate leakage current of the 200 nm GaN + 50 nm AlN sample was nearly independent of the gate-width. Thus, the parameter changing with the gate width is the gate-source capacitance C_{GS} . According to figure 6.10 the full transconductance may be

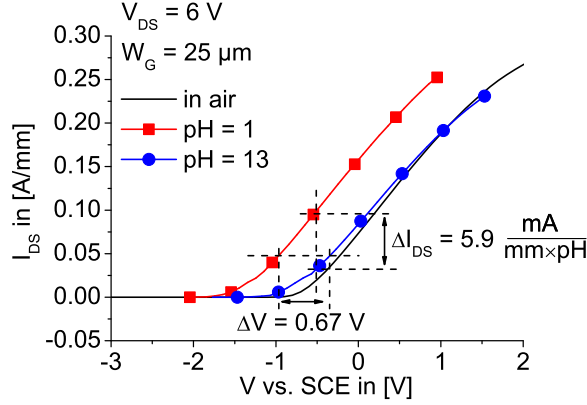


Figure 6.12: Depiction of the transfer characteristics of the hybrid system in pH = 1 (red squares) and pH = 13 (blue circles). The drain-source voltage was $V_{DS} = 6$ V and the gate-width $W_G = 25$ μm . The black line (without symbols) shows the curve of the MISHEMT alone.

available, even if the electrode is connected to wider MISHEMTs. Indeed, similar behavior is observed, when connecting the electrode to FETs with larger W_G . The results obtained for the different combinations are summarized in figure 6.13. The corresponding transfer characteristics are provided in appendix F. The resulting voltage shift, also extracted at $I_{DS} = 0.05$ A/mm, is independent of the gate-width and is $\Delta V = 0.67$ V again correlating to a pH sensitivity of 51 mV/pH. This is expected, since this pH dependency arises from the BDD electrode, which is identical in all cases (same electrode). In contrast, the change of the output current density extracted at V_{GS} vs. SCE = 0.5 V varies between $\Delta I_{DS} \approx 80$ mA/mm and $\Delta I_{DS} \approx 60$ mA/mm decreasing with increasing gate width, which in this case is mainly ascribed to the characteristics of the individual MISHEMTs (mainly g_m) and not to a significant influence of the electrode capacitance ($C_{par} \gg C_{GS}$ for all W_G). In average, the pH sensitivity of the output current density is approximately $5 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$.

The extracted quantities of the pH sensitivity were obtained by simple linear interpolation between the curves recorded in pH = 1 and pH = 13 electrolytes. However, it may not be valid to simply assume a completely linear response within the whole pH range. Therefore an experiment was conducted resolving the pH response around the neutral pH regime. In this experiment the change of I_{DS} , caused by a change of the pH value, is monitored under constant bias conditions over a time period of 60 minutes. This means that the drain-source voltage was kept at $V_{DS} = 6$ V and the gate-source voltage at $V_{GS} = 0$ V vs. SCE. Since the potential V_{GS} vs. SCE cannot be applied directly, but is monitored with an electrometer, the applied gate-source potential was adjusted accordingly (manually). The measurement started in 0.1 M KCl electrolyte (here: pH = 6). The pH value of the electrolyte was gradually increased by adding traces of a KOH solution using a pipette. The same amount of KOH was also added in a reference beaker of the KCl electrolyte, from which the resulting pH value was measured using a commercial

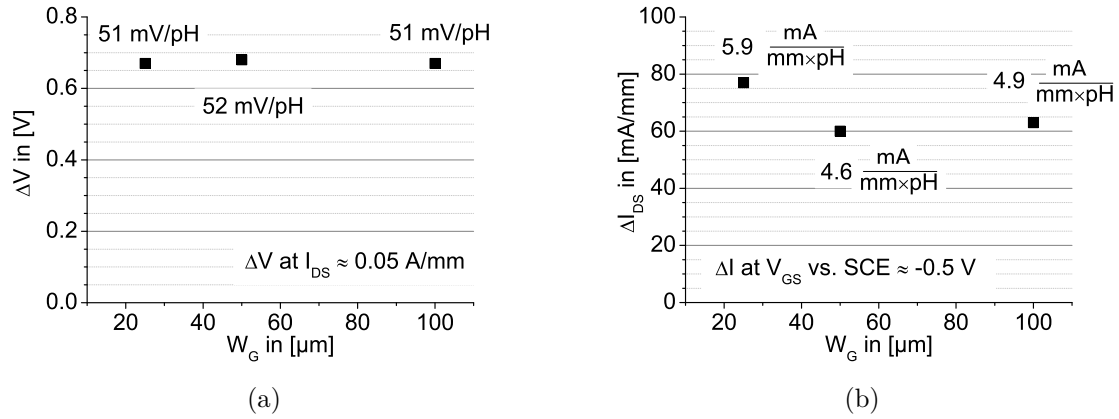


Figure 6.13: (a) Voltage shift ΔV between the curves in pH = 1 and pH = 13 for the combination of a large area electrode and MISHEMTs with different gate-width W_G . The shift was extracted at constant current density of $I_{DS} = 0.05 \text{ A/mm}$. (b) The corresponding shift in the output current density I_{DS} , extracted at a constant V_{GS} vs. SCE = -0.5 V vs. SCE.

pH-meter. The results of this experiment are summarized in figure 6.14, where figure 6.14(a) shows the change of I_{DS} with measurement duration and figure 6.14(b) shows the corresponding pH sensitivity. The drain current at each pH plateau remains constant during the respective time interval. Only in the beginning of each interval a sharp decrease of the current is observed. This is related to the insertion of KOH droplets as well as to the time needed to adjust the gate-source voltage to $V_{GS} = 0 \text{ V}$ vs. SCE. The resulting output currents are plotted against the measured pH value in figure 6.14(b). This figure shows also the current obtained from the linear transfer characteristics in pH = 1 and pH = 13 (see figure 6.12) at the same bias conditions. Indeed, together the points follow a linear relation describing the pH response of the whole ISFET system yielding $\frac{\Delta I_{DS}}{\Delta \text{pH}} = 4.9 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$, which is close to the value extracted above, thus speaking for high linearity of the pH sensitivity over the whole pH scale. Neglecting the observed current spikes at the beginning of each pH plateau the achievable pH resolution can be calculated according to

$$\Delta \text{pH} = \frac{\Delta I_{DS}|_{\text{pH}=\text{const.}}}{\Delta I_{DS}/\Delta \text{pH}} \quad (6.11)$$

and yields a pH resolution up to $\Delta \text{pH} \approx 0.04 \text{ pH}$.

As mentioned in section 6.2, for certain applications it might be necessary to avoid heat generation. Thus, making use of the extremely low currents available in the subthreshold regime of the InAlN/GaN MISHEMT seems attractive. The selected FETs exhibit a pinch-off voltage, i.e. the voltage where the current reaches a constant plateau, of $V_{\text{off}} = -1.7 \text{ V}$, which lies within the potential window of the BDD electrode. Their corresponding off-currents are in the lower pA regime. Thus, low output current densities could be obtained by driving the devices into the subthreshold regime. These

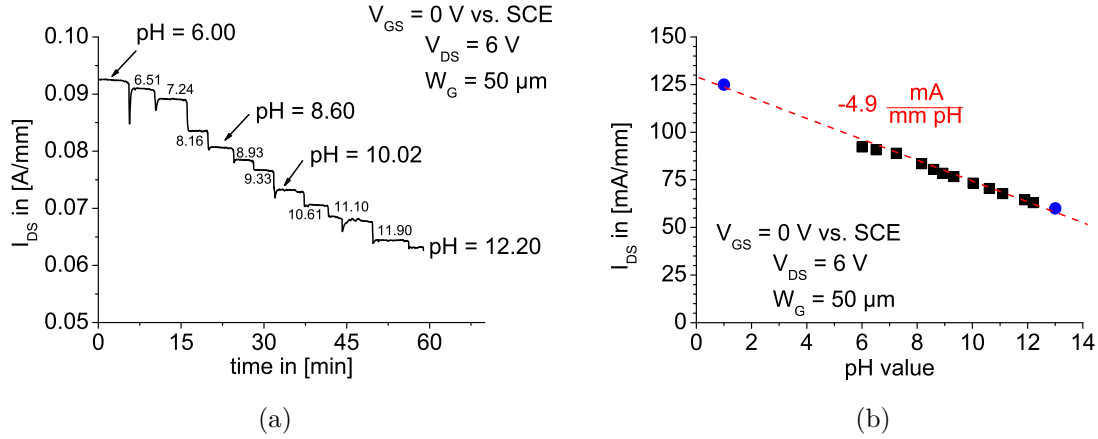


Figure 6.14: (a) I_{DS} monitored with time. The numbers present the pH value read from a pH-meter. (b) Change of I_{DS} with the pH value (extracted from (a)), exhibiting a nearly linear response of $4.9 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$. The measurement was done at $V_{DS} = 6$ V and $V_{GS} = 0$ V vs. SCE. The blue circles present values obtained from the linear transfer characteristics in pH = 1 and pH = 13 under the same bias conditions. The measurements were done and provided by C. Pietzka and Z. Gao.

devices therefore give an insight into the pH response in this bias regime. The transfer characteristics of figure 6.12 is shown in figure 6.15(a) in semilogarithmic representation. The other two semilogarithmic transfer characteristics (wider gates) are also provided in the appendix F. In contrast to the linear representation the difference between the curve at pH = 13 and the curve of the MISHEMT alone becomes more significant. This shift is observed in all three combinations and prohibits complete pinch-off (within the potential window). However, the shift is $\Delta V(\text{air} \rightarrow \text{pH} = 13) \approx 0.5$ V for the 25 μ m and 100 μ m wide devices and only $\Delta V(\text{air} \rightarrow \text{pH} = 13) \approx 0.2$ V for the 50 μ m wide device. A possible explanation for this phenomenon may be the slightly different leakage currents of the individual devices, which were approximately 11 pA for the 25 μ m and 100 μ m wide devices and approximately 5 pA for 50 μ m wide device (compare as well figure 3.12). Then, in accordance with equation (6.4), this would again point out the necessity of having precise control over the leakage behavior, here especially the gate leakage properties. In order to avoid failure of the measurement setup due to H_2/O_2 evolution at the Pt counter or the reference electrode, the gate-source voltage was limited to the potential window. Hence, the evaluation of the pH dependence in the subthreshold regime is limited to -1.7 V. However, due to the mentioned shift of the transfer characteristics complete pinch-off is not possible. As a consequence currents below the nA regime cannot be accessed. Nevertheless, the change of I_{DS} for the three combinations is shown in figure 6.15(b). Due to the exponential behavior in this regime the relative change is extremely large and the current increases more than 4 orders of magnitude in case of the 25 μ m and 50 μ m wide MISHEMTs and more than 3 orders of magnitude in case of the 100 μ m wide HEMT. In reference to the subthreshold swing SS (in [mV/dec]) the exact changes correspond to a pH dependent SS of 3.2 pH/dec, 3.1 pH/dec and 4.3 pH/dec

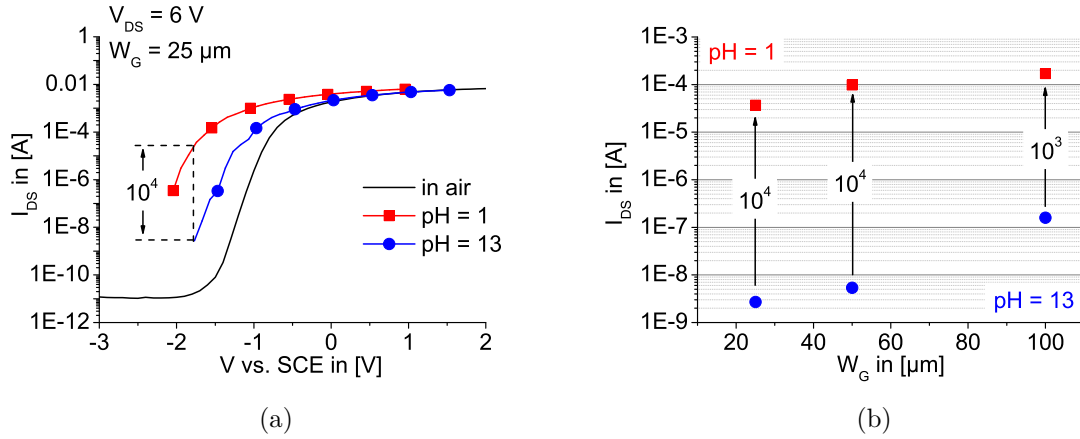


Figure 6.15: (a) Transfer characteristics of the system in pH = 1 (red squares) and pH = 13 (blue circles) in semilogarithmic scale. The solid black line is the curve of the HEMT alone. (b) Exponential change of I_{DS} from pH = 1 to pH = 13 in the subthreshold regime for different W_G .

for $W_G = 25 \mu\text{m}$, $W_G = 50 \mu\text{m}$, and $W_G = 100 \mu\text{m}$, respectively. In other words, in these first experiments the output current would potentially double for a change in the pH of $\Delta\text{pH} = -1$. However, this value is still limited by the extrapolation method, where the exponential dependency at the point of extrapolation $V_{GS} = -1.7 \text{ V}$ cannot be applied for the curve in pH = 1. Nonetheless, these first experiments indicate that an exploitation of the HEMT subthreshold regime is feasible, although further reduction of the gate leakage currents may be required.

6.4.2 ISFETs Comprising MEAs and InAlN/GaN MISHEMTs

Substituting the large area BDD electrode by a microelectrode array in the ISFET measurement configuration basically means that the total active capacitance of the electrode will be reduced (from 200 pF to approx. 30 pF, if dominated by parasitic capacitances, or to 2 pF, if the intrinsic capacitance applies), thus may give an indication for electrode down scaling as would be required for the development of a highly integrated sensor system. According to the findings in section 6.2.2 (see figure 6.10), rather good FET modulation seems still possible, even if a MEA is connected to the gate terminal. Since the different MEAs resulted in similar CV characteristics, it may be sufficient to discuss only one MEA structure in combination with the InAlN/GaN HEMTs. Thus, for the following discussion the MEA with 1600 microelectrodes ($r = 0.25 \mu\text{m}$) was selected. The resulting linear transfer characteristics for the combination of the MEA and MISHEMTs with $W_G = 25 \mu\text{m}$, $W_G = 50 \mu\text{m}$, and $W_G = 100 \mu\text{m}$ in pH = 1 and pH = 13 are summarized in figure 6.16. The drain-source voltage was again $V_{DS} = 6 \text{ V}$. The curves are again compared to the characteristics of the HEMT alone. Although

acceptable modulation efficiency is achieved for all device combinations, compared to the combination with a large area electrode there are some significant deteriorations in the transfer characteristics. First, the curves in $\text{pH} = 1$ and $\text{pH} = 13$ are not parallel. Second, the resulting slopes of the curves in the electrolyte are significantly reduced, also associated by a shift of the threshold voltage V_{th} . While the decreased extrinsic transconductance of the ISFET could be explained by a very small capacitance of the MEA, the shift of the threshold voltage can only be explained by a parallel resistance R_{par} of the MEA much larger than that of the large area electrode (which was indicated in section 5.3, compare figures 5.11 and 5.14), thus a decreased voltage drop at the metal gate ($V_{\text{GS,HEMT}}$). Furthermore, the measurements were not easily reproducible and generally suffered from more signal distortion and noise, which certainly arises from the hybrid integrated system in combination with the very high impedances involved. Especially the problematic reproducibility may be the reason for the non-parallel curves. Due to the shift of the threshold voltage to $V_{\text{th}} \approx -2.0 \text{ V}$ ($\text{pH} = 1$) and $V_{\text{th}} \approx -1.5 \text{ V}$ ($\text{pH} = 13$) the subthreshold regime cannot be analyzed, because lower V_{GS} vs. SCE correspond to potential regimes outside the BDD potential window.

Since the two curves at $\text{pH} = 1$ and $\text{pH} = 13$ are not in parallel, an evaluation of the measurements can produce diverse results, which is why an interpretation of the results is difficult. Nevertheless, the extracted voltage shift ΔV and the change of the output current density ΔI_{DS} are shown in figure 6.17(a) and 6.17(b), respectively. In order to provide comparability between the measurements using the large area electrode and those using the MEA, the same conditions were chosen for parameter extraction. This means that ΔV was extracted at an output current density of $I_{\text{DS}} = 0.05 \text{ A/mm}$ and ΔI_{DS} at a gate-source voltage of $V_{\text{GS}} = 0 \text{ V}$ vs. SCE. In case of the $25 \mu\text{m}$ wide HEMT the voltage shift corresponds to a pH sensitivity of 50 mV/pH , which is close to that obtained for the $200 \times 200 \mu\text{m}^2$, but is decreasing with increasing gate width to 38 mV/pH ($W_{\text{G}} = 100 \mu\text{m}$). Similar behavior is observed for the change of the output current density, where $\frac{\Delta I_{\text{DS}}}{\Delta \text{pH}}$ decreases from $5.3 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$ to $4.2 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$, which is still above the $0.5 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$ reported for Si-based ISFETs [125, 126, 143]. Although the exact values may be insignificant, this trend of decreasing pH response with increasing gate-width strongly suggests that the drop of the extrinsic transconductance is related to a mismatch between the HEMT input circuit and the BDD circuit. In other words, this means that the voltage drop at the gate $V_{\text{GS,HEMT}}$ does not compare to the applied potential V_{GS} . Thus, exploiting the full HEMT transconductance and full modulation efficiency in combination with a MEA may be achievable by further HEMT device downscaling. Even though InAlN/GaN HEMTs with a sub-micrometer gate-width were already demonstrated in literature [137], a prerequisite to benefit from such scaled devices is monolithic integration.

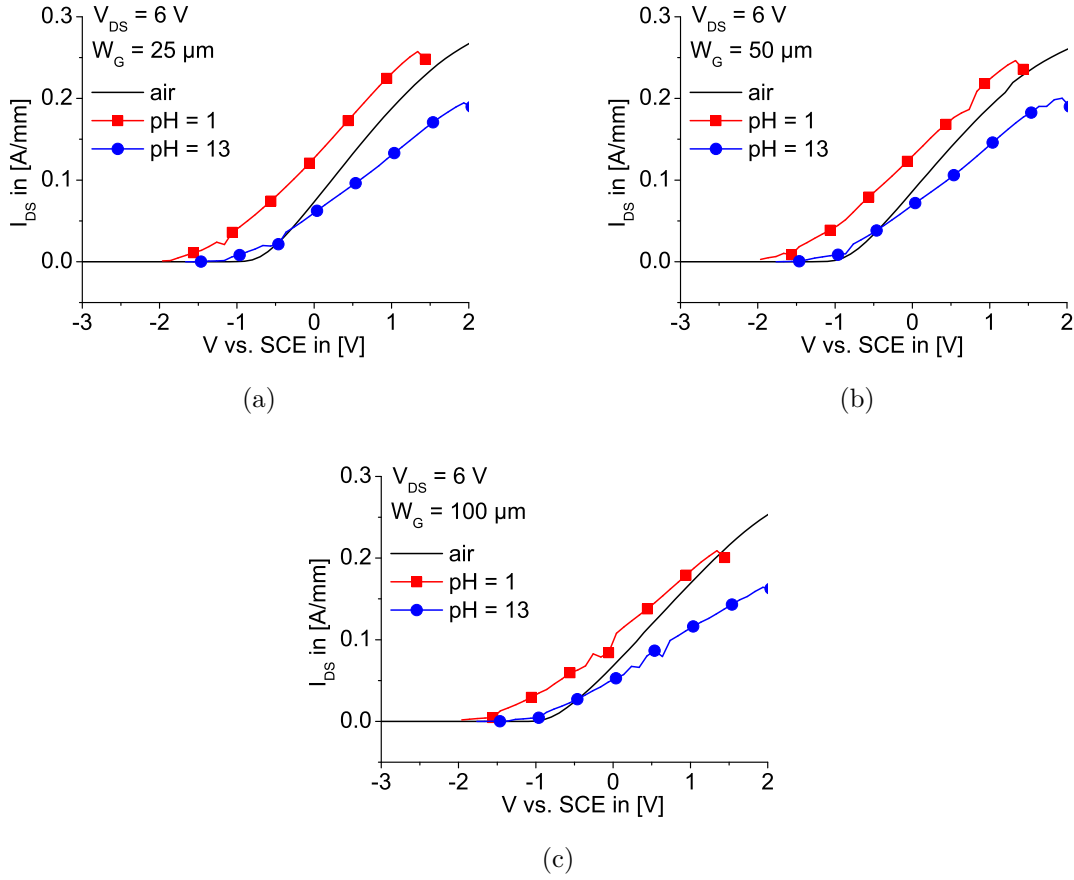


Figure 6.16: Linear transfer characteristics of the MEA combined to the gate of an InAlN/GaN HEMT with (a) $W_G = 25 \mu\text{m}$, (b) $W_G = 50 \mu\text{m}$, and (c) $W_G = 100 \mu\text{m}$ wide InAlN/GaN HEMT. The black line (without symbols) is the transfer characteristics of the HEMT, the red line with squares are the curves in pH = 1, and the blue line with circles are curves in pH = 13.

6.5 Using InAlN/GaN MISHEMTs as Electrode Switch

With its off-current I_{off} in the lower pA regime and the rather steep subthreshold swing of $SS = 82 \text{ mV/dec}$, the 200 nm GaN sample is also a good choice for the application in the switch configuration. As mentioned above, for those measurements the BDD electrode is connected to the drain terminal of the HEMT, which means that the drain-source voltage V_{DS} is applied at the Pt counter electrode, whereas here the gate-source voltage is applied directly at the gate. In contrast to ISFET measurements, measurements in the switch configuration are related to the detection of electrode signal currents depending on the electrode potential (here, the drain-source potential versus SCE) and on the concentration of the investigated species in the electrolyte.

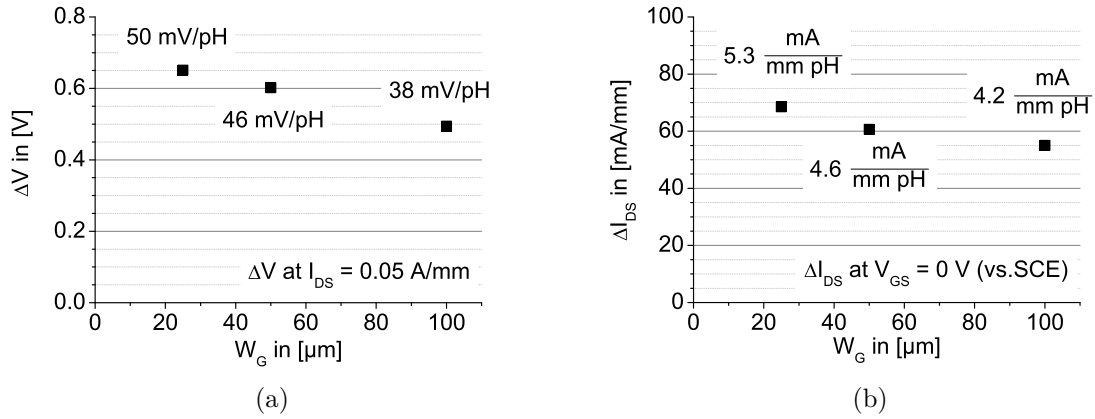


Figure 6.17: (a) Voltage shift ΔV vs. gate-width W_G extracted at a constant current density of $I_{DS} = 0.05 \text{ A/mm}$. (b) Current shift ΔI_{DS} vs. W_G extracted at $V_{GS} = 0 \text{ V}$ vs. SCE.

The measurement conditions were already given in section 6.3, but shall briefly be summarized again. The electrolyte consisted of a 0.1 M KCl solution in which $\text{Ru}(\text{NH}_3)_6^{2+}$ molecules with a concentration of $0.1 \frac{\text{mMol}}{\text{l}}$ were dissolved. The drain-source voltage is limited to the potential window and $V_{DS} = 1 \text{ V}$ vs. SCE was chosen for all measurements presented in the following. This voltage assures also that the electrode current is limited by diffusion and not by the reaction kinetics. The measurement setup was prepared as illustrated in figure 6.1. Thus, in contrast to the discussion of the requirements, here the resulting current was monitored (instead of the output voltage establishing at the HEMT drain terminal), which reduces the measurement efforts. However, the requirements remain identical to those discussed earlier. In consequence, the switch characteristics will be discussed in terms of transfer characteristics, where in on-state the current is limited by the electrode signal current and in off-state it is limited by the MISHEMT.

Discussed in more detail is the switching behavior of a $25 \mu\text{m}$ wide HEMT in combination with the planar $200 \times 200 \mu\text{m}^2$ electrode and with the MEA with 400 microelectrodes with $r = 0.5 \mu\text{m}$. The recorded linear transfer characteristics are presented in figure 6.18. The gate-source voltage was swept from $V_{GS} = -2 \text{ V}$ to $V_{GS} = 1 \text{ V}$ (switching on) as well as vice versa (switching off). In this experiment the pixel can already be considered "on" for $V_{on} \geq -1.2 \text{ V}$ and completely "off" at $V_{off} \leq -1.4 \text{ V}$. Thus, the transition from on to off is within a very narrow window of only 0.2 V and confirms the results of the switch characteristic of figure 6.11(b). This is of special interest for the envisaged application in an electrode array, where dynamic losses may become important. If higher concentrations of the $\text{Ru}(\text{NH}_3)_6^{2+}$ were investigated, the on-voltage would, of course, shift to more positive V_{GS} . However, due to the steep subthreshold swing of 82 mV/dec the shift would still be below +0.1 V even if the concentration is increased by one order of magnitude. At gate voltages lower than -1.2 V the output current is limited by the FET. At larger gate voltages the current is limited by the electrode or,

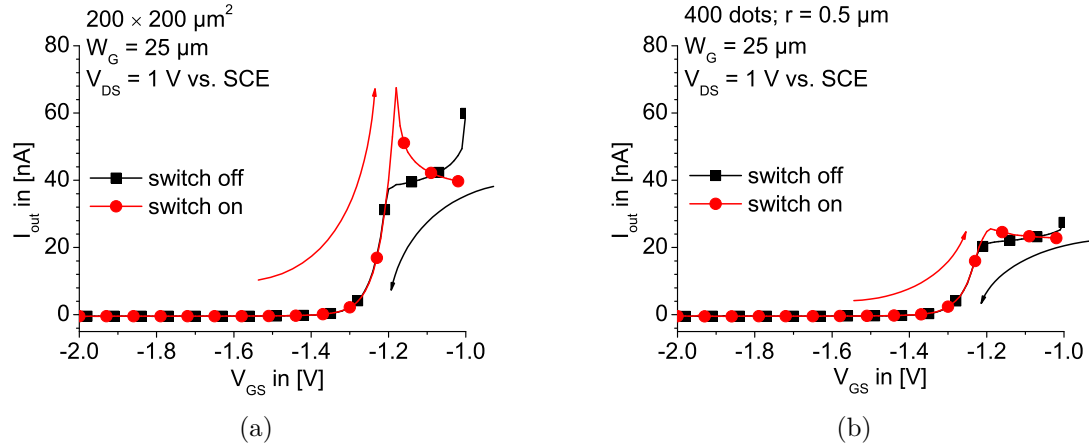


Figure 6.18: Linear transfer characteristics at $V_{DS} = 1$ vs. SCE with (a) a large electrode and (b) a MEA connected to the drain. Black squares indicate the switch-off and the red circles the switch-on behavior.

to be more precise, by the diffusion of reduced species towards the active BDD surface. While the switch-on and switch-off curves of both figures are identical for $V_{GS} \leq -1.2$ V, the curves show different behavior beyond this voltage, which is due to the influence of diffusion. As expected this influence is reduced for the MEA structure. The resulting peak currents are $I_{out} \approx 68$ nA and $I_{out} \approx 25$ nA using the large electrode and MEA, respectively. Both current levels are comparable to that obtained for the reduction peak under similar conditions by cyclic voltammetry at a scan rate of $s = 200$ mV/s (compare figure 5.15(b) in section 5.4). This is only expected for the microelectrode array, but is a coincidence in case of the large area electrode. The reason is that the diffusion limited current of MEAs are nearly independent of the elapsed measurement time (= scan rate in cyclic voltammetry), but it is strongly dependent on measurement duration for planar large electrodes (see equations (5.5) and (5.6)). Since the scan rate in this experiment is unknown, the use of MEAs is strongly recommended in switching applications, since they potentially produce a current plateau, which may significantly simplify data handling for a subsequent read-out electronics. However, in this experiment even the MEA structure exhibits a certain reduction of the electrode current in its on-state, which might be linked to the recessed electrode structure and its aspect ratio $2r/t_{cap}$. A similar behavior was already observed during the characterization of the MEAs in section 5.4.

Another, maybe more intuitive way to present the above results is to monitor the output current I_{out} in response to changes of the gate-source voltage V_{GS} . Here this means, instead of sweeping the gate voltage it is set to a constant, but varying potential. To maintain comparable conditions the drain-source voltage was again set to $V_{DS} = 1$ V vs. SCE. The results of such experiments are shown in figure 6.19, where the output current was recorded every second over a period of approximately three minutes. Within this resolution the response of I_{out} is immediate, meaning that the pixel is completely

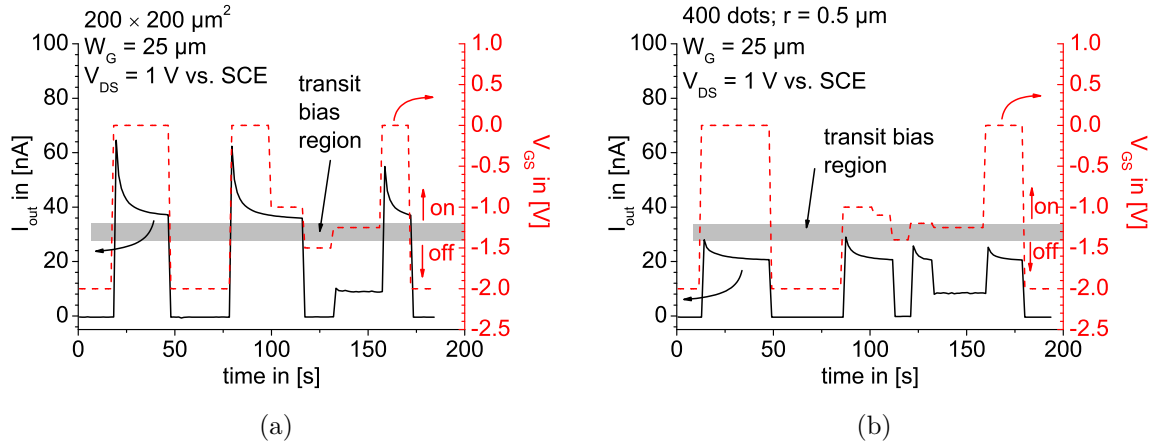


Figure 6.19: Switching experiments in combination with (a) the large area electrode and (b) the MEA. The drain voltage was $V_{DS} = 1 \text{ V}$. The solid black lines present the output current I_{out} (left axis) and the red dashed lines the applied gate voltage V_{GS} (right axis). The gray areas mark the bias regime between on- and off-state.

on or off in the moment the gate voltage is adjusted to the on- ($V_{GS} \geq -1.2 \text{ V}$) or off-state ($V_{GS} \leq -1.4 \text{ V}$). Again, the influence of diffusion is visible for each switch-on sequence and for both electrode types, but again more pronounced in case of the $200 \times 200 \mu\text{m}^2$ electrode. Nevertheless, in this figure also the peak of the MEA appears to be more pronounced compared to figure 6.18(b). This difference arises from the measurement procedure. While the whole characteristics of figure 6.18(b) was recorded within a period of less than two seconds, the current decreased further with measurement duration in figure 6.19(b).

7 Closing Remarks

7.1 Summary and Conclusions

This work was dedicated to the development of a GaN HEMT device technology with low overall device leakage currents prepared for the use in high-temperature electronics as well as for the integration with diamond sensors for electrochemical applications. Inspired by the silicon-on-insulator technology a comparable device technology was developed for GaN-based HEMTs. Used in this work was the lattice-matched InAlN/GaN heterostructure system, grown on sapphire substrate, thus leading to a GaN-on-Sapphire HEMT technology. In this technology, the following three key features can be identified, which led to a dramatic reduction of the overall device leakage currents down to the lower pA regime:

- Surface oxidation of the InAlN barrier
- Deep mesa isolation on sapphire substrate
- Downscaling of the GaN/AlN buffer configuration

Each of these three listed processes addresses the reduction or elimination of a particular leakage current. The two-minute oxidation process creates a native InAlN oxide with high crystalline order basically leading to a MISHEMT structure. This leads to a reduction of gate leakage currents by (at least) four orders of magnitude. Deep mesa isolation down to sapphire confines the heterostructure to the active device region and allows to position the contact pads and wiring directly on the highly insulating sapphire substrate. This eliminates leakage currents outside the active device and enhances inter device isolation by exploiting the high isolation properties of the sapphire. A rather surprising outcome of this work is that an aggressive downscaling of the GaN/AlN buffer configuration can significantly reduce residual buffer leakage.

In combination, such technological implementations led to thin body InAlN/GaN MISHEMTs with interesting device properties. In this work, the buffer layer system was successfully scaled to a total thickness of 100 nm (50 nm GaN buffer + 50 nm AlN nucleation layer) leading to a double heterostructure system, where only slightly degraded

2DEG properties ($\mu_{\text{el}} = 1100 \text{ cm}^2/\text{Vs}$, $N_{\text{S}} = 1.4 \times 10^{13} \text{ cm}^{-2}$ with $t_{\text{InAlN}} = 5 \text{ nm}$) were observed compared to a conventional material system, however with improved carrier confinement in the channel. Such thin body GOS MISHEMTs exhibited a peak output current density of $I_{\text{max}} \approx 0.4 \text{ A/mm}$, a steep subthreshold swing of $SS = 73 \text{ mV/dec}$, and an extremely low off-current of $I_{\text{off}} \approx 1 \text{ pA}$, thus a high current on/off ratio larger than 10^{10} . Such subthreshold characteristics (SS , $I_{\text{off}} \Rightarrow$ current on/off ratio) are the best obtained in this work. Of special interest might be that, independent of the gate-width, the resulting off-current was around 1 pA , which may provide a high degree of freedom for device and/or circuit design. The limited output current density is mainly ascribed to the lack of surface passivation. Thus, despite the thin buffer configuration a proper surface passivation scheme, like in-situ SiN , combined with a more advanced device fabrication (e.g. selective growth of Ohmic contacts) might also lead to further enhanced output characteristics.

A first application of such thin body GOS MISHEMTs was discussed within the frame of high-temperature electronics. Changes of the 2DEG properties, the DC output, and the subthreshold characteristics were monitored up to a temperature of $600 \text{ }^\circ\text{C}$. This was complemented by an analysis of the high-temperature performance under large-signal class A operation at 1 MHz . During these experiments different behavior was observed depending on the ambient conditions, i.e. experiments conducted in vacuum or in atmosphere. A non-permanent reversible degradation of the FET characteristics was observed in atmosphere (up to $300 \text{ }^\circ\text{C}$). Therefore, this degradation is mainly ascribed to adsorbates on the free, unpassivated InAlN surface. In vacuum, the electron mobility was reduced from 1100 Vs/cm^2 (RT) to 550 Vs/cm^2 ($600 \text{ }^\circ\text{C}$) following a $T^{-3/2}$ law as predicted for phonon scattering. A constant threshold voltage indicated the absence of pyroelectric effects suggesting a constant carrier concentration in the channel. Although the on-resistance was degraded (in accordance with the reduction of μ_{el}), a nearly constant peak current density up to $600 \text{ }^\circ\text{C}$ was observed. The observed reduction ($I_{\text{max}} = 0.38 \text{ A/mm} \rightarrow I_{\text{max}} = 0.35 \text{ A/mm}$) corresponds to a change of only 8% , from which it may be concluded that the FET operation at $600 \text{ }^\circ\text{C}$ was still dominated by the electron saturation velocity. Parasitic leakage at $600 \text{ }^\circ\text{C}$ was still below 20 nA leading to an extremely high (at this temperature) current on/off ration of approximately 10^6 . From a first evaluation of the off-currents at different temperatures two different activation energies can be extracted, one between RT and $300 \text{ }^\circ\text{C}$ ($E_{\text{A}} = 0.15 \text{ eV}$) and another between $300 \text{ }^\circ\text{C}$ and $600 \text{ }^\circ\text{C}$ ($E_{\text{A}} = 1.1 \text{ eV}$). The absence of high-temperature degradation was further confirmed by long-term large-signal class A measurements at $600 \text{ }^\circ\text{C}$ and at 1 MHz . The V_{GS} swing covered the full range of FET modulation, i.e. from fully open channel to below threshold. Although the resulting output current swing was already distorted due to a significant leakage current accross the gate diode, a stable mean current density $I_{\text{DS,mean}} = 0.18 \text{ A/mm}$ and output power of $P_{\text{out}} = 109 \text{ mW/mm}$ (at $V_{\text{DS}} = 10 \text{ V}$, $R_{\text{L}} = 120 \text{ }\Omega$) was observed. These results indicate that high-temperature electronics with nearly unchanged characteristics are feasible at temperature regimes that are usually the domain of electro-ceramics, but with significantly improved device characteristics.

The second application of the thin body GOS MISHEMT discussed was in combination with a BDD electrode for the development of a electrochemical sensor system ready for both, amperometric and potentiometric measurements. In essence, this presents a combination of two individual building blocks, where the electrode serves as the actual electrochemical sensor and the FET as transducer (ISFET) or electronic switch, which is used to read-out either the potential drop (pH measurements) or the electrode current at the BDD electrode. Therefore, initially the electrochemical properties, i.e. the pH-sensitivity (58 mV/pH), background current (≈ 0.1 nA), potential window (2.8 V), and the response to the $\text{Ru}(\text{NH}_3)_6^{2+/3+}$ redox system, were identified using different, individual electrode structures (planar electrode and MEAs). Of high relevance in the ISFET configuration is also the equivalent circuit model of the BDD/electrolyte interface. It was shown that these results establish certain boundary conditions, which need to be matched by the FET. This helped to derive some FET design criteria and pointed out the importance of the GOS MISHEMT technology leading to low overall device leakage. As ISFET the full FET modulation range should be exploited, thus a $C_{\text{GS}} \ll C_{\text{par}}$ and $R_{\text{GS}} \gg R_{\text{par}}$ (low gate leakage) are desired. To match the potential window V_{th} should be in the range of -2 V. As electronic switch the FET must allow blocking of the electrode current, thus an I_{off} (much) smaller than the electrode current was needed. First results, here obtained on a hybrid integrated system, already exhibited a high, linear response of the output current on pH variations even as high as $\frac{\Delta I_{\text{ps}}}{\Delta \text{pH}} = 5.9 \frac{\text{mA}}{\text{mm} \cdot \text{pH}}$, exploiting the high modulation efficiency of the MISHEMT, and a very efficient switching of amperometric signals. Due to its steep subthreshold swing, the transition region between complete on and off was in a voltage range of only 200 mV. First investigations on the exploitation of the subthreshold regime for low power sensing applications resulted in a high pH sensitivity of 3.2 pH/dec, however, still limited by residual gate leakage. Since these two investigated combinations, i.e. the ISFET and the switch measurement configuration, present the two basic building blocks needed for highly integrated sensor arrays, the development of such sensor systems seems feasible using InAlN/GaN MISHEMTs and BDD electrodes.

A prerequisite for the development of such electrochemical sensor systems, possibly with high integration density and spatial resolution, certainly is the monolithic integration of the InAlN/GaN MISHEMT and the BDD electrode onto the same chip. Therefore, two integration strategies, the "GaN first" and "diamond first" approach were discussed in this work, where the former was already established and the latter was developed during this work. In the GaN first approach the fully fabricated FET needs to withstand the extremely harsh diamond growth conditions ($T > 750$ °C for several hours), which is why non-degraded FET leakage characteristics are not easily achievable. In contrast, the new diamond first integration method starts with the fabrication of the BDD electrodes and is then followed by the heterostructure growth and FET fabrication. Thus, this method eliminates the need of a high temperature stable device metalization and passivation, as well as concerns about a possible degradation of the FET leakage characteristics. The key enabling this technology was the preparation

of the sapphire surface to provide a perfectly smooth surface for the subsequent heterostructure growth process, which was also confirmed by the limited heterostructure growth onto the existing BDD electrodes. SEM analysis of the prepared sample indicated a high material quality and, indeed, HEMTs fabricated on this material showed excellent device characteristics. The output current density was $I_{\max} = 0.8$ A/mm and the transconductance was $g_m = 340$ mS/mm. However, the GOS MISHEMT technology was not yet fully implemented. Thus, the fabricated FETs could not satisfy the specific requirements established by the BDD electrode. However, the diamond first integration method is attractive, because it would generally allow the integration of diamond components with any other electronic material, which might be incompatible with diamond growth, but the technology has already matured (e.g. thin film transistors based on silicon). Thus, this integration method makes diamond components (not limited to BDD electrodes) available for other materials, which may lead to new device concepts. Nevertheless, diamond components and electronic circuitry must be integrated side by side using the diamond first approach, whereas in the GaN first approach the diamond components could be realized on top of the electronic material, thus allowing for a higher integration density. Moreover, the diamond first approach does generally not allow for an inert diamond passivation.

7.2 Device Scaling for the Future Perspective of Integrated Chemical Sensor System

For the development of highly integrated chemical sensors systems both elements, the BDD electrode and the InAlN/GaN FET, need to be scaled down in geometry. Therefore, in an individual experiment GOS MISHEMTs with a gate-width as low as $W_G = 2$ μm were fabricated (see figure 7.1(a)) on a heterostructure system with a 200 nm GaN buffer. Figure 7.1(b) shows both, the resulting maximum currents and the off-currents dependent on the gate-width W_G . I_{\max} scales with W_G resulting in a current density of 0.4 A/mm. In contrast, I_{off} is around 5 pA, nearly independent of the gate width, and probably limited by leakage currents arising from the much larger contact pads. Thus, this may be less problematic in an integrated system, since the wiring will also shrink.

Electrode scaling was achieved by an additional SU 8 epoxy passivation on the MEA with 400 microelectrodes ($r = 0.5$ μm). 4 individual microelectrodes (of the 400) were kept unpassivated and remained as active electrodes. Considering that the resulting electrode current of this MEA was 25 nA, means that a resulting current of 250 pA can be expected in the same electrolytic solution (1 mMol $\text{Ru}(\text{NH}_3)_6^{2+}$ dissolved in 0.1 M KCL). The cyclic voltammetry at a scan rate of $s = 20$ mV/s of the as-prepared electrode is shown in figure 7.2(a), where the electrode potential is already labeled as V_{DS} vs. SCE (prepared for switching experiments). The resulting electrode current is approximately

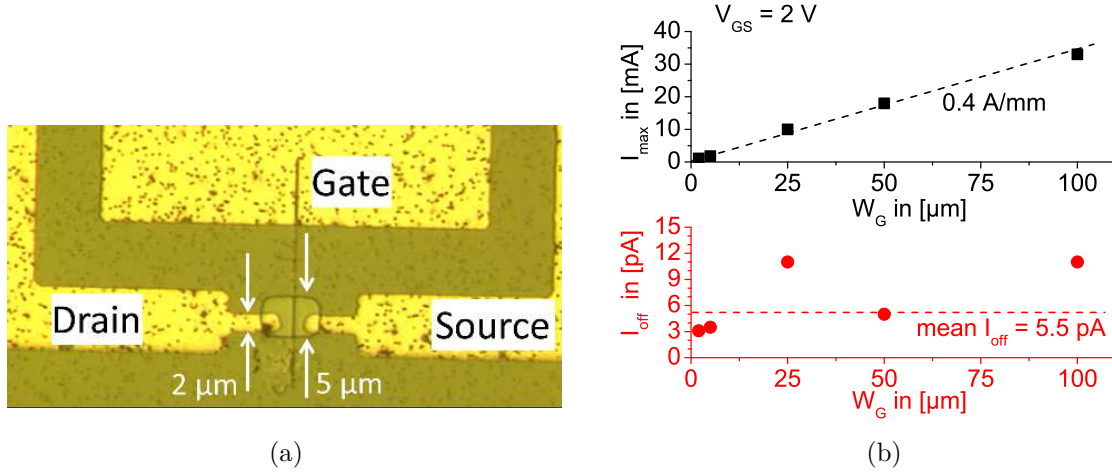


Figure 7.1: (a) Picture of a 2 μm wide MISHEMT. b) Change of I_{DS} (top) and I_{off} (bottom) in absolute current scale with gate-width W_G . W_G is between 2 μm and 100 μm .

260 pA and is in good agreement with expectations. Also, the properties of a MEA structure are maintained, which is confirmed by the evolution of a current plateau.

In a single experiment it was attempted to switch this low electrode current using a scaled GOS MISHEMT. Since the residual off-current of the FET is still 2 orders of magnitude lower than the electrode current, complete on and off switching should be possible. The result of a switch-on experiment, i.e. the linear transfer characteristics at $V_{\text{DS}} = 1$ V vs. SCE with a gate voltage sweep from $V_{\text{GS}} = -1.35$ V to $V_{\text{GS}} = -1.0$ V, is shown in figure 7.2(b). Obviously, the signal is severely distorted and suffers from a relatively high noise level, which is ascribed to the hybrid measurement setup. However, the slightly reduced on-voltage of $V_{\text{on}} = -1.28$ V is in line with what could be expected for smaller electrode currents. Furthermore, the calculated mean output current (for $V_{\text{GS}} = -1.25$ V to $V_{\text{GS}} = -1.0$ V) is 300 pA, which is rather close to the 260 pA obtained in cyclic voltammetry.

This experiment proves that the two elements for the development of a highly integrated sensor system consisting of BDD electrodes and InAlN/GaN FETs are already available today. However, such sensor systems require monolithic integration. Thus, the last remaining hurdle seems an integration technology, which is capable of producing InAlN/GaN FETs with leakage characteristics, which match to the specific boundary conditions established by the BDD electrode. Although it does not allow for an equally high integration density or a diamond passivation scheme, the "diamond first" approach seems a promising integration strategy, since it avoids subjecting the InAlN/GaN FET to the harsh diamond growth and already indicated promising device characteristics.

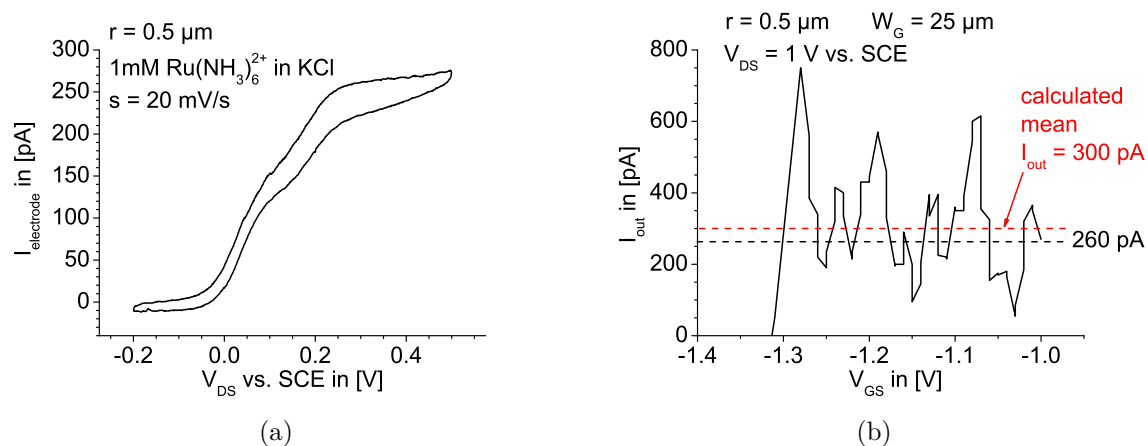


Figure 7.2: (a) Cyclic voltammetry at a scan rate of 20 mV/s of 4 microelectrodes. (b) Switch experiment presented by the linear transfer characteristics at $V_{\text{DS}} = 1 \text{ V vs. SCE}$. The black dashed line indicates the current obtained in (a) and the red dashed line presents the calculated mean I_{out} for $V_{\text{GS}} = -1.25 \text{ V} \dots -1.0 \text{ V}$. Measurements done in collaboration with C. Pietzka.

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A GaN-On-Sapphire HEMT Technology Recipes

Process parameters for the GOS MISHEMT fabrication technology

Reflow technique to define mesa geometry and slanted mesa sidewalls

- photo resist: AZ ECI 3027
- spin coating: 3000 rpm (\Rightarrow 3 μ m thickness)
- developing: 40 s in AZ 726 metal-ion free
- reflow bake: 60 s at 135 °C

Reactive Ion Etching (leading to vertical sidewalls without reflow technique)

- Ar/BCl₃/Cl₂ plasma: gas flow ratio: 5:8:2 sccm
- temperature substrate holder: 5 °C, chamber pressure: 15 mTorr
- power: 50 W (6 inch substrate holder); established DC self-bias: \approx 120 V
- resulting etch rate: 35 nm/min; resulting GaN/resist etch ratio: 1:1.6

Ohmic contacts (lift-off process)

- two layer resist process: LOR 7B and TI09
- spin coating: 4000 rpm and 8000 rpm; developing: 30 s in AZ 726 metal-ion free

- preparation prior deposition (surface cleaning): diluted HCl (70 °C - 80 °C, H₂O : HCl = 2 : 1)
- e-beam evaporation: Ti/Al/Ni (15/100/40 nm)
- contact alloying by RTA: 30 s at 800 °C in nitrogen atmosphere

Thermal oxidation in tube oven (prior gate formation)

- temperature: 800°C
- oxidation time: 2 min
- pure oxygen atmosphere: O₂-flow = 1000 sccm

Gate contacts (lift-off process patterned by e-beam lithography)

- two layer resist process: PMMA/MA and PMMA/MA 950K
- spin coating: 3000 rpm and 6000 rpm
- thermal evaporation: Cu (200 nm)
- e-beam evaporation: Pt (20 nm)

Re-metalization (lift-off process)

- two layer resist process: LOR 7B and TI09
- spin coating: 4000 rpm and 8000 rpm; developing: 30 s in AZ 726 metal-ion free
- thermal evaporation: Cu (200 nm)
- e-beam evaporation: Ti/Pt (10/20 nm)

B Additional Device Characteristics

B.1 Ohmic Contacts and Device Isolation

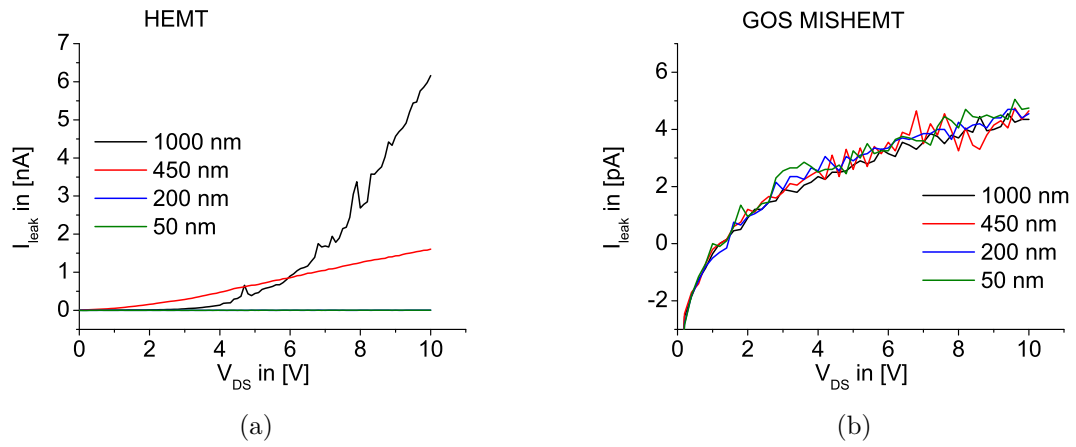


Figure B.1: Measurements of isolation currents for (a) HEMTs and (b) GOS MISHEMTs. Black: 1000 nm GaN, red: 450 nm GaN, blue: 200 nm GaN, and green: 50 nm GaN. The pad widths are 100 μm and the separation is 5 μm .

B.2 On-State Characteristics

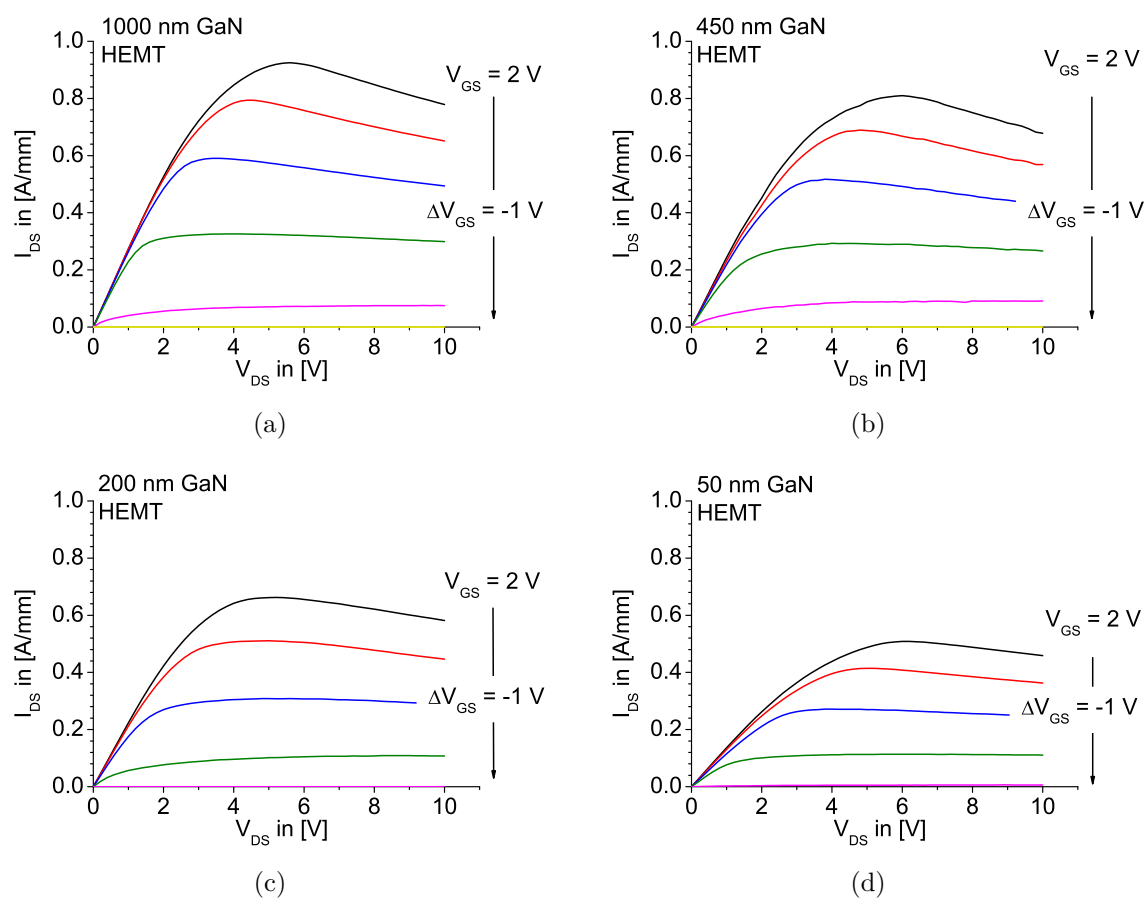


Figure B.2: Output characteristics of HEMTs processed in standard GaN technology. The GaN layer thicknesses are: (a) 1000 nm, (b) 450 nm, (c) 200 nm, and (d) 50 nm; The gate widths are 50 μm .

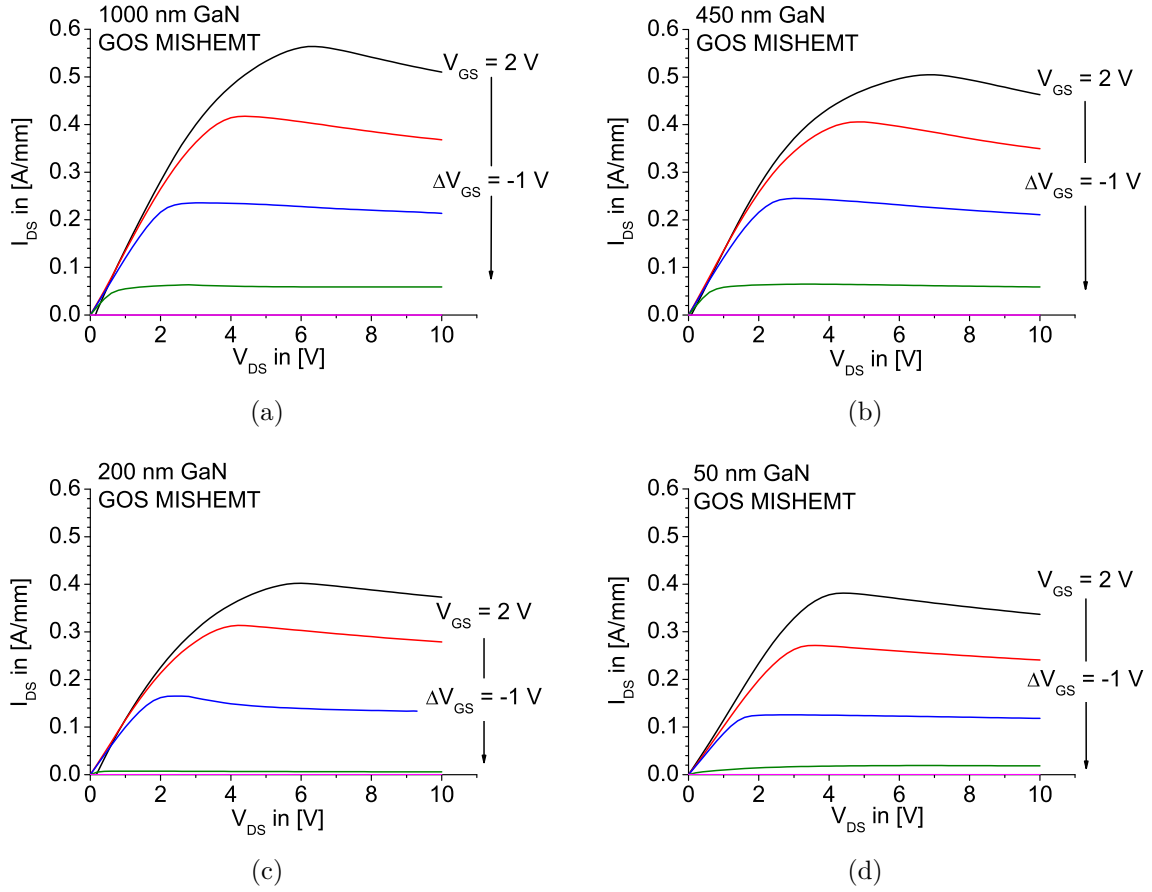


Figure B.3: Output characteristics of MISHEMTs processed following the GOS technology. The GaN layer thicknesses are: (a) 1000 nm, (b) 450 nm, (c) 200 nm, and (d) 50 nm; The gate widths are 50 μm .

C Additional Data for High-Temperature Operations

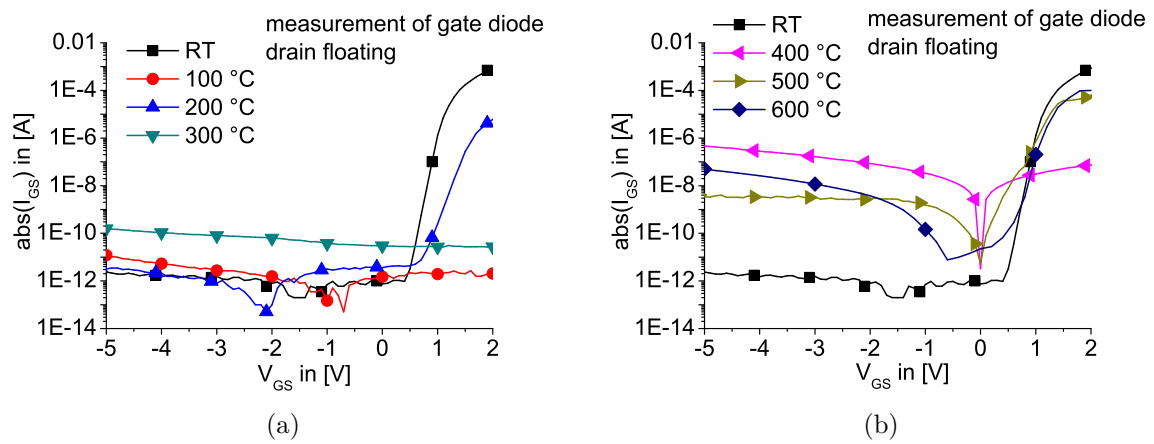


Figure C.1: Measurements of the gate diode at different temperatures in (a) atmosphere and in (b) vacuum.

D Introduction to Electrochemistry

One aim of this work is the design of an electrochemical sensor comprising an InAlN/GaN HEMT and a boron-doped diamond (BDD) electrode. In this work, the HEMT and the electrode are two individual devices, where the former solely serves as an amplifier or a switch and the latter is the actual electrochemical sensor being in contact with an electrolyte. In general, there are two different kinds of electrochemical measurements. One is related to the detection of potential changes depending on the electrolyte composition, e.g. pH value, and is referred to as potentiometric measurement. On the other hand, amperometric measurements are related to currents across the electrolyte/BDD interface caused by oxidation or reduction of molecules, and therefore are depending on the concentration of the detected species dissolved in the electrolyte. Below, the concept of an electrolyte as well as its pH value shall briefly be described. Also, the measurement setup itself and the different measurement concepts shall briefly be introduced with the example of BDD electrodes.

D.1 Electrolytes and Electrochemical Potential Scale

An electrolyte is here an aqueous solution in which mobile ions are dissolved. Because of autoprotolysis pure water itself can be considered an electrolyte. The water molecules (H_2O) continuously decompose into hydroxide ions (OH^-) and hydronium ions (H_3O^+). Simultaneously, hydroxide and hydronium ions react to form water thereby establishing an equilibrium of the H_2O molecules and the H_3O^+ and the OH^- ions in the solution. This behavior is described by the chemical equation (D.1).

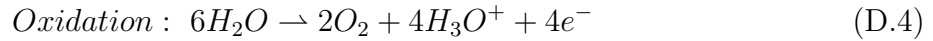
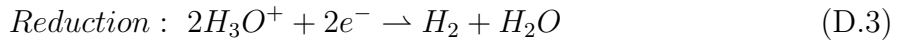


Evidently, there are as many hydronium ions as hydroxide ions available in the solution or, in other words, the H_3O^+ and the OH^- concentrations are equal ($c[H_3O^+] = c[OH^-] \approx 10^{-7}$). Hence, the ionic product of water (K_w), i.e. the product of both concentrations, is approximately $1 \times 10^{-14} \text{ mol}^2/\text{l}^2$ (at room temperature) [114]. The pH value of an aqueous solution can then be calculated after equation (D.2) and is in case of pure water $pH = 7$.

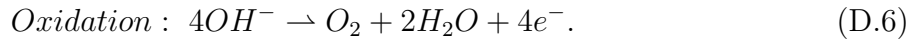
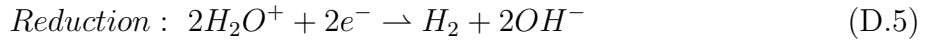
$$pH = -\log(c[H_3O^+]) \quad (D.2)$$

A solution is considered neutral, when its pH value is equal to 7. Through adding an acid (or base) to the electrolyte one can create a higher concentration of hydronium ions (or hydroxide ions) and the pH value will be $\text{pH} < 7$ ($\text{pH} > 7$).

Another way to dissociate water is the electrolysis where an anode and a cathode are brought in contact with the electrolyte. When a voltage larger than 1.23 V (1.48 V in experiments, [114]) is applied water decomposes and hydrogen gas is generated at the cathode and oxygen gas is generated at the anode. This voltage is also known as the stability window of water. The oxygen evolution is the oxidation reaction of water, the hydrogen evolution is the reduction reaction. The corresponding chemical reactions in acidic solutions are



and in basic solutions



Particularly interesting is the hydrogen evolution reaction in $\text{pH} = 0$ (equation (D.3)), because it defines the potential of the standard hydrogen electrode (SHE)¹. In electrochemistry all potentials are referred to SHE, which is defined to 0 V overpotential. Figure D.1 compares the electrochemical potential scale with the physical energy scale, which is commonly used in solid state physics. In physics, the absolute reference energy is the vacuum energy E_{vac} defined to 0 eV. The SHE lies approximately 4.4 V below the vacuum energy.

The individual reactions of the equations (D.3) to (D.6) occur at a certain electrode potential and are depending on the pH value. Therefore, the window of water stability in electrolytes of different pH is shifted (see figure D.1). The electrode potential E and the pH value are linked by the Nernst equation (simplified) [114]

$$E = E_0 + \frac{k_b T}{q} \ln(c[\text{H}_3\text{O}^+]) = E_0 - 2.303 \frac{k_b T}{q} \times \text{pH} \quad (\text{D.7})$$

where E_0 is the standard electrode potential, k_b is the Boltzmann constant, T the absolute temperature, q the elemental charge, and $c[\text{H}_3\text{O}^+]$ is the hydronium ion concentration. At room temperature this corresponds to a shift of the electrode potential of 59.2 mV/pH.

¹This definition of SHE is not completely correct, because SHE is defined through a platinized platinum/electrolyte interface flushed with a constant flow of purified H_2 [114]. However, the above mentioned definition is sufficient for this work.

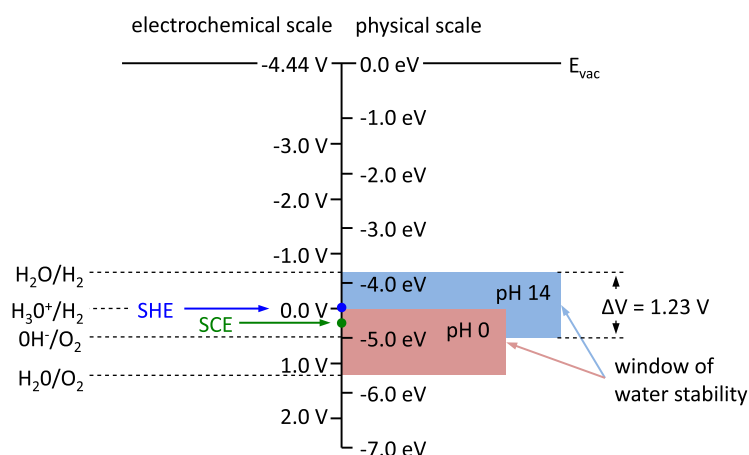


Figure D.1: Comparison of the electrochemical and physical energy scale. The reference of the physical scale is the vacuum energy E_{vac} . The electrochemical scale refers standard hydrogen electrode (SHE) i.e. the hydrogen evolution from water molecules in pH 0. The red and the blue rectangles depict the stability of water in pH 0 and pH 14. SCE denotes the potential level of the saturated calomel electrode at $\approx +0.24$ V, which is used as the reference electrode in this work.

D.2 The BDD/Electrolyte Interface

D.2.1 The Electrochemical Double-Layer

Bringing together a semiconductor and an electrolyte means also combining two different conduction mechanisms. While the electrolyte represents an ionic conductor the semiconductor is an electron or hole conductor. Generally, i.e. in the absence of charge transfer reactions, such an interface has rectifying properties (also in the case of metal/electrolyte interfaces), which prohibits the formation of Ohmic contacts to electrolytes. This is the reason for all electrochemical measurements being done in a three electrode configuration (explained later). The oxygen terminated boron-doped diamond electrode in contact with an electrolyte is a p-type semiconductor with a pinned surface exhibiting a negatively charged space charge region in the vicinity of its surface. As depicted in figure D.2 the fixed negative charges of the BDD attract positive ions of the solution, which are partially adsorbed on the diamond surface. The adsorbed ions approach the diamond surface as close as possible and thereby form the Helmholtz plane, which is defined by the charge centroid of the ions. The distance between the electrode surface and the Helmholtz plane typically ranges between 0.1 nm and 0.2 nm [115]. Usually the charge on the diamond surface alone is not sufficient to counter balance the charge of the space charge region, which is the reason why a part of the counter charge is represented through solvated ions in proximity to the electrode. This region of solvated ions is termed diffusion layer. Together, the Helmholtz layer and diffusion layer form the

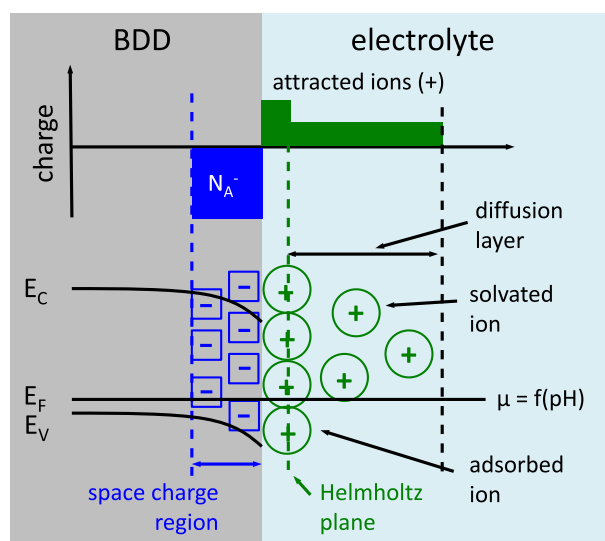


Figure D.2: Sketch of a BDD electrode in contact with an electrolyte. A negatively charged space charge region evolves in the diamond. The corresponding counter charge forms in the electrolyte via adsorbed ions on the diamond surface and solvated ions within the diffusion layer. Cations from the electrolyte approach the diamond surface as close as possible. Their charge centroid defines the Helmholtz plane. The combination of Helmholtz and diffusion layer is the electrochemical double layer.

electrolytic double layer. In electrochemical measurements it can be represented by two plate capacitors in series. Since the Helmholtz layer is very narrow its capacitance is very high (experimentally determined to the range of $5 \mu\text{F}/\text{cm}^2$ to $50 \mu\text{F}/\text{cm}^2$ [115]). However, this value is at least seven times lower than that expected from theoretical calculations assuming a relative permittivity of water of $\epsilon_r \approx 80$. Commonly, a value between $\epsilon_r = 6$ and $\epsilon_r = 8$ is assigned to the relative permittivity of water inside the Helmholtz plane reflecting the lower degree of freedom of motion and reorientation of water dipoles.

D.2.2 The pH-Sensitivity of BDD Electrodes

As already mentioned, the BDD electrode is a p-type semiconductor being in contact with an electrolyte. A schematic representation of the BDD/electrolyte interface for two different pH values is given in figure D.3. When a semiconductor is brought in contact with an electrolyte, the electrochemical potential μ of the electrolyte and the Fermi level E_F of the semiconductor (which is equivalent to the electrochemical potential of electrons in a solid) will align to each other, similar to the case of pn or Schottky diodes. The electrochemical potential combines the energy chemically stored in the electrolyte (chemical potential) and the electrostatic potential, which can be applied externally. The chemical potential is closely related to the electrode potential and also follows the Nernst

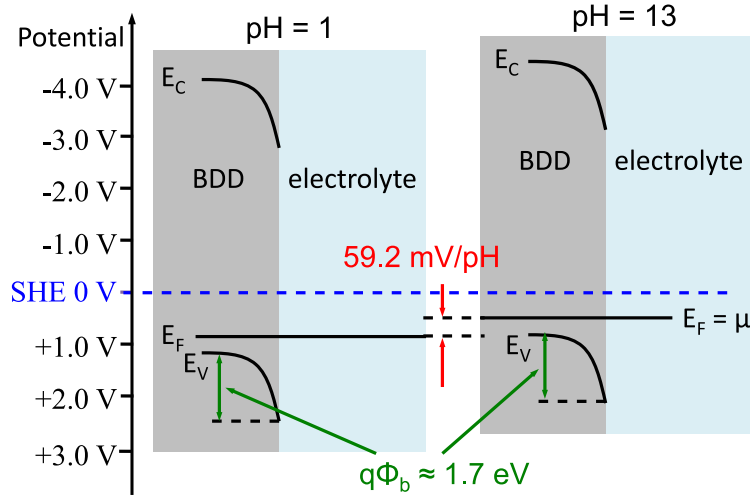


Figure D.3: Schematic representation of the BDD/electrolyte interface for pH = 1 (left) and pH = 13 (right) in equilibrium. The Fermi level and the electrochemical potential are aligned.

equation (see equation (D.7)). In essence, this means that the electrochemical potential of the electrolyte is dependent on both, the applied voltage and the ion concentration.

Oxygen terminated diamond has a pinned surface with a surface barrier of $q\Phi_b \approx 1.7$ eV slightly depending on the individual surface treatment [113]. This barrier height is independent of the exact electrolyte composition. Therefore, when measuring the IV characteristics (by means of cyclic voltammetry) of the BDD/electrolyte junction the resulting curves should be identical for different pH values. However, in reference to a reference electrode (like SHE or SCE) the surface potential decreases with increasing pH. Thus, the pH sensitivity can be interpreted as a pH dependent depletion layer capacitance $C = f(\text{pH})$ in the diamond or as a pH dependent built-in potential $V_{bi} = f(\text{pH})$ at the BDD/electrolyte interface.

D.2.3 Charge Transfer Reactions

Until here, all BDD/electrolyte interactions of this section were discussed under the assumption that no charge is transferred across the phase boundary implying that applied potentials do not lead to the decomposition of water. Although the H_2 and O_2 evolution themselves involve charge transfer it is desirable to investigate reduction and oxidation processes of other species, so called redox systems, dissolved in the electrolyte. Prerequisite certainly is that the standard electrode potential of the reduction and oxidation of the redox system lies within the stability window of water. Otherwise, the current arising through the hydrogen or oxygen evolution would screen that of the redox system. Depicted in figure D.4 is an electrolyte containing a redox system with

both electrode potentials within the water stability window. The redox system always comprises oxidized and reduced states of the investigated species (depicted in the figure as distribution of density of states), although the equilibrium can be shifted towards either site by adding more reducing or oxidizing agents, similar to the case of the pH value. The states below the electrochemical potential or the Fermi level are considered filled. If an electrical field is applied, electrons can transfer from the dissolved molecule to the partially filled surface states of the BDD electrode (loss of electrons \rightarrow oxidation). If the diamond is highly p-type doped, electrons can tunnel through the space charge region into the valence band. Naturally, a similar behavior is found for the reverse direction, when electrons are transferred from the diamond into the electrolyte (gain of electrons \rightarrow reduction). The corresponding current-voltage characteristic is described by the Butler-Volmer equation in the form [115]:

$$j = j_0 \left[\exp \left(\frac{\alpha z F}{R_g T} (V - V_0) \right) - \exp \left(-\frac{(1 - \alpha) z F}{R_g T} (V - V_0) \right) \right] \quad (\text{D.8})$$

where j_0 is the exchange current density at equilibrium, $\alpha = 0 \dots 1$ the anodic transfer coefficient, z the number of transferred electrons, $F = 96485 \text{ C/mol}$ the Faraday constant, $R_g = 8.314 \frac{\text{J}}{\text{mol} \cdot \text{K}}$ the universal gas constant, T the absolute temperature, and V_0 is the equilibrium potential of the reaction, where the net current density is zero. In essence, this means that the above described charge transfer mechanism also occurs under equilibrium conditions. However, the anodic (oxidation) and cathodic (reduction) components of the current density are equal, but of opposite sign and the resulting net current is zero. The rectifying properties of the BDD/electrolyte junction are evident from equation (D.8). Away from equilibrium and depending on the sign of the applied overpotential ($V - V_0$) one of the two exponential terms will dominate resulting in a net anodic (positive, first exponential term) or cathodic current (negative, second exponential term).

D.3 Diffusion Processes

With the before described charge transfer reaction it was implicitly given that there is an infinite amount of donor or acceptor molecules in the vicinity of the electrode surface to contribute to the electrode current. This current described by the Butler-Volmer equation (D.8) mainly depends on the reaction kinetics and is therefore referred to as reaction limited current. Considering for instance the oxidation of molecules, i.e. the loss of electrons at positive electrode potentials, the fact that molecules, which already transferred their electrons, cannot contribute further to the electrode current was not taken into account. This implies that, with time, the electrode surface would be passivated by oxidized molecules and no further charge could be transferred. However, the dissolved molecules diffuse in the electrolyte to maintain equilibrium conditions. This means that also the oxidized species on the electrode surface will diffuse into the

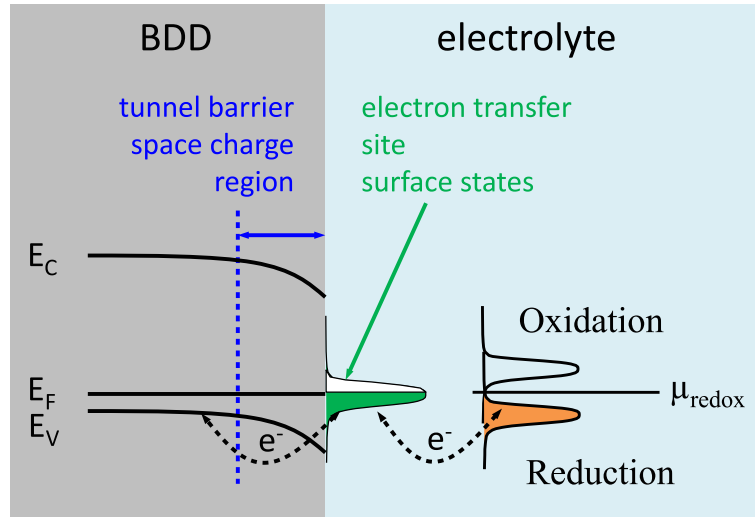


Figure D.4: Sketch of the charge transfer mechanism of redox couples and a BDD electrode. Filled areas represent filled densities of states.

bulk electrolyte and reduced molecules will diffuse towards the electrode surface. Hence, for large overpotentials the electrode current will be limited by this diffusion process.

By modifications of the electrode surface the diffusion process itself can be modified. The two for this work relevant diffusion patterns are illustrated in figure D.5, where figure D.5(a) shows the linear diffusion on a planar large area electrode and figure D.5(b) the hemispherical diffusion on a micro or nano patterned electrode. In the latter depiction the major part of the BDD surface is covered with a passivation layer. Contact between the electrolyte and the active BDD electrode is achieved by small circular openings in this passivation layer. Since the driving force for the diffusion is a gradient of the concentration, such a micro pattern results in diffusion hemispheres allowing fast diffusion of reduced species from all directions towards the active electrode site, whereas in case of the planar electrode the diffusion is directed in one dimension only. However, in a microelectrode array (MEA) configuration the alignment of the individual microelectrodes is crucial for the performance of the array. In order to maintain the hemispherical diffusion pattern the distance between two microelectrodes must be at least 20 times its radius [119]. Otherwise the different diffusion hemispheres will overlap leading to a reduction of the diffusion velocity. For very narrow alignment the diffusion pattern will approach that of the planar electrode.

As mentioned, the driving force for the diffusion is a gradient of the concentration c_b in the electrolyte. The time-dependent concentration profile can be calculated by [114]

$$c(x, t) = c_b \cdot \operatorname{erf} \left(\frac{x}{\sqrt{4Dt}} \right) \quad (\text{D.9})$$

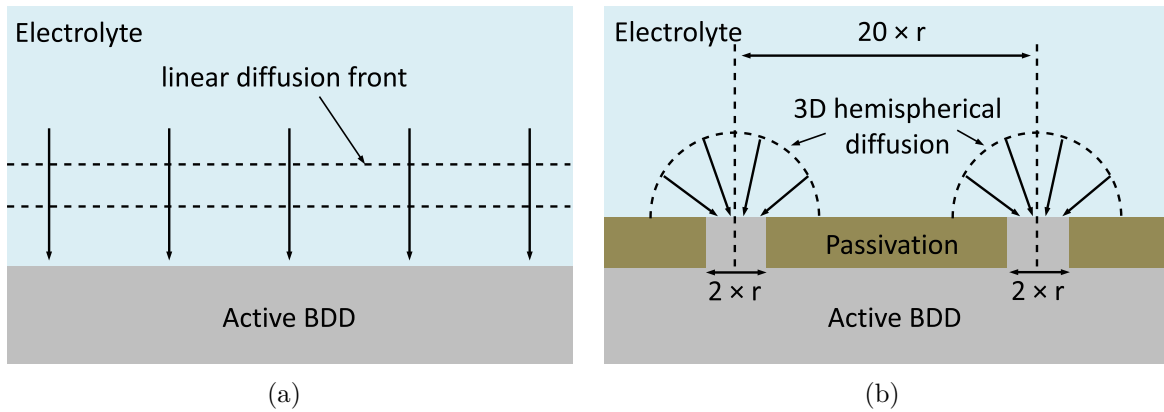


Figure D.5: Illustration of (a) linear and (b) hemispherical diffusion on a large area and a microelectrode array.

for the one-dimensional diffusion on a planar electrode and by

$$c(r, t) = c_b \cdot \left[1 - \frac{r_0}{r} \cdot \operatorname{erfc} \left(\frac{r - r_0}{\sqrt{4Dt}} \right) \right] \quad (\text{D.10})$$

for the three-dimensional hemispherical diffusion on a microelectrode. In these equations x is the distance from the electrode surface (one-dimensional), r the distance from the microelectrode center (three-dimensional), D the diffusion constant, and r_0 the radius of the microelectrode. In both cases the concentration profile shows a significant dependency on the measurement time. This means that the concentration of reduced molecules in the vicinity of the active electrode decreases with measurement duration. However, in case of a microelectrodes the time dependency can be reduced, if small electrode radii were chosen. With the knowledge of the concentration profile the diffusion limited current density can be calculated.

Considering at first the planar large area electrode, its diffusion limited current density is calculated by [114]

$$j = zFc_b \cdot \sqrt{\frac{D}{\pi t}}, \quad (\text{D.11})$$

where c_b is the bulk concentration before the experiment ($t = 0$). Again, the electrode current will show a dependence on the measurement duration. In practical measurements (cyclic voltammetry) this dependency will appear as a dependency on the scan rate $s = \frac{dV}{dt}$. This behavior is depicted by figure D.6(a), where the oxidation of $\text{Ru}(\text{NH}_3)_6^{2+}$ molecules is shown for scan rates of $s = 50 \text{ mV/s}$ and $s = 200 \text{ mV/s}$. As expected, the peak current is significantly higher for a fast scan rate. Moreover, due to the slow diffusion mechanism the electrode current is decreasing with the elapsed time and the potential, at which the peak current is obtained, is slightly shifted towards larger electrode potentials for higher scan rates ($V_{\text{peak}}(s = 50 \text{ mV/s}) = 0.35 \text{ V} \rightarrow V_{\text{peak}}(s = 200 \text{ mV/s}) = 0.38 \text{ V}$). For potentials below V_{peak} the electrode current follows the reaction limited case described by the Butler-Volmer equation (equation (D.8)).

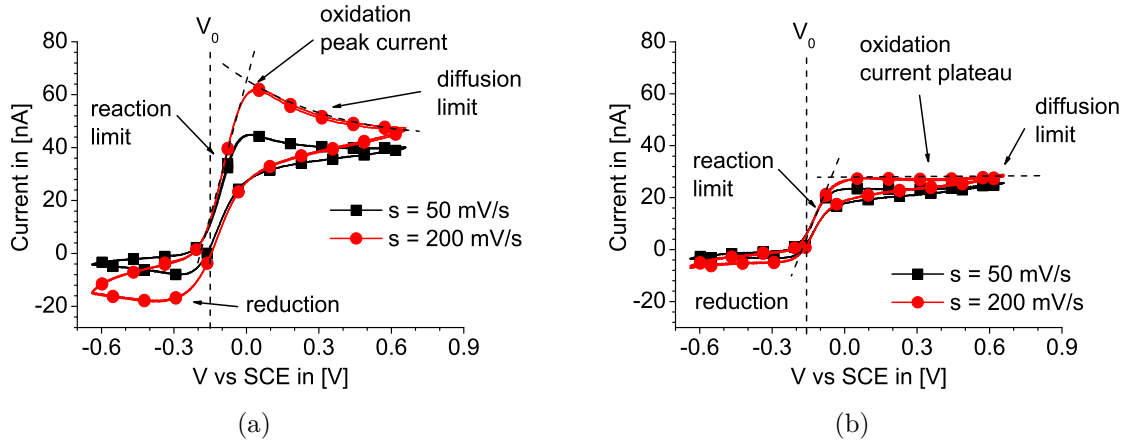


Figure D.6: Cyclic voltammetry measurements with different scan rates (50 mV/s = black squares; 200 mV/s = red circles) for the oxidation of 1 mM $\text{Ru}(\text{NH}_3)_6^{2+}$ on (a) a planar large area electrode and on (b) a microelectrode array.

The situation changes, if a microelectrode array is fabricated according to the above mentioned design criteria. With the enhanced three-dimensional diffusion, its diffusion limited current of an individual microelectrode is calculated by [114]

$$j = zFDc_b \cdot \left(\frac{1}{\sqrt{\pi Dt}} + \frac{1}{r_0} \right). \quad (\text{D.12})$$

The first part of this equation is identical to equation (D.11) and describes the contribution of the linear diffusion. The second part describes the contribution of the hemispherical diffusion, which can be further enhanced by a reduction of the microelectrode radius r_0 . Furthermore, by this presentation it can be seen that the time dependence (= scan rate dependence) of the electrode current becomes negligible, if the radius is much smaller than the diffusion length $\sqrt{4Dt}$. Figure D.6(b) shows the corresponding voltammogram of the oxidation of the $\text{Ru}(\text{NH}_3)_6^{2+}$ redox couple using a MEA structure. The two scan rates were $s = 50 \text{ mV/s}$ and $s = 200 \text{ mV/s}$. Since the microelectrode array and the planar electrode share the same basic device geometry (square with area of $200 \times 200 \mu\text{m}^2$), the two graphs of figure D.6 are presented in the same scale. The first noticeable difference is that the MEA electrode is reduced to approximately half of the planar electrode ($s = 200 \text{ mV/s}$), which is due to the reduced active electrode area. However, considering that more than 99 % of the surface are passivated the reduction of the absolute current corresponds to an increase of the current density (only the active BDD surface) by more than one order of magnitude. Although this is an interesting feature, the main benefits MEAs offer to real sensor device applications are the reduced sensitivity to the scan rate as well as the evolution of a current plateau.

E Determining the Gate-Source Capacitance

As mentioned in chapter 6, the direct measurement of the gate capacitance C_{GS} using the fabricated HEMTs is difficult, because with the small gate dimensions the corresponding complex impedance becomes extremely large, especially at low frequencies. Therefore, one can either rely on measurements in the microwave regime or on measurements on large area test diodes. For measurements in an electrolyte the test frequency is limited to the lower kHz regime. Also, other components of the equivalent circuit, which had not been considered, may become more important or even dominating at very high frequencies. Therefore, microwave measurements seem not the ideal choice for the investigation of the barrier layer capacitance. Instead, here the analysis of the gate-source capacitance is based on measurements on large area, circular test electrodes. As reported in [138] the evaluation of large area gate structures on GaN-based heterostructure is subjected to a non-linear evolution of the capacitance with the gate area, which is why also this method suffers from underestimated capacitance values. Another way to evaluate CV measurements was reported in [139], which is based on the evaluation of the depletion voltage V_{depl} and is therefore also not subjected to distortion possibly caused by a gate leakage current through the InAlN/AlN barrier layer. Applying this method allows accurately determining the relative permittivity ϵ_r of the InAlN barrier from which then the value of the barrier layer capacitance is calculated. The approach to obtain the relative permittivity is briefly discussed in the following.

The described method makes use of CV measurements obtained on samples with varying InAlN barrier thickness ($t_{InAlN} = 3.0, 3.5, 4.0, 4.5,$ and 6.0 nm). Due to their relevance for this work, in the following the oxidized MISHEMT structures will be discussed. CV measurements were conducted for each sample on circular Schottky diodes with different diameters. The investigated diameters were $D = 30 \mu\text{m}$, $D = 40 \mu\text{m}$, and $D = 60 \mu\text{m}$. The test frequency was $f = 1$ MHz. Like discussed in chapter 5, CV measurements can be analyzed according to a series or a parallel circuit model. The resulting capacitances are summarized in figure E.1. Obviously, the two models can produce differing results, especially for very thin barrier layers, where the series resistance of the gate-to-source region cannot be neglected, even though the parallel model is applied (see e.g. figure E.1(e)). Therefore, figure E.1 additionally compares the results of CV measurements to those obtained by impedance spectroscopy, where the measurement results were fitted to a model combining the series and the parallel model (in essence, a

resistance in series to an $R \parallel C$ circuit). In contrast to the electrochemical impedance spectroscopy discussed in chapter 5, the impedance spectroscopy of the gate diodes is not limited to the lower kHz regime, but limited by the measurement setup to the range between 20 Hz and 2 MHz. Generally, the best agreement between CV analysis and impedance spectroscopy is obtained, if the CV measurements were evaluated according to the series model. Therefore, the CV analysis according to the series model will be considered for further investigation. The parameter, which will be used for the following analysis, is the depletion voltage V_{depl} , and is defined at the point, where the 2DEG channel under the gate is depleted and the extracted capacitances approach 0 F under reverse bias conditions. Thus, V_{depl} can be identified with the threshold voltage V_{th} in the HEMT structure.

In contrast to the CV analysis of other semiconductor devices, where the free mobile carriers of the channel arise from doping, the CV curves of GaN based heterostructures, where the 2DEG arises from the polarization discontinuity, produces a nearly constant capacitance within a certain potential regime, which is thought to be related to the capacitance of the InAlN/AlN barrier layer. The observed slight increase of the capacitance with increasing V_{GS} in this potential regime might be due to the quantum capacitance (see 2.4), which, however, will be neglected in the following. Neglecting the quantum capacitance seems reasonable, since here the depletion voltage will be evaluated. Due to the nearly constant capacitance an evaluation of the $1/C^2$ cannot reveal information on the Schottky barrier height Φ_{SB} and therefore remains unknown (especially for Cu gates on oxidized InAlN surfaces). There exist a number of reports in the literature, where it was attempted to extract Φ_{SB} from the IV characteristics, which also might be not suitable, since, even if commonly referred as Schottky contact, the nature of the gate contact in GaN based HEMTs is not really comparable to that of a conventional Schottky diode of a Si or a GaAs Metal-Semiconductor-FET. However, for this method the knowledge of the exact Schottky barrier height is not necessary, since the relative change of the depletion voltage with increasing barrier layer thickness will be evaluated.

In order to describe the analysis in more detail, initially the band diagrams of the InAlN/GaN HEMT with different barrier layer thickness shall be considered. Figure E.2(a) shows the band diagrams under equilibrium conditions, i.e. at $V_{\text{GS}} = 0$ V and figure E.2(b) shows the corresponding band diagrams of depleted sheet charge concentration, i.e. at $V_{\text{GS}} = V_{\text{depl}}$. To keep the evaluation simple the AlN spacer layer is treated as part of the InAlN layer. The native oxide is treated in the same way. Such simplifications will not affect the final result as long as the thicknesses of the AlN spacer and the oxide layer remain constant. Considering at first the band diagrams in equilibrium. The red band diagram depicts the situation of a barrier layer thickness equivalent the critical barrier layer thickness, where the 2DEG carrier concentration n_s is depleted due to the Schottky barrier potential. With increasing barrier thickness the conduction band edge of GaN buffer starts penetrating underneath the Fermi level and electrons start accumulating in the quantum well (blue and green). The thicker the barrier layer, the deeper is the penetration (within certain limits) of E_C below the Fermi energy, and

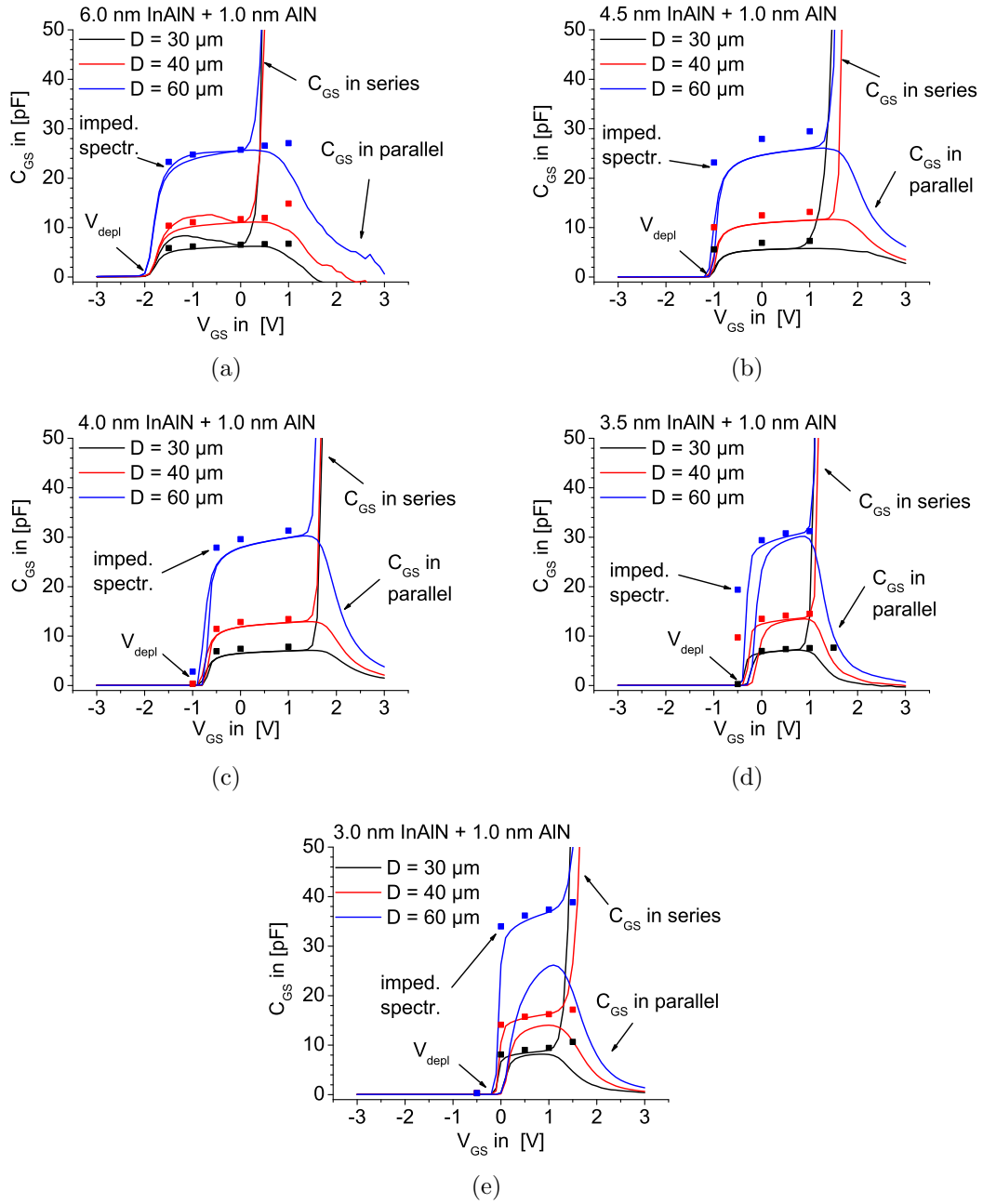


Figure E.1: CV measurements at a test frequency of $f = 1$ MHz on samples with InAlN barrier layer thickness of (a) $t_{InAlN} = 6.0$ nm, (b) $t_{InAlN} = 4.5$ nm, (c) $t_{InAlN} = 4.0$ nm, (d) $t_{InAlN} = 3.5$ nm, and (e) $t_{InAlN} = 3.0$ nm, on circular test diodes with diameters of $D = 30$ μ m, $D = 40$ μ m, and $D = 60$ μ m. The symbols present values obtained by impedance spectroscopy.

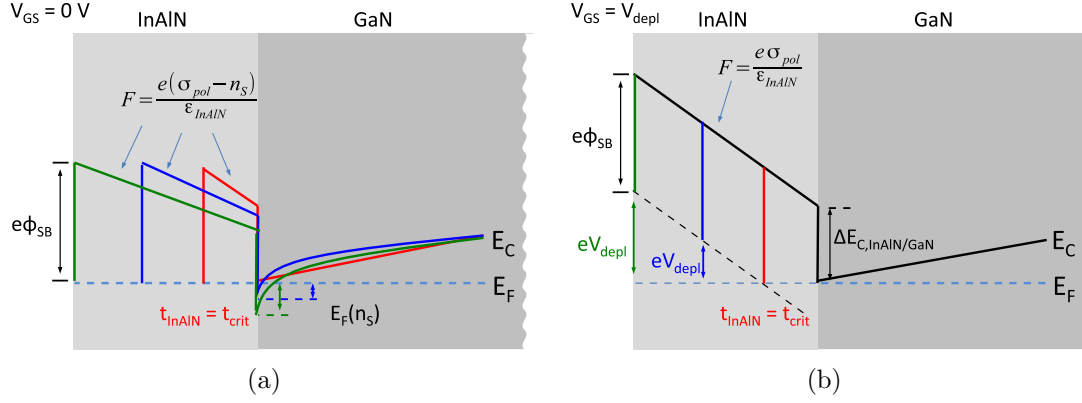


Figure E.2: Schematic band diagrams of InAlN/GaN HEMTs with different barrier layer thicknesses under (a) equilibrium conditions and (b) under depletion conditions.

consequently the larger is n_s in the channel. The electrical field in the InAlN barrier is partially compensated by n_s and follows the equation

$$F = \frac{e \cdot (\sigma_{pol} - n_s)}{\varepsilon_{InAlN}}, \quad (E.1)$$

where $P_{sp,InAlN} = e\sigma_{pol}$ is the spontaneous polarization of the InAlN barrier. The value of n_s can only be calculated through numerical iterations, which is why it is beneficial to investigated cases, where the influence of the carrier concentration vanishes. Such cases are illustrated in figure E.2(b), where n_s vanishes by applying a gate bias equal to the depletion voltage. Under these conditions the electrical field in the barrier does not longer depend on the carrier concentration. Furthermore, any influence arising from the Schottky barrier height can be neglected, because it would present a constant off-set, independent of the barrier thickness. In other words, the Schottky barrier height can significantly influence the critical barrier layer thickness or the value of the depletion voltage at a given barrier thickness, but it cannot affect the ratio $\Delta V_{depl}/\Delta t_{InAlN}$. This means that the electrical field across the InAlN barrier is equivalent to the polarization field and equation (E.1) simplifies to

$$F = \frac{e \cdot \sigma_{pol}}{\varepsilon_{InAlN}}. \quad (E.2)$$

The depletion voltages of the different samples are extracted from figure E.1 and summarized in figure E.3(a). From the change of the depletion voltage with barrier layer thickness the polarization field of the InAlN barrier is determined to $F = \Delta V/\Delta t_{InAlN} = -6.4$ MV/cm. In order to calculate now the relative permittivity of the lattice matched InAlN, first its spontaneous polarization needs to be determined, which can be calculated by [45]

$$P_{sp,InAlN}(x) = -0.042 \cdot x - 0.090 \cdot (1 - x) + 0.07 \cdot x \cdot (1 - x) \quad (E.3)$$

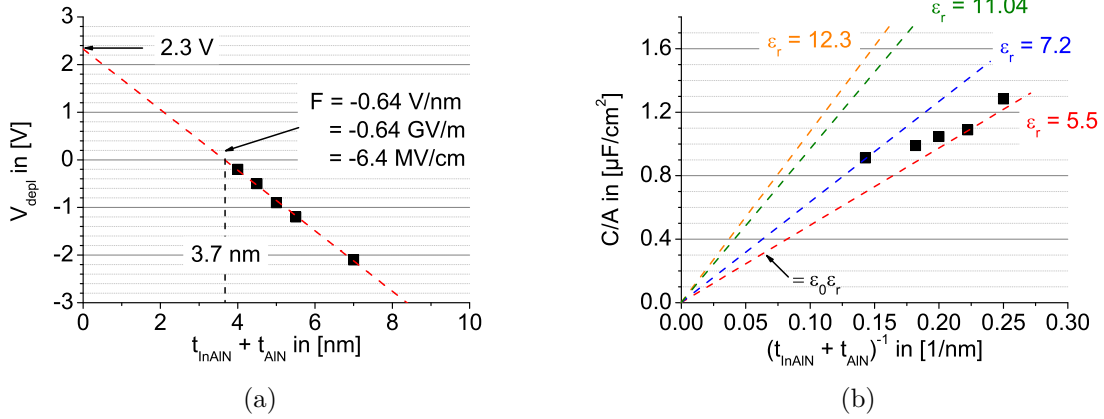


Figure E.3: (a) From figure E.1 extracted depletion voltage V_{depl} vs. total barrier thickness. The change of V_{depl} with barrier thickness is -0.64 V/nm presenting the electrical field across the lattice matched InAlN barrier. (b) Change of the resulting capacitances with barrier layer thickness $1/(t_{\text{InAlN}} + t_{\text{AlN}})$ using different ϵ_r compared to the values obtained by simple CV analysis.

yielding $P_{\text{sp,InAlN}} = -0.071 \frac{\text{C}}{\text{m}^2}$ for the lattice matched case ($x = 0.17$). The relative permittivity of the InAlN barrier can now be calculated by using this value in equation (E.2), yielding

$$\epsilon_{\text{InAlN}} = \frac{P_{\text{sp,InAlN}}}{\epsilon_0 \cdot F} = \frac{-0.071 \frac{\text{C}}{\text{m}^2}}{8.854 \times 10^{-12} \frac{\text{C}}{\text{V} \cdot \text{m}} \cdot -6.4 \times 10^8 \frac{\text{V}}{\text{m}}} = 12.3, \quad (\text{E.4})$$

a value, which is close to that predicted by Vegard's law, where the value of the ternary alloy is given by the weighted average of the binary compounds and yields in case of the lattice matched (17 % In) configuration

$$\epsilon(\text{In}_x\text{Al}_{1-x}\text{N}) = \epsilon_{\text{InN}} \cdot x + \epsilon_{\text{AlN}} \cdot (1 - x) = 14.61 \cdot 0.17 + 10.31 \cdot 0.83 = 11.04. \quad (\text{E.5})$$

Figure E.3(b) compares the resulting capacitances for a relative permittivity of $\epsilon_r = 12.3$ (described method) and $\epsilon_r = 11.04$ (Vegard's law) to those obtained by CV measurements (compare figure E.1). Using the well known relation

$$\frac{C}{A} = \frac{\epsilon_0 \cdot \epsilon_r}{t} \quad (\text{E.6})$$

yields in the worst case $\epsilon_r = 5.5$ ($t_{\text{InAlN}} = 3.5$ nm) and in the best case an $\epsilon_r = 7.2$ ($t_{\text{InAlN}} = 6$ nm). This means that the gate-source capacitance is underestimated by approximately 50 %, when relying on CV measurements on large area test structures. However, in this experiment the deviation is more prominent for thin barriers. Speculating on a reason for this deviation supports the fact that in simple CV analysis a (probably constant) parameter is entirely neglected. Such a parameter could be given

by the conduction band offset $\Delta E_{C,\text{InAlN}/\text{GaN}}$, which is independent of the barrier layer thickness and therefore may have less influence in thick layers. Another possibility might be the quantum capacitance, which was neglected in equation (E.6). However, this has not been investigated further.

Another interesting feature of figure E.3(a) is presented by the depletion voltage at 0 nm barrier thickness (to be more precise $t \rightarrow 0$ nm, V_{depl} is then the voltage necessary to start accumulating charges in the channel), because it presents a measure for the Schottky barrier height. Considering again the band diagrams of figure E.2(b) it is evident that the depletion voltage plus the Schottky barrier height is equal to the potential drop across the barrier plus the conduction band offset. The corresponding equation is:

$$e \cdot \Phi_{SB} + e \cdot V_{\text{depl}} = e \cdot F \cdot t_{\text{InAlN}} + \Delta E_{C,\text{InAlN}/\text{GaN}} \quad (\text{E.7})$$

For an infinitesimal thin barrier, the voltage drop across the barrier is 0 and it follows:

$$e \cdot \Phi_{SB} = \Delta E_{C,\text{InAlN}/\text{GaN}} - e \cdot V_{\text{depl}} \quad (\text{E.8})$$

The conduction band offset of a random InAlN ternary alloy on GaN is calculated after [45]

$$\Delta E_{C,\text{InAlN}/\text{GaN}} = 0.63 \cdot (E_{g,\text{InAlN}} - E_{g,\text{GaN}}) = 0.63 \cdot (4.44 \text{ eV} - 3.4 \text{ eV}) = 0.65 \text{ eV} \quad (\text{E.9})$$

where the band gap is

$$E_{g,\text{InAlN}}(x) = 0.7 \cdot x + 6.13 \cdot (1 - x) - 5.4 \cdot x \cdot (1 - x) = 4.4 \text{ eV}. \quad (\text{E.10})$$

Using these numbers and the depletion voltage at 0 nm in equation (E.8) results in a Schottky barrier height of Cu gates on oxidized lattice matched InAlN barriers of $\Phi_{SB} = 2.95$ V. However this value might be subjected to certain inaccuracies, because the oxidation process reduces the InAlN thickness and consequently the real value might be smaller. Naturally it would decrease by 0.64 V/nm. Assuming the formation of a 1.5 nm thin native oxide [38] a reduction of the barrier height to 2 V could be expected. However, in that case also the band diagram would need to be complemented by the native oxide. Then, the band alignment of this oxide to the InAlN barrier presents another unknown parameter, which influences the Schottky barrier height.

F Additional Data for Hybrid Measurement

The two in section 6.4 not shown linear transfer characteristics are shown in figure F.1, where the large area BDD electrode is connected to an InAlN GaN with $W_G = 50 \mu\text{m}$ and $W_G = 100 \mu\text{m}$. The corresponding semilogarithmic transfer characteristics are shown in figure F.2

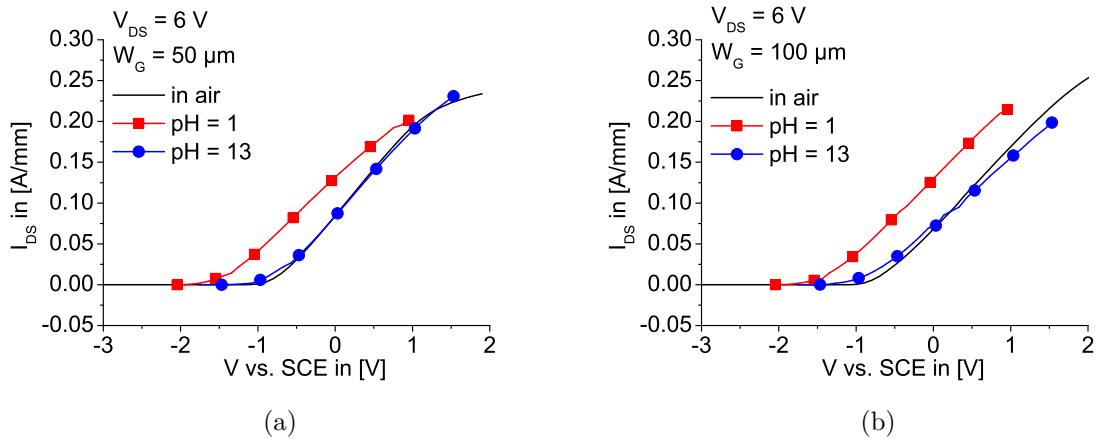


Figure F.1: Linear transfer characteristics at $V_{DS} = 6$ V of the whole system in ISFET configuration. The large area electrode is connected to (a) a $50 \mu\text{m}$ wide and to (b) a $100 \mu\text{m}$ wide gate device.

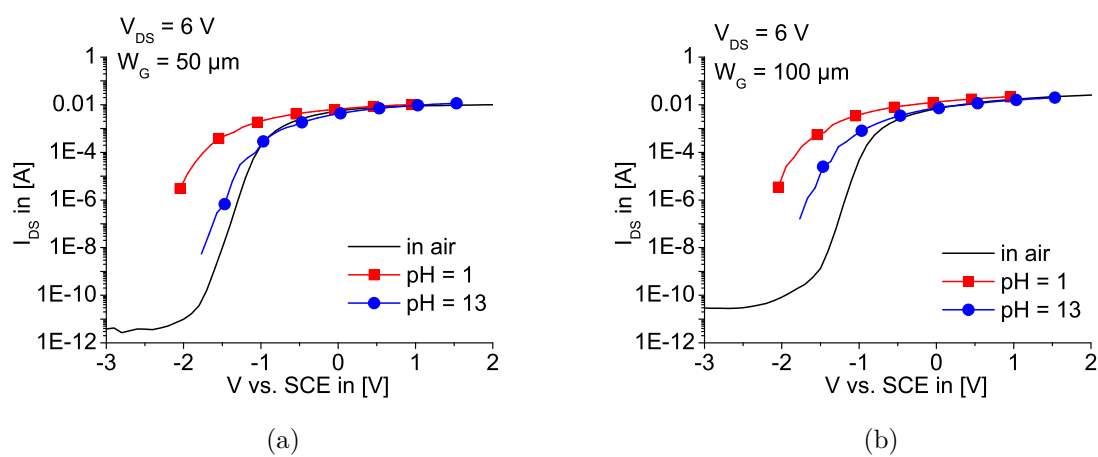


Figure F.2: Semilogarithmic transfer characteristics at $V_{DS} = 6$ V of the whole system in ISFET configuration. The large area electrode is connected to (a) a 50 μ m wide and to (b) a 100 μ m wide gate device.

List of Publications

Journals

- J. Kusterer, A. Lüker, P. Herfurth, Y. Men, W. Ebert, P. Kirby, M. O’Keefe, and E. Kohn, *Piezo-actuated nanodiamond cantilever technology for high-speed applications*, Diamond and Related Materials, vol. 17 (2008), pp 1429–1433.
- E. Colombo, Y. Men, J. Scharpf, C. Pietzka, M. Dipalo, P. Herfurth, Z. Gao, M. Schneider, V. Carabelli, E. Carbone, E. Kohn, A. Pasquarelli, *Fabrication of a NCD microelectrode array for amperometric detection with micrometer spatial resolution*, Diamond and Related Materials, vol. 20 (2011), pp 793–797.
- P. Herfurth, Y. Men, R. Rösch, N. Grandjean, and E. Kohn, *GaN on sapphire mesa technology*, Proceedings on 9th International Conference on Nitride Semiconductors, Phys. Status Solidi C 9 (2012), No. 3–4, pp. 945–948.
- C. Ostermaier, M. Alomari, P. Herfurth, D. Maier, A. Alexewicz, M.-A. di Forte-Poisson, S. L. Delage, G. Strasser, D. Pogany, E. Kohn, *Reliability investigation of the degradation of the surface passivation of InAlN/GaN HEMTs using a dual gate structure*, Microelectronics Reliability, vol. 52 (2012), Issues 9-10, pp. 1812-1815.
- P. Herfurth, D. Maier, Y. Men, R. Rösch, L. Lugani, J.-F. Carlin, N. Grandjean, and E. Kohn, *Ultrathin Body InAlN/GaN HEMTs for High Temperature (600 °C) Electronics*, IEEE Electron Device Letters, vol. 34 (2013), no. 4, pp.496-498.
- L. Lugani, J.-F. Carlin, M. A. Py, D. Martin, F. Rossi, G. Salviati, P. Herfurth, E. Kohn, J. Bläsing, A. Krost, and N. Grandjean, *Ultrathin InAlN/GaN heterostructures on sapphire for high on/off current ratio high electron mobility transistors*, Journal of Applied Physics , vol. 113, no. 21 (2013), pp.214503,214503-6.
- P. Herfurth, D. Maier, Y. Men, R. Rösch, L. Lugani, J.-F. Carlin, N. Grandjean, and E. Kohn, *GaN-on-Insulator technology for high-temperature electronics beyond 400 °C*, Semiconductor Science and Technology, vol. 28 (2013), pp. 074026.

Oral and Poster Presentations

- **P. Herfurth**, D. Kueck, M. Alomari, and E. Kohn, *Analytical dual gate FET model to identify surface charge instabilities in the gate drain drift region*, Workshop on Compound Semiconductor Devices and Integrated Circuits Europe (WOCSDICE), Mai 17-20, 2009, Malaga, Spain.
- **E. Colombo**, C. Pietzka, B. Barabelli, Z. Gao, P. Herfurth, Y. Men, M. Schneider, E. Arbone, E. Kohn, and A. Pasquarelli, *Transparent NCD microelectrode array for spatially resolved detection in micro-areas of single cells*, International Meeting on Substrate-Integrated Microelectrode Arrays (MEA Meeting), 29.6-2.7, 2010, Reutlingen, Germany.
- P. Herfurth, Y. Men, R. Rösch, N. Grandjean, and **E. Kohn**, *GaN-on-Insulator mesa technology*, European Workshop on Heterostructure Technology (HETECH), Oct. 18-20, 2010, Fodele, Crete, Greece.
- **P. Herfurth**, M. Alomari, J.-F. Carlin, N. Grandjean, C. Garquiere, M.-A. Difforte-Poisson, S. Delage, and E. Kohn, *Passivation Studies on InAlN/GaN-HEMT Devices*, Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), Feb. 14-17, 2010, Newport Beach, California, USA.
- **P. Herfurth**, C. Steinmann, Y. Men, Z. Gao, E. Colombo, R. Rösch, A. Pasquarelli, and E. Kohn, *InAlN/GaN HEMT with submicron buffer*, Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), Feb. 20-23, 2011, Savannah, Georgia, USA.
- **P. Herfurth**, Y. Men, R. Rösch, N. Grandjean, and E. Kohn, *GaN on sapphire mesa technology*, International Conference on Nitride Semiconductors (ICNS), July 10-15, 2011, Glasgow, Scotland.
- **P. Herfurth**, David Maier, Yakiv Men, Rudolf Rösch, Lorenzo Lugani, Jean-Francois Carlin, Nicolas Grandjean, and Erhard Kohn, *GaN-on-Sapphire Technology for High Temperature Electronics*, International Workshop on Nitride Semiconductors (IWN), Oct. 14-19, 2012, Sapporo, Japan.
- C. Ostermaier, P. Lagger, M. Alomari, P. Herfurth, D. Maier, **A. Alexewicz**, M.-A. Di Forte-Poisson, S. L. Delage, G. Strasser, D. Pogany and E. Kohn, *GReliability Investigation of the Degradation of the Surface Passivation of InAlN/GaN HEMTs using a Dual Gate Structure*, 23 rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Oct. 1-5, 2012, Cagliari, Italy.

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